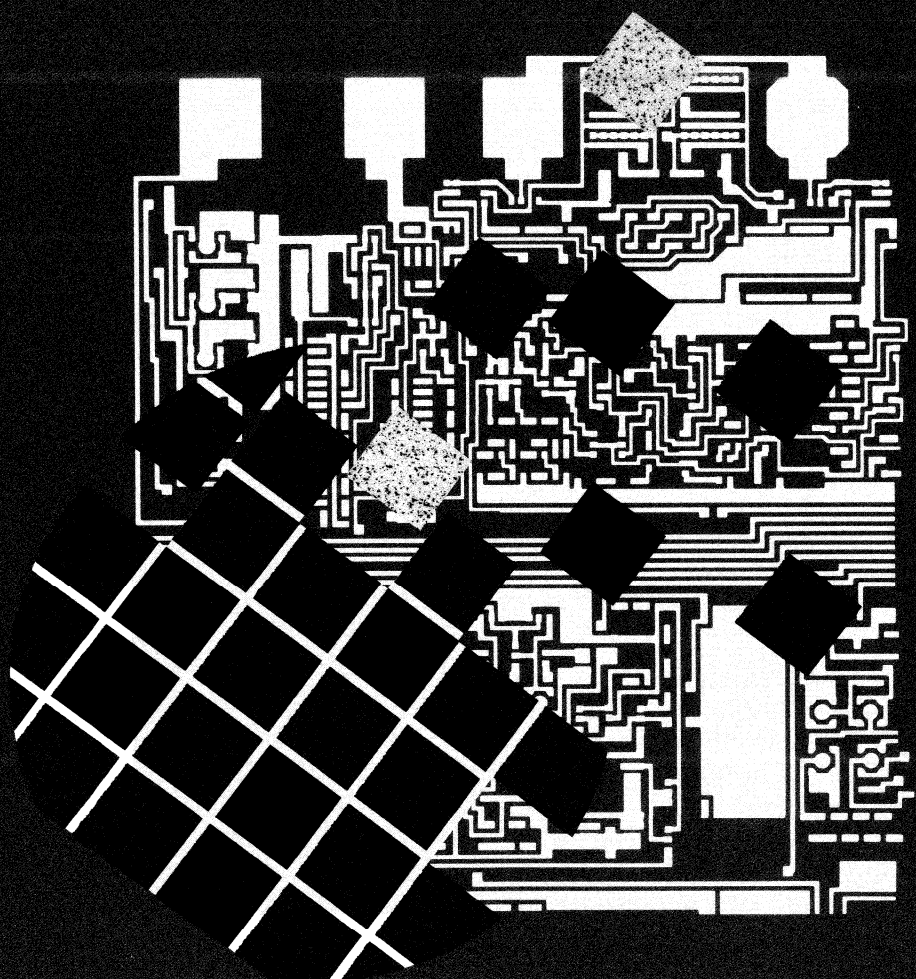
1991 DATA BOOK

Semi-Standard Analog



Micro Linear

Introduction

Founded in 1983, with headquarters in San Jose, California, Micro Linear is a leading manufacturer of high performance standard and semi-standard analog and mixed-signal ICs for specific market applications as well as supplying analog user-specific integrated circuits (USICs).

Focusing at achieving the high levels of integration customers want, Micro Linear provides ICs at the sub-system level, addressing five specific end markets: power and motion control, hard disk drives, analog telecom, local area networks and data converters/ filters. These products use a variety of bipolar and CMOS process technologies chosen to optimize performance and level of integration.

For power control applications where high volumetric efficiency is a benefit, Micro Linear offers a broad line of high-frequency switching power supply controllers. Anticipating the emerging energy and noise regulations for electronic equipment, Micro Linear introduced the industry's first power factor control IC and has followed that up with a family of products applicable to many types of electronic equipment including electronic lamp ballasts.

Micro Linear has emerged as a major supplier to the competitive, fast moving and high volume hard disk drive industry. High performance analog ICs are supplied for the three subsystem areas: data path signal processing, head positioning and motor control. Its products have been widely used in 3.5 inch drives, led by its dedicated servo chip set which establishes the standard for minimum access time disk drives.

The company's telecommunications IC's meet the demanding technical specifications required for Network Communications Terminating Equipment (NCTE). The NCTE products consist of a broad line of programmable attenuators, line equalizers, tone detectors and generators.

In the local area network market, Micro Linear has focused on supplying transceivers that conform to the IEEE 802 standards for transmission over twisted copper wire pairs and fiber optics. The company presently supplies standard and semi-standard 10Base-T transceivers for computer terminations and Multiport Repeaters and quantizers for fiber optic based systems.

Among its converter and filter products are high performance A/D and D/A converters and switched capacitor filters. The A/D's range from 8- to 12- bits and use electronic techniques, such as digital correction, instead of trim methods to achieve cost effective high performance parts.

A pioneer in analog semi-custom integrated circuits, Micro Linear continues to expand its unique tile array for use in USICs. This advanced proprietary tile array approach methodology means that custom designs can be easily and quickly integrated into silicon with minimum expense.

Since its inception, Micro Linear has been committed to excellence in every facet of design and manufacturing. Micro Linear has focused its resources on supplying customers with exceptionally high quality, reliable, and responsive service.

Micro Linear Corporation Data Book 1991

LIFE SUPPORT POLICY

MICRO LINEAR'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF MICRO LINEAR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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Micro Linear

Micro Linear

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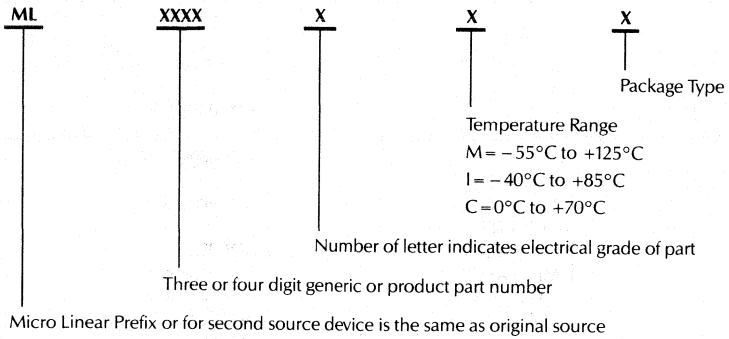
General Information

Section 1

Part Number and Package Type Explanation

PART NUMBER



PACKAGE TYPE

Letter Suffix	Description
D	Side Brazed Hermetic DIP
F	Flat Pack
J	Ceramic Hermetic DIP (CERDIP)
L	Ceramic Leadless Chip Carrier (LCC)
P	Plastic DIP
Q	Plastic Chip Carrier (PCC)
S	Small Outline (SOIC)

Alternate Source Part Number

Analog Devices

Analog Devices Part Number	Micro Linear Direct Replacement[1]
AD7820BQ	ML2261CIJ
AD7820CQ	ML2261BIJ
AD7820KN	ML2261CCP
AD7820KP	ML2261CCQ
AD7820LN	ML2261BCP
AD7820LP	ML2261BCQ
AD7820TQ	ML2261CMJ
AD7820UQ	ML2261BMJ
AD7824BQ	ML2264CIJ
AD7824CQ	ML2264BIJ
AD7824KN	ML2264CCP
AD7824LN	ML2264BCP
AD7824TQ	ML2264CMJ
AD7824UQ	ML2264BMJ

Exar

Exar Part Number	Micro Linear Direct Replacement[1]
XR117R-2CP	ML117R-2CP
XR117R-4CP	ML117R-4CP
XR117R-4MD	ML117R-4CS
XR117R-6CJ	ML117R-6CQ
XR117R-6CP	ML117R-6CP
XR117R-6MD	ML117R-6CS
XR117-2CN	ML117-2CJ
XR117-2CP	ML117-2CP
XR117-2MD	ML117-2CS
XR117-4CN	ML117-4CJ
XR117-4CP	ML117-4CP
XR117-4MD	ML117-4CS
XR117-6CJ	ML117-6CQ
XR117-6CN	ML117-6CJ
XR117-6CP	ML117-6CP
XR117-6MD	ML117-6CS

Linear Technology

LTC Part Number	Micro Linear Direct Replacement[1]
LTC1060ACJ	ML2110BIJ[2]
LTC1060ACN	ML2110BCP[2]
LTC1060AMJ	ML2110BMJ[2]
LTC1060CJ	ML2110CIJ[2]
LTC1060CN	ML2110CCP[2]
LTC1060MJ	ML2110CMJ[2]

National Semiconductor

NSC Part Number	Micro Linear Direct Replacement[1]
ADC0808CJ	ADC0808CJ ML2258BMJ
ADC0808CCJ	ADC0808CCJ ML2258BIJ
ADC0808CCV	ADC0808CCV ML2258BIQ
ADC0809CCN	ADC0808CCN ML2258CIP
ADC0809CCV	ADC0809CCV ML2258CIQ
ADC0820BCJ	ML2261BIJ
ADC0820BCN	ML2261BCP
ADC0820BCV	ML2261BCQ
ADC0820CCJ	ML2261CIJ
ADC0820CCN	ML2261CCP
ADC0820CCV	ML2261CCQ
ADC0820CJ	ML2261CMJ
ADC0831BCJ	ADC0831BCJ ML2281BIJ
ADC0831BCN	ADC0831BCN ML2281BCP
ADC0831CCJ	ADC0831CCJ ML2281CIJ
ADC0831CCN	ADC0831CCN ML2281CCP
ADC0832BCJ	ADC0832BCJ ML2282BIJ
ADC0832BCN	ADC0832BCN ML2282BCP
ADC0832CCJ	ADC0832CCJ ML2282CIJ
ADC0832CCN	ADC0832CCN ML2282CCP
ADC0833BCJ	ADC0833BCJ ML2283BIJ
ADC0833BCN	ADC0833BCN ML2283BCP
ADC0833CCJ	ADC0833CCJ ML2283CIJ
ADC0833CCN	ADC0833CCN ML2283CCP
ADC0834BCJ	ADC0834BCJ ML2284BIJ
ADC0834BCN	ADC0834BCN ML2284BCP

Note 1. 100% pin-for-pin compatible with improved electrical specifications.
Note 2. Consult data sheet for electrical specifications that may vary from limit or conditions of alternate source.
Note 3. Alternate source ships –40°C to +85°C product as molded; Micro Linear does this on a customer need basis.

National Semiconductor (Continued)

NSC Part Number	Micro Linear Direct Replacement[1]
ADC0834CCJ	ADC0834CCJ
	ML2284CIJ
ADC0834CCN	ADC0834CCN
	ML2284CCP
ADC0838BCJ	ADC0838BCJ
	ML2288BIJ
ADC0838BCN	ADC0838BCN
	ML2288BCP
ADC0838BCV	ADC0838BCV
	ML2288BCQ
ADC0838CCJ	ADC0838CCJ
	ML2288CIJ
ADC0838CCN	ADC0838CCN
	ML2288CCP
ADC0838CCV	ADC0838CCV
	ML2288CCQ
ADC1061CIJ	ML2271CIJ
ADC1061CIN	ML2271CCP[3]
ADC1061CIWM	ML2271CCS[3]
ADC1061CMJ	ML2271CMJ
DP5016QC	ML501-6CQ
DP5016RQC	ML501R-6CQ
DP5018QC	ML501-8CQ
DP5018RQC	ML501R-8CQ
μA5016QC	ML501-6CQ
μA5016RQC	ML501R-6CQ
μA5018QC	ML501-8CQ
μA5018RQC	ML501R-8CQ
DP8464BN-3	ML8464B-3CP[2]
DP8464BV-3	ML8464B-3CQ[2]
DP8464BN-2	ML8464B-2CP[2]
DP8464BV-2	ML8464B-2CQ[2]
DP8464BN-2	ML8464B-2CP[2]
DP8464BN-3	ML8464B-3CP[2]
DP8464BV-2	ML8464B-2CQ[2]
DP8464BV-3	ML8464B-3CQ[2]
DP8468BTP-3	ML4568-3CQ[2]
DP8468BTP-2	ML4568-2CQ[2]
LMF100CCN	ML2111CCP
LMF100CCWM	ML2111CCS
MF10AJ	ML2110CMJ[2]
MF10ACN	ML2110BCP[2]
MF10CCJ	ML2110CIJ[2]
MF10CCWM	ML2110CCS[2]
MF10CCN	ML2110CCP[2]

Silicon Systems, Inc.

SSI Part Number	Micro Linear Direct Replacement[1]
SSI 32P541-CH	ML541CQ
SSI 32P541-P	ML541CP
SSI 32P541A-CH	ML4042CQ
SSI 32P541A-P	ML4042CP
SSI 32P541B-CH	ML4042CQ
SSI 32P541B-P	ML4042CP
SSI 32R117R-2P	ML117R-2CP
SSI 32R117R-4F	ML117R-4CF
SSI 32R117R-4P	ML117R-4CP
SSI 32R117R-6F	ML117R-6CF
SSI 32R117R-6H	ML117R-6CQ
SSI 32R117R-6P	ML117R-6CP
SSI 32R117-2P	ML117-2CP
SSI 32R117-4F	ML117-4CF
SSI 32R117-4P	ML117-4CP
SSI 32R117-6F	ML117-6CF
SSI 32R117-6H	ML117-6CQ
SSI 32R117-6P	ML117-6CP
SSI 32R501R-6H	ML501R-6CQ
SSI 32R501R-8F	ML501R-8CF
SSI 32R501R-8H	ML501R-8CQ
SSI 32R501R-8P	ML501R-8CP
SSI 32R501-6H	ML501-6CQ
SSI 32R501-8F	ML501-8CF
SSI 32R501-8H	ML501-8CQ
SSI 32R501-8P	ML501-8CP
SSI 32R511R-4S	ML511R-4CS
SSI 32R511R-6H	ML511R-6CQ
SSI 32R511R-6P	ML511R-6CP
SSI 32R511R-6S	ML511R-6CS
SSI 32R511R-8H	ML511R-8CQ
SSI 32R511R-8P	ML511R-8CP
SSI 32R511R-8S	ML511R-8CS
SSI 32R511-4S	ML511-4CS
SSI 32R511-6H	ML511-6CQ
SSI 32R511-6P	ML511-6CP
SSI 32R511-6S	ML511-6CS
SSI 32R511-8H	ML511-8CQ
SSI 32R511-8P	ML511-8CP
SSI 32R511-8S	ML511-8CS

Note 1. 100% pin-for-pin compatible with improved electrical specifications.
Note 2. Consult data sheet for electrical specifications that may vary from limit or conditions of alternate source.
Note 3. Alternate source ships –40°C to +85°C product as molded; Micro Linear does this on a customer need basis.

Texas Instruments

NSC Part Number	Micro Linear Direct Replacement[1]
ADC0808MJ	ML2258BMJ
ADC0808FN	ML2258BCQ
ADC0808N	ML2258BIP
ADC0809FN	ML2258CCQ
ADC0809N	ML2258CIP
TLC0820ACN	ML2261CCP
TLC0820ACFN	ML2261CCQ
TLC0820BCN	ML2261BCP
TLC0820BCFN	ML2261BCQ
ADC0831ACP	ML2281CCP
ADC0831AIP	ML2281CIJ[3]
ADC0831BCP	ML2281BCP
ADC0831BIP	ML2281BIJ[3]
ADC0832ACP	ML2282CCP
ADC0832AIP	ML2282CIJ[3]
ADC0832BCP	ML2282BCP
ADC0832BIP	ML2282BIJ[3]
ADC0834ACN	ML2284CCP
ADC0834AIN	ML2284CIJ[3]
ADC0834BCN	ML2284BCP
ADC0834BIN	ML2284BIJ[3]
ADC0838ACN	ML2288CCP
ADC0838AIN	ML2288CIJ[3]
ADC0838CCN	ML2288BCP
ADC0838BIN	ML2288BIJ[3]

Unitrode

Unitrode Part Number	Micro Linear Direct Replacement[1]
UC1823J	ML4823MJ
UC1825J	ML4825MJ
UC2823N	ML4823IP
UC2823Q	ML4823IQ
UC2825N	ML4825IP
UC2825Q	ML4825IQ
UC3823N	ML4823IP
UC3823Q	ML4823CQ
UC3825N	ML4825IP
UC3825Q	ML4825CQ

VTC

VTC Part Number	Micro Linear Direct Replacement[1]
VM117-2DK	ML117-2CJ
VM117-2PK	ML117-2CP
VM117-4FK	ML117-4CF
VM117-4PK	ML117-4CP
VM117-4DK	ML117-4CJ
VM117-6PK	ML117-6CP
VM117-6DK	ML117-6CJ
VM117-6PK	ML117-6CP
VM117-6PLK	ML117-6CQ
VM117R-2DK	ML117R-2CJ
VM117R-2PK	ML117R-2CP
VM117R-4FK	ML117R-4CF
VM117R-4PK	ML117R-4CP
VM117R-4DK	ML117R-4CJ
VM117R-6DK	ML117R-6CJ
VM117R-6PK	ML117R-6CP
VM117-6PLK	ML117R-6CQ
VM217-6PK	ML501-6CP
VM217-6PLK	ML501-6CQ
VM217-8PK	ML501-8CP
VM217-8PLK	ML501-8CQ

Note 1. 100% pin-for-pin compatible with improved electrical specifications.
Note 2. Consult data sheet for electrical specifications that may vary from limit or conditions of alternate source.
Note 3. Alternate source ships –40°C to +85°C product as molded; Micro Linear does this on a customer need basis.

Alpha Numeric Index

A/D Converters, D/A Converters

Section 2

Selection Guide

Part Number	Resolution (Bits)	Non Linearity (Max LSB)	Dynamic Performance Signal to Noise Ratio	Conversion Time (μs)	Power Supplies (V)	Temperature Range[1] C	I	M	Package	Comments
ADC0808	8	±1/2		6.6	5 (±10%)	X	X	X	28-Pin DIP, 28-Pin PCC	μP Comp, 8-CH
ADC0809	8	±1		6.6	5 (±10%)	X	X	X	28-Pin DIP, 28-Pin PCC	μP Comp, 8-CH
ADC0831B	8	±1/2		6.0	5 (±10%)	X	X	X	8-Pin DIP	Serial I/O, Single CH
ADC0831C	8	±1		6.0	5 (±10%)	X	X	X	8-Pin DIP	Serial I/O, Single CH
ADC0832B	8	±1/2		6.0	5 (±10%)	X	X	X	8-Pin DIP	Serial I/O, 2-CH
ADC0832C	8	±1		6.0	5 (±10%)	X	X	X	8-Pin DIP	Serial I/O, 2-CH
ADC0833B	8	±1/2		6.0	5 (±10%)	X	X	X	14-Pin DIP	Serial I/O, 4-CH
ADC0833C	8	±1		6.0	5 (±10%)	X	X	X	14-Pin DIP	Serial I/O, 4-CH
ADC0834B	8	±1/2		6.0	5 (±10%)	X	X	X	14-Pin DIP	Serial I/O, 4-CH
ADC0834C	8	±1		6.0	5 (±10%)	X	X	X	14-Pin DIP	Serial I/O, 4-CH
ADC0838B	8	±1/2		6.0	5 (±10%)	X	X	X	20-Pin DIP, 20-Pin PCC	Serial I/O, 8-CH
ADC0838C	8	±1		6.0	5 (±10%)	X	X	X	20-Pin DIP, 20-Pin PCC	Serial I/O, 8-CH
ML2200B	12 + Sign	±3/4	12kHz, ±2.5V SINE, S/N 72dB	31.5	±5 (±5%)	X			40-Pin DIP	4-CH Data Acq Peripheral
ML2200C	12 + Sign	±1	12kHz, ±2.5V SINE, S/N 72dB	31.5	±5 (±5%)	X			40-Pin DIP	4-CH Data Acq Peripheral
ML2200D	12 + Sign	±1	8.5kHz, ±2.5V SINE, S/N 72dB	44	±5 (±5%)	X			40-Pin DIP	4-CH Data Acq Peripheral
ML2208B	12 + Sign	±3/4	12kHz, ±2.5V SINE, S/N 72dB	31.5	±5 (±5%)	X			40-Pin DIP	8-CH Data Acq Peripheral
ML2208C	12 + Sign	±1	12kHz, ±2.5V SINE, S/N 72dB	31.5	±5 (±5%)	X			40-Pin DIP	8-CH Data Acq Peripheral
ML2208D	12 + Sign	±1	8.5kHz, ±2.5V SINE, S/N 72dB	44	±5 (±5%)	X			40-Pin DIP	8-CH Data Acq Peripheral
ML2221B*	12 + Sign	±3/4	8.5kHz, ±5.0V SINE, S/N 72dB	44	±5 (±5%)	X	X		16-Pin DIP, 20-Pin PCC	Serial, S.P.I.
ML2221C*	12 + Sign	±1	8.5kHz, ±5.0V SINE, S/N 72dB	44	±5 (±5%)	X	X		16-Pin DIP, 20-Pin PCC	Serial, S.P.I.
ML2222B*	12 + Sign	±3/4	12kHz, ±2.5V SINE, S/N 72dB	35	±5 (±5%)	X	X		16-Pin DIP, 20-Pin PCC	Serial, CODEC
ML2222C*	12 + Sign	±1	12kHz, ±2.5V SINE, S/N 72dB	35	±5 (±5%)	X	X		16-Pin DIP, 20-Pin PCC	Serial, CODEC

* Future Products

Note 1. Temperature Range:
C = 0°C to +70°C, I = -40°C to +85°C, M = -55°C to +125°C

Part Number	Resolution (Bits)	Non Linearity (Max LSB)	Dynamic Performance Signal to Noise Ratio	Conversion Time (μs)	Power Supplies (V)	Temperature Range[1] C	I	M	Package	Comments
ML2223B*	12 + Sign	±3/4	8.5kHz, ±5.0V SINE, S/N 72dB	44	±5 (±5%)	X	X		16-Pin DIP, 20-Pin PCC	Serial, ASYNC
ML2223C*	12 + Sign	±1	8.5kHz, ±5.0V SINE, S/N 72dB	44	±5 (±5%)	X	X		16-Pin DIP, 20-Pin PCC	Serial, ASYNC
ML2230B	12 + Sign	±3/4	12kHz, ±2.5V SINE, S/N 72dB	31.5	±5 (±5%)	X			24-Pin DIP,	μP Comp, 8-Bit Bus
ML2230C	12 + Sign	±1	12kHz, ±2.5V SINE, S/N 72dB	31.5	±5 (±5%)	X			24-Pin DIP,	μP Comp, 8-Bit Bus
ML2230D	12 + Sign	±1	8.5kHz, ±2.5V SINE, S/N 72dB	44	±5 (±5%)	X			24-Pin DIP,	μP Comp, 8-Bit Bus
ML2233B	12 + Sign	±3/4	12kHz, ±2.5V SINE, S/N 72dB	31.5	±5 (±5%)	X			28-Pin DIP,	μP Comp, 16-Bit Bus
ML2233C	12 + Sign	±1	12kHz, ±2.5V SINE, S/N 72dB	31.5	±5 (±5%)	X			28-Pin DIP,	μP Comp, 16-Bit Bus
ML2233D	12 + Sign	±1	8.5kHz, ±2.5V SINE, S/N 72dB	44	±5 (±5%)	X			28-Pin DIP,	μP Comp, 16-Bit Bus
ML2252B	8	±1/2	51kHz, 5V SINE, S/N 47dB	6.6	5 (±10%)	X	X	X	20-Pin DIP, 20-Pin PCC	μP Comp, 2-CH
ML2252C	8	±1	51kHz, 5V SINE, S/N 47dB	6.6	5 (±10%)	X	X	X	20-Pin DIP, 20-Pin PCC	μP Comp, 2-CH
ML2258B	8	±1/2	51kHz, 5V SINE, S/N 47dB	6.6	5 (±10%)	X	X	X	20-Pin DIP, 20-Pin PCC	μP Comp, 8-CH
ML2258C	8	±1	51kHz, 5V SINE, S/N 47dB	6.6	5 (±10%)	X	X	X	20-Pin DIP, 20-Pin PCC	μP Comp, 8-CH
ML2259B	8	±1/2	51kHz, 5V SINE, S/N 47dB	6.6	5 (±10%)	X	X	X	28-Pin DIP, 28-Pin PCC	μP Comp, 8-CH
ML2259C	8	±1	51kHz, 5V SINE, S/N 47dB	6.6	5 (±10%)	X	X	X	28-Pin DIP, 28-Pin PCC	μP Comp, 8-CH
ML2261B	8	±1/2	250kHz, 5V SINE, S/N 48dB	.67	5 (±5%)	X	X	X	20-Pin DIP, 20-Pin PCC	μP Comp, RD/WR
ML2261C	8	±1	250kHz, 5V SINE, S/N 48dB	.67	5 (±5%)	X	X	X	20-Pin DIP, 20-Pin PCC	μP Comp, RD/WR
ML2264B	8	±1/2	250kHz, 5V SINE, S/N 48dB	.68	5 (±5%)	X	X	X	24-Pin DIP, 24-Pin SOIC	μP Comp, RD/WR, 4-CH Mux
ML2264C	8	±1	250kHz, 5V SINE, S/N 48dB	.68	5 (±5%)	X	X	X	24-Pin DIP, 24-Pin SOIC	μP Comp, RD/WR, 4-CH Mux
ML2271B*	10	±1/2	150kHz, 5V SINE, S/N 60dB	1.5	5 (±5%)	X	X	X	20-Pin DIP, 20-Pin SOIC	μP Comp, RD/WR
ML2271C*	10	±1	150kHz, 5V SINE, S/N 60dB	1.5	5 (±5%)	X	X	X	20-Pin DIP, 20-Pin SOIC	μP Comp, RD/WR
ML2280B	8	±1/2	51kHz, 5V SINE, S/N 47dB	6.6	5 (±10%)	X	X	X	8-Pin DIP	Serial I/O, Single CH
ML2280C	8	±1	51kHz, 5V SINE, S/N 47dB	6.6	5 (±10%)	X	X	X	8-Pin DIP	Serial I/O, Single CH
ML2281B	8	±1/2	51kHz, 5V SINE, S/N 47dB	6.6	5 (±10%)	X	X	X	8-Pin DIP	Serial I/O, Single CH
ML2281C	8	±1	51kHz, 5V SINE, S/N 47dB	6.6	5 (±10%)	X	X	X	8-Pin DIP	Serial I/O, Single CH
ML2282B	8	±1/2	47.5kHz, 5V SINE, S/N 47dB	6.6	5 (±10%)	X	X	X	8-Pin DIP	Serial I/O, 2-CH
ML2282C	8	±1	47.5kHz, 5V SINE, S/N 47dB	6.6	5 (±10%)	X	X	X	8-Pin DIP	Serial I/O, 2-CH

* Future Products

Note 1. Temperature Range:
C = 0°C to +70°C, I = –40°C to +85°C, M = –55°C to +125°C

Part Number	Resolution (Bits)	Non Linearity (Max LSB)	Dynamic Performance Signal to Noise Ratio	Conversion Time (μs)	Power Supplies (V)	Temperature Range[1] C	I	M	Package	Comments
ML2283B	8	±1/2	36.5kHz, 5V SINE, S/N 47dB	6.6	5 (±10%)	X	X	X	14-Pin DIP	Serial I/O, 4-CH
ML2283C	8	±1	36.5kHz, 5V SINE, S/N 47dB	6.6	5 (±10%)	X	X	X	14-Pin DIP	Serial I/O, 4-CH
ML2284B	8	±1/2	39kHz, 5V SINE, S/N 47dB	6.6	5 (±10%)	X	X	X	14-Pin DIP	Serial I/O, 4-CH
ML2284C	8	±1	39kHz, 5V SINE, S/N 47dB	6.6	5 (±10%)	X	X	X	14-Pin DIP	Serial I/O, 4-CH
ML2288B	8	±1/2	36.5kHz, 5V SINE, S/N 47dB	6.6	5 (±10%)	X	X	X	20-Pin DIP, 20-Pin PCC	Serial I/O, 8-CH
ML2288C	8	±1	36.5kHz, 5V SINE, S/N 47dB	6.6	5 (±10%)	X	X	X	20-Pin DIP, 20-Pin PCC	Serial I/O, 8-CH

* Future Products

Note 1. Temperature Range:
C = 0°C to +70°C, I = –40°C to +85°C, M = –55°C to +125°C

Selection Guide

Part Number	Resolution (Bits)	Non Linearity (Max LSB)	Settling Time (μs Max)	Power Supplies (V)	Reference (V)	Output Voltage (V)	Temperature Range C	I	M	Package	Comments
ML2340B	8 (11-bits with gain ranging)	±¼	5	Single 5 or 12, dual ±5	2.25 or 4.50	Rail-to-rail, bipolar, unipolar	X	X	X	18-pin DIP 18-pin SOIC	Flow through, or single buffered data
ML2340C	8 (11-bits with gain ranging)	±½	5	Single 5 or 12, dual ±5	2.25 or 4.50	Rail-to-rail, bipolar, unipolar	X	X	X	18-pin DIP 18-pin SOIC	Flow through, or single buffered data
ML2341B	8 (11-bits with gain ranging)	±¼	5	Single 5 or 12, dual ±5	2.25 or 4.50	Rail-to-rail, bipolar, unipolar	X	X	X	20-pin DIP 20-pin PCC	Double or single buffered data
ML2341C	8 (11-bits with gain ranging)	±½	5	Single 5 or 12, dual ±5	2.25 or 4.50	Rail-to-rail, bipolar, unipolar	X	X	X	20-pin DIP 20-pin PCC	Double or single buffered data
ML2350B	8 (11-bits with gain ranging)	±¼	5	Single 5 or 12, dual ±5	2.50 or 5.00	Rail-to-rail, bipolar, unipolar	X	X	X	18-pin DIP 18-pin SOIC	Flow through, or single buffered data
ML2350C	8 (11-bits with gain ranging)	±½	5	Single 5 or 12, dual ±5	2.50 or 5.00	Rail-to-rail, bipolar, unipolar	X	X	X	18-pin DIP 18-pin SOIC	Flow through, or single buffered data
ML2351B	8 (11-bits with gain ranging)	±¼	5	Single 5 or 12, dual ±5	2.50 or 5.00	Rail-to-rail, bipolar, unipolar	X	X	X	20-pin DIP 20-pin PCC	Double or single buffered data
ML2351C	8 (11-bits with gain ranging)	±½	5	Single 5 or 12, dual ±5	2.50 or 5.00	Rail-to-rail, bipolar, unipolar	X	X	X	20-pin DIP 20-pin PCC	Double or single buffered data

* Future Products

Note 1. Temperature Range:
C = 0°C to +70°C, I = –40°C to +85°C, M = –55°C to +125°C

Micro Linear

ML2200, ML2208

12-Bit Plus Sign Data Acquisition Peripheral

GENERAL DESCRIPTION

The ML2200 and ML2208 Data Acquisition Peripherals (DAP) are monolithic CMOS data acquisition subsystems. These data acquisition peripherals feature an input multiplexer, a programmable gain instrumentation amplifier, a 2.5V bandgap reference, and a 12-bit plus sign A/D converter with built-in sample-and-hold. In addition to a general purpose 8-bit microprocessor interface, the ML2200 and ML2208 include a programmable processor, data buffering, a 16-bit timer, and limit alarms.

The ML2200B and ML2208B self-calibrating algorithmic A/D converters have a maximum non-linearity error over temperature of 0.018% of full-scale, while the ML2200C, ML2200D, ML2208C, and ML2208D have a maximum non-linearity error over temperature of 0.024%.

The ML2200 has a four channel differential input multiplexer and the ML2208 has an eight channel single ended input multiplexer.

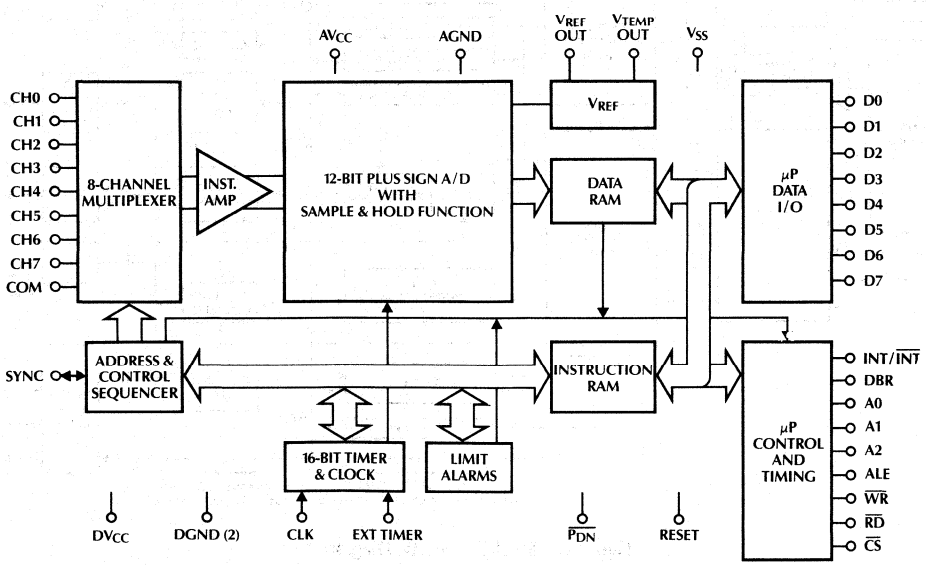
The digital interface, with software-alterable configurations, is designed to off-load the microprocessor. Control of the DAP is autonomously handled through the control sequencer which receives its instructions from the instruction RAM.

FEATURES

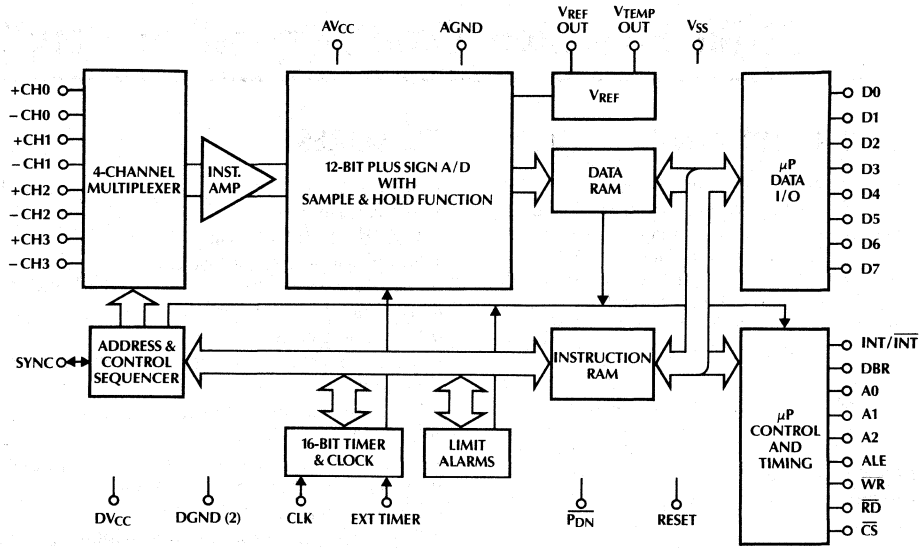
- Resolution 12 bits + sign
- Conversion time (including S/H acquisition) 31.5μs max
- Sample-and-hold acquisition 2.3μs max
- Non-linearity error ±¾LSB and ±1LSB max
- Low harmonic distortion 0.01%
- No missing codes
- Self-calibrating — maintains accuracy over time and temperature
- Inputs withstand |7V| beyond supplies
- Internal voltage reference 2.5V ±2%
- Four differential or eight single-ended input channels
- Data buffering (8 word data RAM)
- Programmable limit alarm
- 8-Bit microprocessor interface — interrupt, DMA, or polling
- 16-Bit timer for programmable conversion rates
- Standard hermetic 40-pin DIP

2

ML2208 BLOCK DIAGRAM



ML2200 BLOCK DIAGRAM



BLOCK SCHEMATIC DIAGRAM

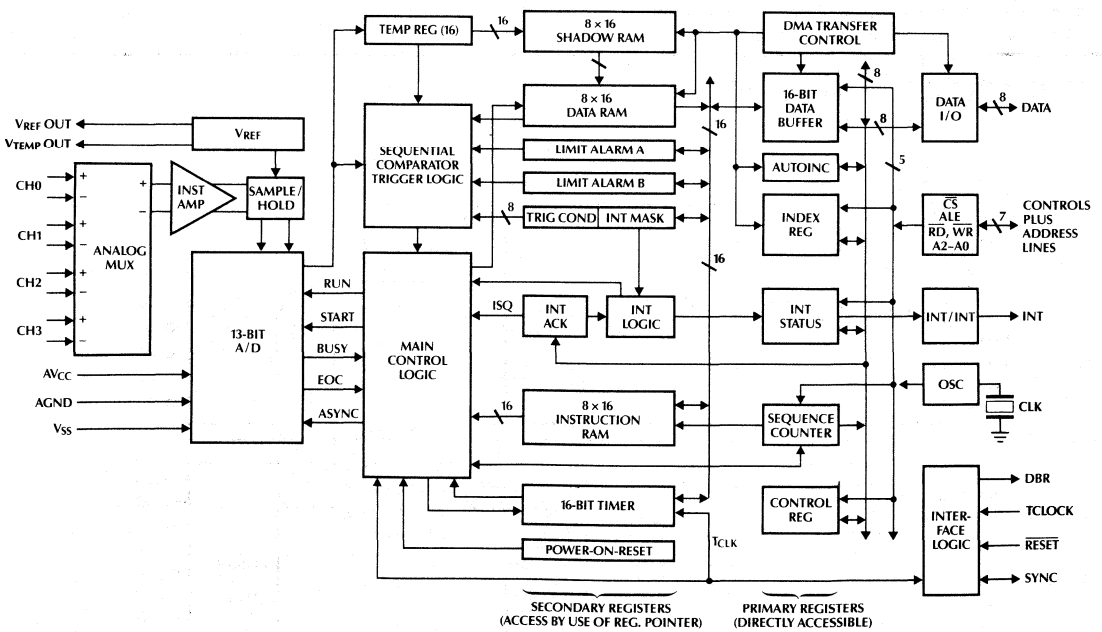


Figure 1. Block Schematic Diagram

PIN DESCRIPTIONS

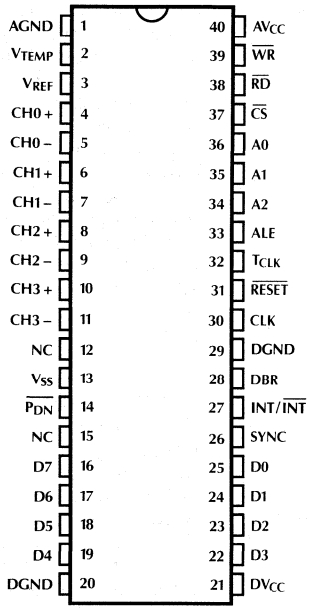
PIN NO.	NAME	FUNCTION
1	AGND	Analog Ground.
2	V_{TEMP}	Voltage output proportional to the die temperature.
3	V_{REF}	Internal voltage reference output
4-11	CH	Analog Inputs. ML2200 — Positive or negative input of four differential inputs ML2208 — Eight single ended inputs referenced to common pin. Digitally selected by control sequencer.
12	NC COM	ML2200 — No connection. ML2208 — Negative common input for the eight input channels. Tie to analog ground or (V_{SS} +2.5) to (AV_{CC} − 2.5 V)
13	V_{SS}	Negative power supply; decouple to AGND.
14	$\overline{P_{DN}}$	Power-Down Input. When $\overline{P_{DN}}$ = 0, device in power-down mode with register contents retained if AV_{CC} > 2.0 V.
15	NC	No Connection.
16-19	D7, D6, D5, D4	Bidirectional data bits.
20	DGND	Digital Ground.
21	DV_{CC}	Digital power supply. Tie to AV_{CC} from same power supply.
22-25	D3, D2, D1, D0	Bidirectional data bits.
26	SYNC	In the slave mode, SYNC is a positive edge triggered input used to start a conversion. In master mode, SYNC is an output and indicates a conversion has occurred.
27	INT	Interrupt output. A maskable interrupt programmable to be active high or low or will default to active high. INT will not clear until acknowledged in halt mode; not affected by the run or halt state. INT = 0 during reset and inactive during P_{DN}.
28	DBR	Data Buffer Ready output active high indicates that a sequence of operations has completed and data is ready to transfer. DBR is not maskable. It can be used to generate an interrupt in addition to the INT pin when the DBRIE bit in the interrupt mask register has not been enabled. DBR is the DMA request pin when DMA mode is enabled. DBR is not active unless in run mode and at least one sequence of operations has been completed. DBR remains active in the halt mode if not acknowledged; low during reset time and power-down.
29	DGND	Digital Ground.
30	CLK	Clock input. Drive with an external clock or crystal reference to DGND. The crystal must be parallel resonant with minimum capacitive loading (i.e., No bypass caps should be used and leads should be kept short).
31	$\overline{RESET}$	Active low hardware reset with internal pull up resistor of 200 K. Tie to system reset line or to grounded capacitor. The capacitor size (usually > 6 μF) is based on the time the power supplies stabilize, to the time reset voltage reaches 1.4 V (> 400 ms).
32	T_{CLK}	External timer, T_{CLK} is used as external clock input for the 16-bit timer when the T_{CLK} bit in the control register is set to one.
33	ALE	Address latch enable, active low latches information on A0, A1, A2 and $\overline{CS}$. Tie to AV_{CC} to disable use when separate address and data bus are used.
34	A2	Address 2
35	A1	Address 1
36	A0	Address 0
37	$\overline{CS}$	Chip select, active low
38	$\overline{RD}$	Read, active low enables ML2200 or ML2208 to drive data bus.
39	$\overline{WR}$	Write, active low allows writing into the registers.
40	A V_{CC}	Positive analog Power supply. Decouple to AGND. Tie to DV_{CC} from same power supply

2

PIN CONNECTIONS

ML2200

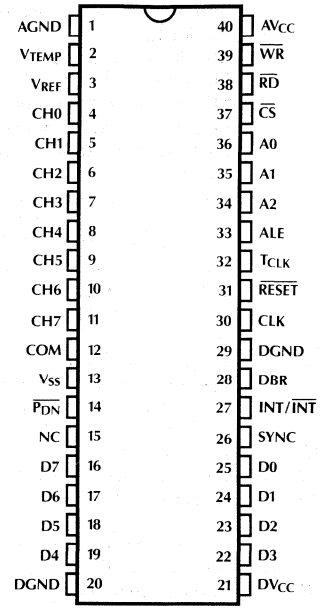
40-PIN DIP



TOP VIEW

ML2208

40-PIN DIP



TOP VIEW

ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltages (AV_{CC} and DV_{CC}) 6.0V
Negative Supply Voltage (V_{SS}) ..... −6.0V
Voltage at Analog Inputs ..... V_{SS} − 7V to AV_{CC} +7V
Voltage at V_{REF} ..... V_{SS} − 7V to AV_{CC} +7V
Input Current per Digital Pin ..... ±10mA
Input Current at Analog Inputs ..... ±20mA
Storage Temperature Range ..... −65°C to +150°C
Package Dissipation @ 25°C 1W
Lead Temperature (Soldering 10 sec.)
Dual-In-Line Package (Ceramic) ..... 300°C

OPERATING CONDITIONS

(Note 2)

Temperature Range ..... $T_{MIN} \leq T_A \leq T_{MAX}$
ML2200BCJ, ML2200CCJ, ML2200DCJ ..... 0°C to 70°C
ML2208BCJ, ML2208CCJ, ML2208DCJ ..... 0°C to 70°C
Supply Voltage (AV_{CC} and DV_{CC}) ..... $4.5V_{DC}$ to $6.0V_{DC}$
Negative Supply Voltage (V_{SS}) ..... $-4.5V_{DC}$ to $-6.0V_{DC}$

ELECTRICAL CHARACTERISTICS

The following specifications apply for AV_{CC} = DV_{CC} = +5V ± 5%, V_{SS} = -5V ± 5%, AGND = DGND = COM = CHX- = 0V, T_A = T_{MIN} to T_{MAX} unless otherwise specified. C_L = 100pF for D0–D7, C_L = 50pF for INT, DBR, and SYNC.

SYMBOL	PARAMETER	NOTES	CONDITIONS	MIN	TYP NOTE 3	MAX	UNITS
Converter Characteristics							
	Linearity Error						
	ML2200BCJ, ML2208BCJ	4	f_{CCLK} = 0.1 ≤ 7MHz			±¾	LSB
	ML2200CCJ, ML2208CCJ		f_{CCLK} = 0.1 ≤ 7MHz			±1	LSB
	ML2200DCJ, ML2208DCJ		f_{CCLK} = 0.1 ≤ 5MHz			±1	LSB
	Unadjusted Zero Error						
	ML2200BCJ, ML2208BCJ	4				±¾	LSB
	ML2200CCJ, ML2208CCJ					±2	LSB
	ML2200DCJ, ML2208DCJ					±2	LSB
	Unadjusted Positive and Negative Full Scale Error	5				±4	LSB
	Zero Error Temperature Coefficient				0.5		ppm/°C
	Gain Temperature Coefficient		External Reference		3		ppm/°C
	Common-Mode Rejection	13			80		dB
	Analog Input Range	5	All Analog Inputs	V_{SS}-0.05		AV_{CC}+0.05	V
	External Source Resistance	5	Channel = Analog Input			2	kΩ
	for Analog Inputs	5	Channel = Voltage Reference			0.5	kΩ
	Differential Analog Input Range	4	CHX referred to COM for ML2208 CHX+ referred to CHX- for ML2200	$-V_{REF}$		$+V_{REF}$	V
	Off Channel Leakage Current	5, 6	On Chan = 2.5V, Off Chan = -2.5V	-100			nA
			On Chan = -2.5V Off Chan = 2.5V			+100	
	On Channel Leakage Current	5, 6	On Chan = -2.5V, Off Chan = 2.5V	-100			nA
			On Chan = 2.5V Off Chan = -2.5V			+100	
	Gain Error		Gain = 2, 4, or 8		0.03		%
Voltage Reference and V_{TEMP} Characteristics							
	V_{REF} Absolute Value	4	Referred to AGND	2.45		2.55	V
	V_{REF} Output Pin						
	Output Resistance	5				300	mΩ
	Minimum Load Resistance	5		1			kΩ
	Maximum Load Resistance	5				50	pF
	Temperature Coefficient				50		ppm/°C
	Line Regulation		4.75 ≤ AV_{CC} ≤ 5.25		1		mV
			-4.75 ≥ V_{SS} ≥ -5.25		1		mV
	Load Regulation		1µA - 2.5mA		1		mV
	Output Noise				100		μV_{RMS}
	V_{TEMP} Output Pin				AV_{CC}-1.5		V
	Absolute Value @ 25°C						
	Volts per °C				5		mV/°C

2

ELECTRICAL CHARACTERISTICS (Continued)

The following specifications apply for AV_{CC} = DV_{CC} = +5V ± 5%, V_{SS} = –5V ± 5%, AGND = DGND = COM = CHX– = 0V, T_A = T_{MIN} to T_{MAX} unless otherwise specified. C_L = 100pF for D0–D7, C_L = 50pF for INT, DBR, and SYNC.

SYMBOL	PARAMETER	NOTES	CONDITIONS	MIN	TYP NOTE 3	MAX	UNITS
DC Characteristics							
	Power Supply Current						
	AI_{CC}, Analog AV_{CC}	4			30	50	mA
	DI_{CC}, Digital DV_{CC}	12	$\overline{RD}$ = $\overline{CS}$ = V_{IH}		10		µA
	I_{SS}, V_{SS}	4			18	30	mA
I_{CC}	Standby Current AV_{CC} + DV_{CC}	4, 9	$\overline{P_{DN}}$ pin = GND		10	1000	µA
I_{SS}	Standby Current				10	1000	µA
	V_{CCPD} Minimum AV_{CC} and DV_{CC} for power-down data retention		$\overline{P_{DN}}$ pin = GND V_{SS} = –5.25 to GND	2			V
	Power Supply Rejection	7					
	AV_{CC}/DV_{CC}		DC		80		dB
			DC to 25kHz, 200mV_{P-P}		50		dB
	V_{SS}		DC		80		dB
			DC to 25kHz, 200mV_{P-P}		50		dB
V_{IL}	Input Low Voltage (except CLK, t_{CLK})	4				0.8	V
V_{IL1}	Input Low Voltage (CLK, t_{CLK})	4				0.8	V
V_{IH}	Input High Voltage (except CLK, t_{CLK})	4		2.0			V
V_{IH1}	Input High Voltage (CLK, t_{CLK})	4		3.5			V
V_{OL}	Output Low Voltage	4	I_{OL} = 2.0mA			0.45	V
V_{OH}	Output High Voltage	5	I_{OH} = –1mA	4.0			V
I_L	Input Leakage Current (except CLK and RESET)	4	GND < V_{IN} < V_{CC}			±10	µA
I_{L1}	Input Leakage Curent (CLK)	4	GND < V_{IN} < V_{CC}			±200	µA
I_{L0}	Output Leakage Curent (D0–D7)	4	$\overline{RD}$ = $\overline{CS}$ = V_{IH}			±10	µA
I_{RST}	RESET Pin Source Current	4	$\overline{RESET}$ = 0V	15	50	100	µA
C_I	Input Capacitance (All Digital Inputs)				10		pF
C_O	Output Capacitance (All Outputs and D0–D7)				20		pF
AC Electrical Characteristics (Note 8)							
t_C	Conversion Time	4, 9	CLK Mode = 0, f_{CLK} = 7.0MHz	31.5			µs
			CLK Mode = 0, f_{CLK} = 5.0MHz	44.0			µs
	Sample and Hold Acquisition	4, 9	CLK Mode = 0, f_{CLK} = 7.0MHz			2.3	µs
			CLK Mode = 0, f_{CLK} = 5.0MHz			3.2	µs
SNR	Signal-to-Noise Ratio		V = 10kHz, 2.5V Sine. f_{CLK} = 7MHz ($f_{SAMPLING}$ = 31.8kHz). Noise is sum of all nonfundamental components up to ½ of $f_{SAMPLING}$.		73		dB
THD	Total Harmonic Distortion		V = 10kHz, 2.5V Sine. f_{CLK} = 7MHz ($f_{SAMPLING}$ = 31.8kHz). THD is sum of 2, 3, 4, 5 harmonics relative to fundamental.		–75		dB

ELECTRICAL CHARACTERISTICS (Continued)

The following specifications apply for AV_{CC} = DV_{CC} = +5V ± 5%, V_{SS} = –5V ± 5%, AGND = DGND = COM = CHX– = 0V, T_A = T_{MIN} to T_{MAX} unless otherwise specified. C_L = 100pF for D0–D7, C_L = 50pF for INT, DBR, and SYNC.

SYMBOL	PARAMETER	NOTES	CONDITIONS	MIN	TYP NOTE 3	MAX	UNITS
AC Electrical Characteristics (Note 8) (Continued)							
IMD	Intermodulation Distortion		V_{IN} = f_A + f_B. f_A = 9kHz, 1.25V sine. f_B = 10kHz, 1.25V sine. f_{CLK} = 7MHz ($f_{SAMPLING}$ = 31.8kHz). IMD is (f_A + f_B), (f_A – f_B), ($2f_A$ – f_B), ($2f_A$ – f_B), (f_A + $2f_B$), (f_A – $2f_B$) relative to fundamental.		–75		dB
FR	Frequency Response		V_{IN} = 0 to 10kHz, 2.5V sine relative to 1kHz		0.01		dB
f_{CLK}	CLK Frequency	4	(no crystal)	0.1		7	MHz
f_{CLKX}	CLK Frequency	4	(crystal)	3		7	MHz
f_{CLKI}	Internal CLK Frequency				1/2		f_{CLK} or f_{CLKX}
f_{CLKT}	CLK Frequency (t_{CLK} only)	4				f_{CLKI}	MHz
t_{CLKW}	Minimum Clock High/Low Width (CLK)	5		50			ns
t_{CLKWT}	Minimum Clock High/Low Width (t_{CLK})	5		75			ns
t_{RF}	Maximum Rise/Fall Times, All Inputs	5				25	ns
t_{RESET}	Minimum Reset Active Time	4, 10		10			f_{CLKI} Periods
t_{PDN}	Power-Up Time		Time After P_{DN} = V_{IH}		1		ms
Multiplexed Data Bus Timing							
t_{AL}	Address to ALE Setup Time	4		20			ns
t_{LA}	Address Hold Time After ALE	4		20			ns
t_{LC}	Latch to RD or WR Control	4		20			ns
t_{RD}	Valid Data Delay from Read	4				150	ns
t_{AD}	Address Stable to Valid Data	5		150			ns
t_{LL}	ALE Width	4		80			ns
t_{DF}	Data Bus Float After Read	4		10		50	ns
t_{CL}	Read or Write Control to ALE	4		20			ns
t_{CC}	Read or Write Control Width	4		150			ns
t_{DW}	Data Setup Time for Write	4		100			ns
t_{WD}	Data Hold Time for Write	4		0			ns
t_{RV}	Recovery Time Between Two Reads or Writes	4		250			ns
Non-Multiplexed Data Bus Timing							
t_{AD}	Address Stable to Valid Data	5		150			ns
t_{AR}	Address Stable Before Read	4		0			ns
t_{RA}	Address Hold Time for Read	4		0			ns
t_{RR}	Read Pulse Width	4		150			ns
t_{RD}	Data Delay from Read	4				150	ns
t_{DF}	Read to Data Float	4		10		50	ns

ELECTRICAL CHARACTERISTICS (Continued)

The following specifications apply for AV_{CC} = DV_{CC} = +5V ± 5%, V_{SS} = –5V ± 5%, AGND = DGND = COM = CHX– = 0V, T_A = T_{MIN} to T_{MAX} unless otherwise specified. C_L = 100pF for D0–D7, C_L = 50pF for INT, DBR, and SYNC.

SYMBOL	PARAMETER	NOTES	CONDITIONS	MIN	TYP NOTE 3	MAX	UNITS
Non-Multiplexed Data Bus Timing							
t_{RV}	Recovery Time Between Two Reads or Writes	4		250			ns
t_{AW}	Address Stable Before Write	4		0			ns
t_{WA}	Address Hold Time for Write	4		0			ns
t_{WW}	Write Pulse Width	4		150			ns
t_{DW}	Data Setup Time for Write	4		100			ns
t_{WD}	Data Hold Time for Write	4		0			ns
DMA Interrupt and SYNC Timings							
t_{CKDBR}	Clock to DBR Assert	11, 4	DMA		120	180	ns
t_{RDD}	Read to DBR Negation on Last Byte	4			110	160	ns
t_{CKDBR}	Clock to DBR or t_{CKINT}, INT Assert	11, 4	Non-DMA		100	180	ns
t_{WRDBR}	Write to DBR or t_{WRINT} INT Negation	11, 4			70	120	ns
t_{CKSYNC}	Clock to SYNC Delay	11, 4	Master Mode		150	200	ns
t_{SYNCN}	SYNC Input Width	5		3			f_{CLKI}
t_{SYNCCK}	SYNC to Clock Setup	4	Slave: Mode 4 Only	50			ns
t_{SYNCO}	Minimum SYNC Output Width	4		4		4	f_{CLKI}

Note 1: Absolute maximum ratings are limits beyond which the life of the integrated circuit may be impaired. All voltages unless otherwise specified are measured with respect to ground.

Note 2: 0°C to +70°C operating temperature range devices are 100% tested with temperature limits guaranteed by 100% testing, sampling, or by correlation with worst-case test conditions.

Note 3: Typicals are parametric norm at 25°C.

Note 4: Parameter guaranteed and 100% production tested.

Note 5: Parameter guaranteed. Parameters not 100% tested are not in outgoing quality level calculation.

Note 6: Leakage current is measured with the clock not switching.

Note 7: Power supply rejection is the ratio of the change in zero error to the change in power supply voltage.

Note 8: All parameters measured from 0.8V to 2.0V.

Note 9: Power-down current is with power-down pin at GND potential only. Any other level will dissipate more power. Other digital input pins may float but cannot be above V_{DD} or below GND.

Note 10: RESET should be held active for at least 10 internal clocks after power supplies have stabilized to within 5% of 5V.

Note 11: Since the internal master clock is the input clock divided by 2, this number can be either the maximum listed or the maximum listed plus ½ the input clock period.

Note 12: When RD = CS = V_{IL}, the current into the DV_{CC} pin depends on the load on the data bus pins D0–D7.

Note 13: Common-Mode rejection is the ratio of the change in zero error to the change in common-mode input voltage.

TIMING DIAGRAMS

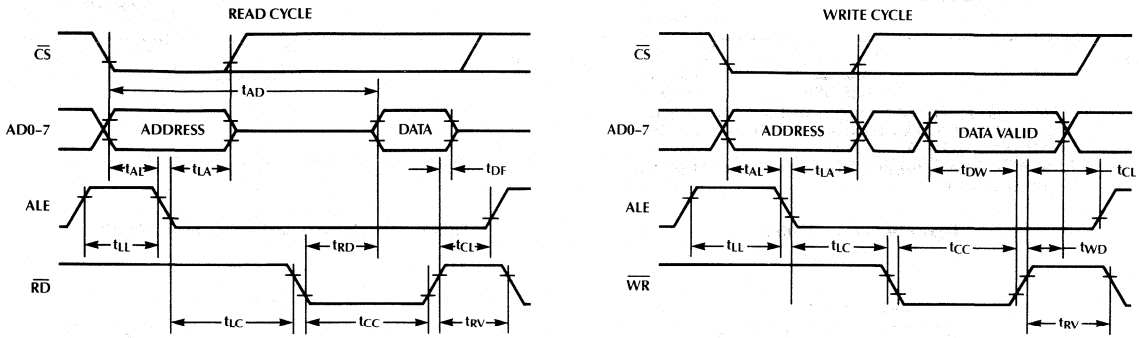


Figure 2. Multiplexed Bus

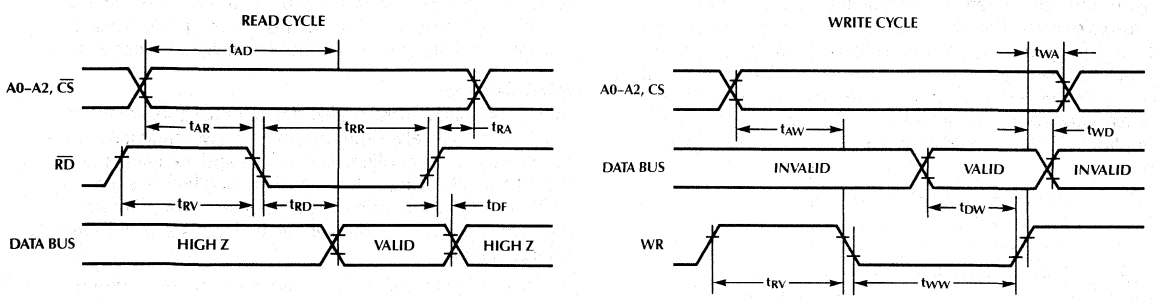
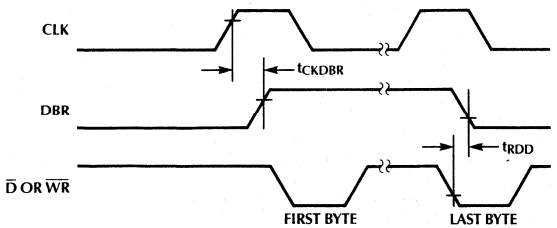


Figure 3. Non-Multiplexed Bus

TIMING DIAGRAMS (Continued)



THERE ARE 2*n READ OPERATIONS WHERE n IS THE NUMBER OF WORDS TO BE TRANSFERRED. DBR IS SET AND CLEARED BY INTERNAL CIRCUITRY.

NOTE: DMA BIT IN THE CONTROL REGISTER MUST BE SET FOR THIS OPERATION.

Figure 4. DMA Mode

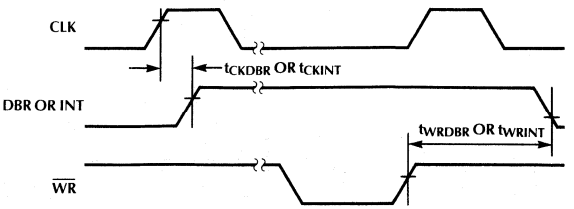


Figure 5. DBR and INT (Non-DMA Mode)

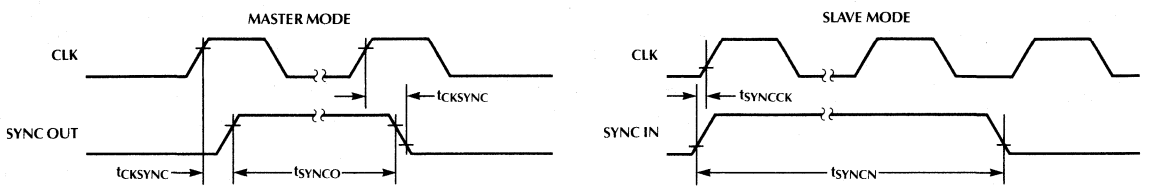


Figure 6. SYNC

1.0 FUNCTIONAL DESCRIPTION

1.1 Algorithmic A/D Converter

Micro Linear's algorithmic converter uses a successive approximation technique. Most of today's successive approximation converters use a DAC to feed back the approximated signal, however this technique requires more circuitry than algorithmic converters. In addition the values of all of the resistors or capacitors in the DAC must be matched to within the accuracy of the converter. This is difficult to do in silicon beyond 10 bits unless trimming is used. An algorithmic converter uses less circuitry and is more easily trimmed. Micro Linear's algorithmic converter is implemented using a 2× amplifier, a sample/hold amp, and a comparator as shown in Figure 7.

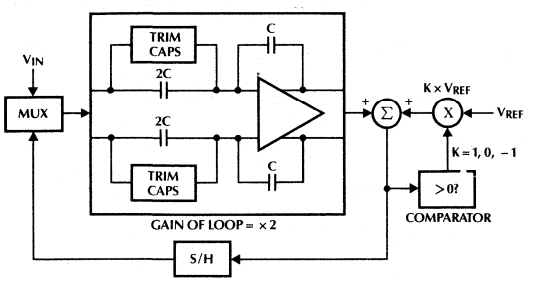


Figure 7. Self Calibrating A/D Converter

The input sample is first multiplied by two then compared to the reference voltage. If the 2× input voltage is greater than the reference, the MSB is a 1 and the reference voltage is subtracted from the 2× input voltage. The remainder is stored in the sample-and-hold. If the 2× input voltage is less than the reference, the MSB is a 0 and the 2× input voltage is stored in the sample-and-hold. This process repeats again, however now the sample-and-hold voltage is multiplied by 2.

Self-Calibration

In order to maintain integral and differential linearity to the 1/2 LSB level in an algorithmic converter, two critical parameters need to be controlled, loop offsets and the gain of the loop. Loop offsets are automatically nulled before each conversion using auto-zeroing circuitry on both the sampling amp and the 2× amp. The gain of the loop is adjusted using self-calibration.

Self-calibrating the algorithmic converter, once the offsets have been nulled, is performed by measuring the 2× gain of the loop and adjusting it. The gain can be measured by converting the reference voltage as the input as well as the reference (V_{REF}/V_{REF}), and examining the output code. Converting V_{REF} should yield plus full-scale, since V_{REF}/V_{REF} should equal 1. If the gain of the loop is slightly less than 2, the resulting LSB of the conversion will be "0". If the magnitude bits of the resulting conversion are all "1s", the gain may

be too great, therefore the gain is reduced to the point where the threshold of the LSB is reached.

Adjustment of the 2× gain is done with the binary weighted trim capacitor arrays connected to each of the 2C input capacitors. A small value of capacitance is either added to or subtracted from the 2C input caps until the gain of the loop is within 13-bit accuracy of 2.

1.2 Multiplexer Input

The input voltage is ±2.5V relative to COM of the ML2208 or a CH− of the ML2200. The input voltages under normal operation must not exceed supply voltages by 0.05V. Each channel is selected by the programmable sequencer.

1.3 Internal Voltage Reference and V_{TEMP}

The internal bandgap voltage reference with a temperature coefficient of 50ppm/°C has an external use current of 2.5mA.

The voltage reference V_{TEMP} output is directly proportional to the chip temperature.

1.4 Conversion Times

The following table lists the conversion times which include the sample-and-hold acquisition time. For a CALRD and CALWR no A/D conversion actually takes place.

Operation	Number of Internal Clocks*
8-bit A/D	80
13-bit A/D	110
CALWR	52
CALRD	80

*Internal clock is the external clock divided by two.

1.5 Sample-and-Hold Timing

Figure 8 shows the internal timing for the sample-and-hold circuitry. The relationship between the "Start of Conversion" and the input channel going into sample mode is fixed at 6 internal clocks, regardless of the Start Mode. Six internal clocks after the Start of Conversion, the Sample-and-Hold is switched into the sample mode, placing two 9pF capacitors in parallel with the input pins; one on CH+ and one on CH− for the ML2200, and CH and COM for the ML2208. The sample switch is kept in the sample mode for 8 internal clocks (2.3μs at a 7MHz external clock), then placed in the hold mode. During the next 2 internal clocks the charge on the sample-and-hold is transferred into the A/D, after which the V_{REF} pin is sampled for 8 internal clocks.

Figure 8 also illustrates the timing of the SYNC pin in Master Mode during a conversion. SYNC is activated one internal clock cycle before the Start of Conversion and lasts for four internal clocks.

1.6 Analog Inputs

Differential Inputs and Common-Mode Rejection

The differential inputs of the ML2200 eliminate the effects of common-mode input noise (60Hz, for example), as CH+ and CH− are sampled at the same time.

Noise

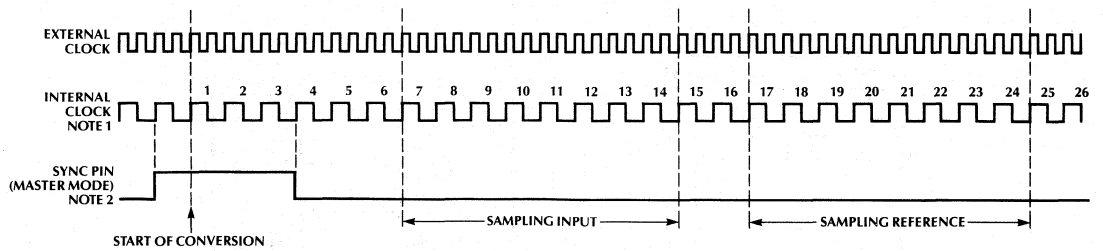
The leads to the analog inputs should be kept as short as possible to minimize output noise. Noise as well as digital clocks can couple into the inputs and cause errors. Input filters can be used to reduce the effects of these sources.

Power Supply Decoupling

Low inductance tantalum capacitors of 1μF or greater and 0.01μF disc ceramic capacitors are recommended for bypassing AV_{CC} as well as V_{SS} to AGND. These capacitors should be placed close to the AV_{CC} and V_{SS} pins.

2.0 μP HARDWARE INTERFACE

The microprocessor interface is a byte-oriented structure which occupies eight memory or I/O locations in the microprocessor's address space. Each register is readable and writable via the chip select, read and write pins, three address lines, and 8-bit data bus.



NOTE:
1. EXTERNAL CLOCK IN PHASE WITH INTERNAL CLOCK USING RESET.
2. IMMEDIATE EXECUTE MODE WHERE START OF CONVERSION AND START OF OPERATION OCCUR AT THE SAME TIME.

Figure 8. Sample-and-Hold Timing

Interfaces are shown for multiplexed address data bus in Figure 9 and Figure 10. When non-multiplexed interfaces are used, ALE can be tied high. All internal address and chip select latches are transparent.

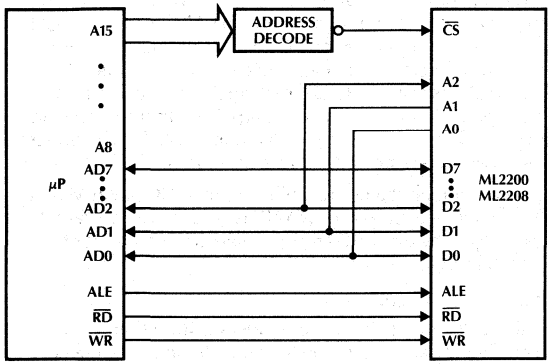


Figure 9. 8-Bit Multiplexed Bus Interface

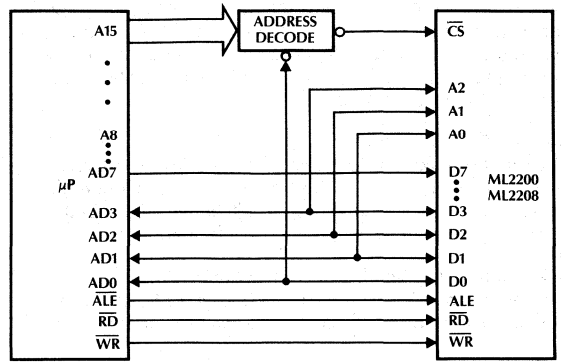


Figure 10. 16-Bit Multiplexed Bus Interface

2.1 Interrupts

The ML2200 and ML2208 provide two interrupt pins, one for control/status interrupts (INT), and one for data interrupts (DBR). The standard INT pin is maskable via an interrupt mask register while the DBR pin is always enabled to signify that data is available. DBR can be mapped into the INT pin if only one interrupt pin is desired.

The interrupt pin (INT) can be programmed, via the Interrupt Bit Mask register, to be active high, or active low. When programmed for active high, it is driven in both directions. When INT is programmed for active low, it is an open drain output, therefore an external pull-up resistor of 2.5 kΩ or more should be used. The DAP's Status register can be read to determine whether its interrupt is active or not.

2.2 DMA

The separate DBR pin can also serve as a DMA request signal when DMA operation is enabled in the Control register. DBR goes active high when the data buffer is full and ready to be read. DBR remains high until the last byte in the data buffer has been read. This allows back-to-back DMA cycles or single cycle transfers depending on how the DMA controller is programmed. The data for the DMA cycle is transferred over the 8-bit data bus at address 0 (A0-A2 = 0). The ML2200 or ML2208 automatically places both high and low bytes of the 16-bit wide data buffer at address 0 or 1 for the DMA controller to read. The LOBYT bit in the Control register specifies whether the high or low byte is placed on the bus first. Figure 11 shows a block diagram interfacing to the 8237 DMA controller.

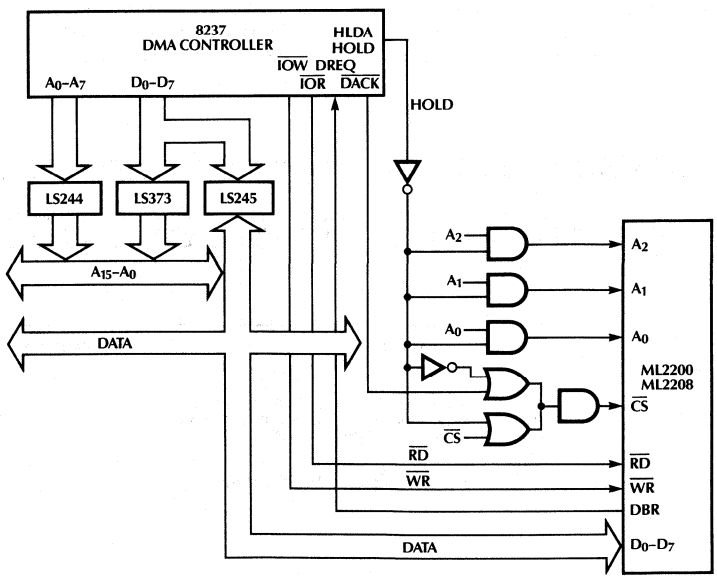


Figure 11. DMA Interface

3.0 REGISTER DEFINITIONS

These data acquisition peripherals contain six directly addressable 8-bit registers, and twenty indirectly addressable 16-bit registers. Figure 12 illustrates the register architecture while Figures 13, 14 & 15 illustrate the bit maps and addresses. The first three primary registers (Window Low, Window High, and Index) are used to access the 20 secondary registers. Window Low and Window High provide read/write access to the low and high bytes of the secondary register pointed to by Index.

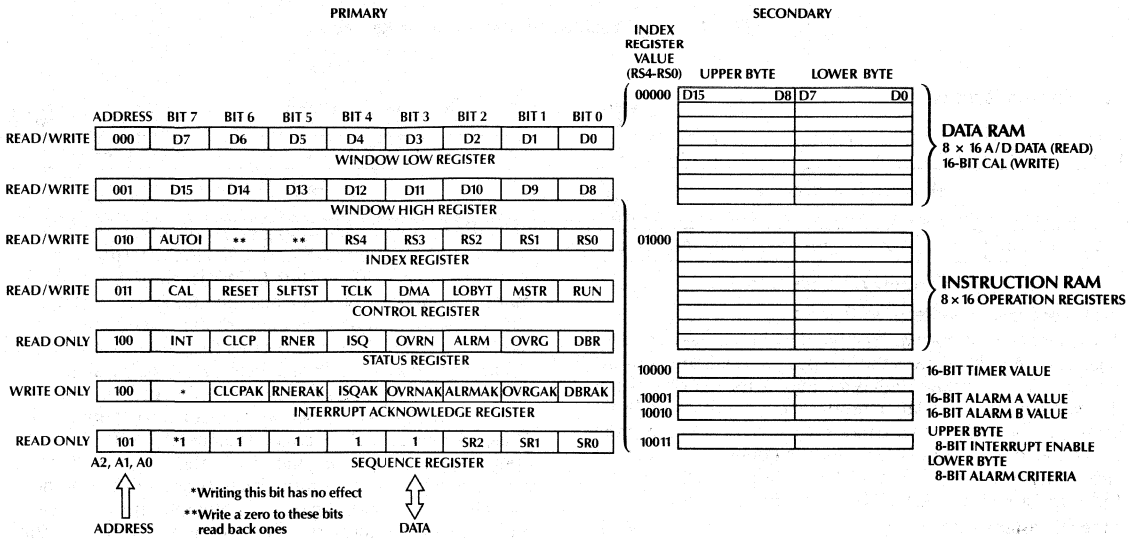


Figure 12. Register Architecture

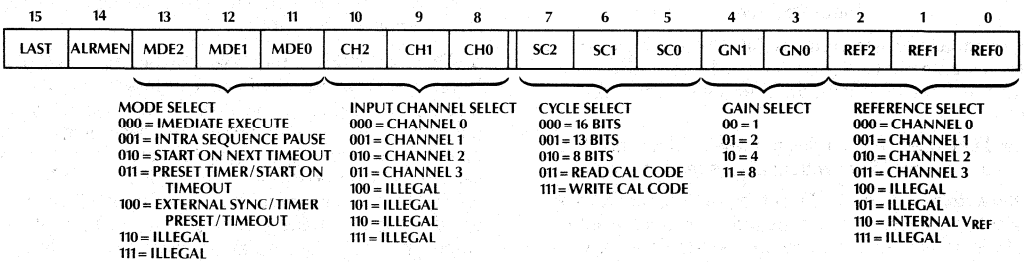


Figure 13. ML2200 Bit Map of Instruction RAM

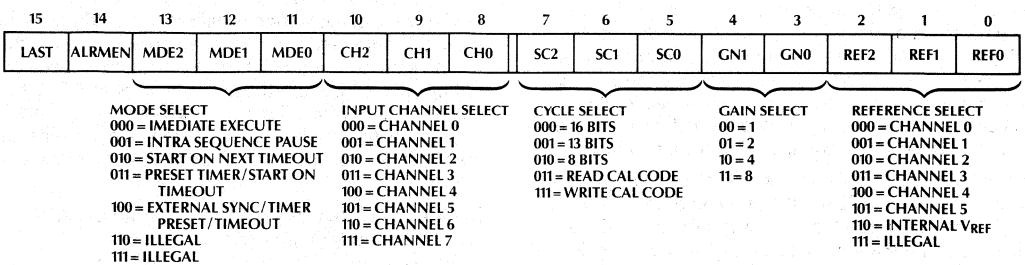


Figure 14. ML2208 Bit Map of Instruction RAM

SECONDARY REGISTER 19 RS4–RS0 = 10011

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTL	CLC PIE	RNERIE	ISQIE	OVRNIE	ALRMIE	OVRGIE	DBRIE				EN B	EN A	AND/OR	>B/<B	>A/<A
INTERRUPT ENABLE REGISTER								ALARM CRITERIA REGISTER							

Figure 15. Interrupt Enable and Alarm Criteria Registers

3.1 Primary Registers

D7	D6	D5	D4	D3	D2	D1	D0
							READ/WRITE

Window Low Register

D15	D14	D13	D12	D11	D10	D9	D8
							READ/WRITE

Window High Register

Window Registers — Registers 0 and 1

These registers form a two-byte window into the secondary registers. Window Low is the low byte of the secondary 16-bit word, and Window High is the high byte. Any one of the 20 words in the secondary register set can be accessed by first setting a 5-bit address in the Index register, then reading from or writing to the Window registers. Sequential access of the secondary registers is also available without writing to the Index register via the AUTOI bit in the Index register.

Index Register — Register 2

AUTOI			RS4	RS3	RS2	RS1	RS0
							READ/WRITE

Index Register

RSX = Secondary Register Address (Bits 0 to 4): The lower five bits of this register (RSO–RS4) define the location within the secondary register set that the window registers are positioned at.

Bits 5 and 6: Undefined. Writing to these bits have no effect, however a zero should be written; always read as ones.

AUTOI = autoincrement (Bit 7): Setting AUTOI signifies that the lower five addressing bits in the Index register are automatically incremented after either the Window Low or Window High register is accessed. Whether the auto-increment occurs when accessing Window Low or Window High register, is based on the LOBYT bit in the Control register.

Interrupt Operation Caution!!! - Using the auto-increment feature with interrupt driven software deserves special attention. A problem can arise when an interrupt service routine accessing the secondary registers, interrupts another routine accessing secondary registers. This problem can be avoided one of two ways: disable the interrupt in the main routine while accessing secondary registers, or reload the index register to its entry value when exiting the interrupt routine.

Note: The Index register is automatically cleared only under two conditions, one is a RESET, the other is when DMA mode is used. This register is reset to 0 in DMA mode just prior to the DMA request (DBR going active). DMA mode uses the index register for operation, so the index register should never be written to when RUN and DMA are set.

Control Register — Register 3

CAL	RESET	SLFTST	t_{CLK}	DMA	LOBYT	MSTR	RUN
							READ/WRITE

Control Register

RUN (Bit 0): Setting this bit to a one will cause the chip to start executing the operations defined in the Instruction RAM, beginning with location 0. This is referred to as the Run mode. Clearing this bit will place the ML2200 in the Halt mode. The run bit is initially cleared on power up or after a hardware or software reset. In order to properly start the chip operation, the RUN bit should be set after setting all other applicable bits in the control register. The act of halting the chip will always reset the sequence pointer to operation 0. Thus, the next time RUN is asserted, the chip starts from operation 0 again. Placing the chip in the Run or Halt mode has no effect on the Interrupt pins (INT and DBR), nor the status bits in the status register. It is recommended that secondary registers only be written to in the Halt mode. Writing to secondary registers in the Run mode will cause the RNER status bit to be set, indicating a run error. All of the status bits in the Status register should be acknowledged (cleared) before entering the Run mode.

MSTR = master (Bit 1): Indicates whether the SYNC pin will be an input or an output. If set the chip will enter the master mode of operation and the SYNC pin will become an output pin which puts out a sync pulse at the beginning of each operation. This serves as a signal for other slave chips that are used in a synchronous operating method. While in master mode, any operation requiring a sync input will not proceed, and the chip will "hang", waiting for a sync that will never come. The chip default is slave mode with the SYNC pin as an input.

LOBYT = low byte first (Bit 2): This bit is used to indicate which byte is accessed first in AUTOI or DMA operation. When this bit is set, the index register is incremented on the read or write of the Window High register. When this bit is clear, the index register is incremented on the read or write of the Window Low register. If DMA operation is specified, then setting this bit will make the low byte be output first, then the high byte, after which the index register is incremented. Conversely, clearing this bit will output the high byte first, then the low byte, then increment the index register. The default is low.

DMA = DMA Mode (Bit 3): When set enables DMA operation. DMA operation proceeds as follows:

1) The DMA bit must be set after defining all other registers (Instruction RAM, Alarm etc.) but prior to setting the RUN bit. The RUN bit is then set.

2) The sequence of operations in the Instruction RAM is executed.

3) At the end of the sequence, the DBR pin goes true, requesting DMA service, and the Index register is automatically cleared, pointing to the first location of the data buffer.

4) Each read of either Window Low or Window High register outputs a byte from the data registers. The DMA controller can read Window Low register, or Window High register, or alternate between Window Low and Window High. The same data is placed in both Window Low and Window High registers, and updated in both of them when either one is read. The data is placed in the Window registers beginning with data word 0 and incrementing on up. The placement of the low byte/high byte order is based on the LOBYT bit in the Control register. The number of bytes transmitted equals twice the number of operations defined, since the words are 16 bits going over an 8-bit bus. DBR remains asserted until all of the bytes have been transmitted. It is negated on the leading edge of the last byte read pulse. DBR acknowledge (setting the DBRAK bit in the Status register) is not required when transferring bytes via DMA.

The AUTOI bit does not have to be set when in the DMA mode. Setting the DMA bit forces the Index register to be auto-incremented in the Run mode. However if AUTOI is not set, then when in Halt mode auto-increment will not be enabled. If the AUTOI bit and DMA bit are both set, the auto-increment will occur in both the Run mode and the Halt mode.

t_{CLK} = enable external timer clock (Bit 4): When set, will divert the clock input for the internal sixteen bit timer to the t_{CLK} pin. When reset to 0, the timer runs at the internal chip clock frequency, which is 1/2 of that generated at the CLK pin.

SLFTST = self test (Bit 5): When set, the function of the input multiplexer is modified to enable self test operations. This bit also redefines the Instruction Word, specifically the CHAN field of the instruction word (See Figure 16 for the redefinition of the Instruction Word when SLFTST = 1). With SLFTST set the CHAN bits now specify which of four self tests is to be performed as shown below.

Instruction Word CHAN Field	Function	Description
000	System Offset	Inputs shorted together and shorted to ground
001	Internal Reference	Convert internal V_{REF} plus side tied to V_{REF} minus side tied to AGND
010	Minus Internal Reference	Convert internal V_{REF} minus side tied to V_{REF} plus side tied to AGND
011	Common Mode	Both inputs of the converter are tied to V_{REF}
100-111	Illegal	

These self-test results are useful for user confidence at power-on. The default on reset is 0, normal mode of operation.

RESET = soft reset (Bit 6): Is a software reset of the chip. This bit does not have to be cleared once set. The microprocessor should read this bit back to determine if the reset operation has completed, especially if a slow clock rate is being used. It takes at least 4 internal clocks for the reset bit to clear. Microprocessor communication with the chip should be held off until this bit is read back as cleared. When issuing a hardware reset, communication with the chip should be held off until the $\overline{RESET}$ pin goes inactive. The chip will be in the Halt mode (RUN bit cleared) after a reset. See RESET/Power-On Conditions (Section 4.2) for chip register conditions after a reset.

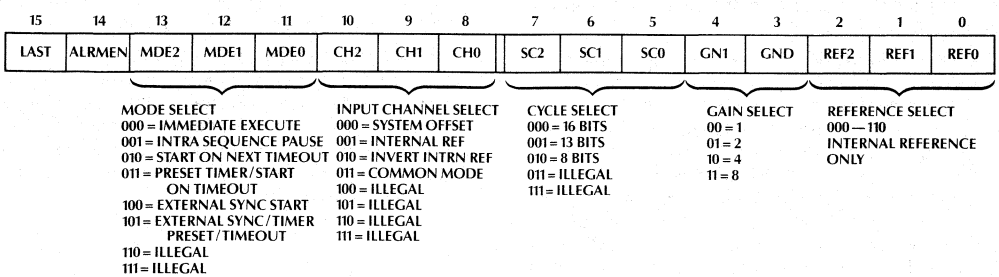


Figure 16. Bit Map of Instruction Word When SLFTST = 1

CAL = calibration start (Bit 7): When set, a self-calibration of the A/D converter will begin. Reading the CAL bit indicates whether the chip has been calibrated since the last reset or power-on condition. If CAL is a 1, then a calibration of the A/D converter has been performed since the last reset or power-up. When setting CAL, the user should not write a 0 back to clear it. ***Writing a 0 to the CAL bit has no effect;*** this will not clear it if it was previously set. Attempting to set the RUN bit without this bit being set will result in a run error condition, in which the RNER status bit will be set, and an interrupt being generated if it was enabled in the mask register. The amount of time required for calibration is 8,260 internal clocks, or 16,520 external clocks. To determine when a calibration is complete, the microprocessor should enable the calibration complete interrupt (CLCPIE) in the interrupt mask register, and wait for the interrupt to occur. Interrupt servicing of the calibration complete interrupt is done in a normal manner, in which the interrupt is acknowledged by setting the CLCPAK bit in the interrupt acknowledge register. All I/O to the ML2200 should be avoided during calibration (i.e., 16,520 external clocks after the CAL bit is set), because accessing the chip during calibration could adversely affect the calibration. If an interrupt is not desired, the microprocessor can read the Status register to verify completion 16,520 external clocks after the CAL bit is set. When the CAL bit is set, all other bits in the Control register should be cleared. DO NOT set the CAL and RUN bits simultaneously.

Status Register — Register 4

READ ONLY

INT	CLCP	RNER	ISQ	OVRN	ALRM	OVRG	DBR

Status Register

Register 4 serves as the status register of the various conditions that can occur. The bits in the Status register will be updated regardless of the Mask register. The status bits are updated any time within or at the end of a sequence of operations. The bits in the Status register are cleared by setting the corresponding bits in the Interrupt Acknowledge register. The status register can be polled at any time without fear of clearing the status bits. This register is not cleared at HALT time. When entering the Run mode, all of the old status bits should be cleared (acknowledged).

DBR = Data Buffer Ready (Bit 0): Is set when the chip has gone through one complete sequence of operations and has filled the data registers with the converted results. This bit signifies that the microprocessor should read all locations in the data registers that have relevant data. Reading all loaded data locations will clear DBR. If all loaded data locations are not read, DBRAK in the Interrupt Acknowledge register should be set to clear DBR, else OVRN will be set. The DBR pin is logically the same as the DBR status bit. The DBR pin is ALWAYS enabled and cannot be masked out. The DBR status bit is the only condition that can cause the DBR pin to be asserted. The DBR status bit can be enabled to assert the INT pin through the Interrupt Mask register.

OVRG = overrange interrupt (Bit1): Is set at the end of an operation when an underflow or overflow of the A/D converter has occurred (underflow and overflow are the most negative and most positive number, respectively, that is representable in the chip according to the specified cycle length). The overflow and underflow conditions apply to ALL incoming A/D converted data.

ALRM = limit alarm (Bit 2): Is the limit alarm status bit. It is set whenever the alarm criteria specified in the alarm registers is satisfied by a conversion from an operation where the ALRMEN bit is enabled. The limit alarm test only applies to an operation in which the ALRMEN bit is set.

Note that OVRG and ALRM can be enabled without enabling the DBR interrupt so that the microprocessor can be left alone until an overflow/underflow or limit alarm occurs. This is done to search for a limit condition first without taking any data into the microprocessor. Doing this, however, will set the OVRN (overrun error) bit in the status register, indicating that the microprocessor has not read any data from previous sequences.

OVRN = overrun error (Bit 3): The OVRN bit indicates that the microprocessor has missed from one byte to several blocks of data. Even if an overrun error occurs, the ML2200 or ML2208 continues converting the inputs and updating the data registers with the new conversions.

This bit may intentionally become set as a result of searching for the overflow/underflow or limit alarm criteria without reading the data.

The setting of the OVRN bit also occurs in DMA mode if all data has not been read by the completion of the next sequence. (Note: DBRAK should not be set in DMA mode, since DBR is automatically cleared by the chip.) If OVRN occurs in DMA mode, DBR will not be reactivated once all of the data from the sequence which was overrun is read; OVRN automatically disables DBR re-activation. Acknowledging OVRN (setting OVRNAK in the Interrupt Acknowledge register) will re-enable the DBR pin, however the OVRN bit may immediately be set again before the DMA controller can read the entire buffer. Therefore, it is recommended that in DMA mode if OVRN gets set, put the ML2200 or ML2208 in the Halt state, acknowledge the overrun and the DBR, then place the chip back in the Run mode.

ISQ = intra-sequence pause (Bit 4): Indicates that the chip has halted operation within a sequence as a result of choosing the ISQ op code in the mode field of the Instruction word. Setting the ISQAK bit in the interrupt acknowledge register will then re-start the operation within the sequence. This lets the microprocessor achieve timing control of individual operations within a sequence.

RNER = run error (Bit 5): Indicates that an error occurred either entering or operating in the Run state. The following operational errors cause the RNER bit to get set

1. Entering the Run state without having performed a self-calibration after the most recent Reset or power-up. The status of whether a calibration was executed or not is indicated by the CAL bit in the control register. If the CAL bit in the Control register is a one, the chip has already been calibrated.
2. Writing to any secondary registers other than the data registers during Run mode. All secondary register locations are readable during Run time.

CLCP = calibration complete (Bit 6): Is set at the end of a calibration sequence. The purpose of this bit is to notify the microprocessor that a self-calibration has completed.

INT = interrupt (Bit 7): Is identical to the state of the INT pin. The INT status bit and pin is an OR of the status bits enabled in the Interrupt Mask register. While the polarity of the INT pin can be defined in the interrupt mask register, this bit is positive true only.

Interrupt Acknowledge Register — Register 4

WRITE ONLY

	CLCPAK	RNERAK	ISQAK	OVRNAK	ALRWAK	OVRGAK	DBRAK

Interrupt Acknowledge Register

The status bits in the status register can only be cleared by setting the appropriate bit in this register; writing a zero has no effect. The relative bit positions in the Interrupt Acknowledge register are identical to the Status register except for bit 7, which is valid for reads (see explanation in Status Register) and undefined for writes (user must write a zero to this bit to be software-compatible for possible future redefinitions).

Sequence Register — Register 5

READ ONLY

1	1	1	1	1	SR2	SR1	SR0

Sequence Register

During the RUN mode, this register can be read back to indicate the current operation in progress. This is especially useful for examining interrupts when multiple intra-sequence pauses are specified. Bits 3-7 always reads 1s.

Registers 6 and 7 — these registers are reserved for future use.

3.2 Secondary Registers

There are twenty 16-bit wide secondary registers containing the Data RAM, Instruction RAM, Timer, Alarms, Alarm Criteria Register, and Interrupt Mask. Except for the Data RAM, the secondary registers should only be accessed on initialization, or when the chip is placed in the Halt mode.

Secondary Registers 0 to 7

Data RAM (read only)
Calibration Holding Register (write only)

UPPER BYTE D15	D8	LOWER BYTE D7	D0	
				0
				1
				2
				3
				4
				5
				6
				7

8 x 16 A/D DATA REGISTERS
16-BIT CAL REGISTER

The Data RAM consists of eight 16-bit wide registers that hold the output results from the latest conversion sequence. Each word in the Data RAM has a one-for-one correspondence with a word in the Instruction RAM. The Data RAM is also referred to as the data output registers.

The data output registers are double buffered and readable by the microprocessor at any time. The A/D converter fills a "shadow" bank of registers during conversions, while the microprocessor is free to read the output registers. When the sequence is done, the "shadow" bank information is transferred to the output registers for the microprocessor to read, after which time DBR is asserted. Therefore, the microprocessor has essentially one sequence time to drain the data buffer. This time varies according to the number of operations defined, the system clock frequency, the mode field for each operation, and the cycle length (number of bits to be converted). Refer to Conversion Times for more information.

Data Format

All data is returned from the converter in 16-bit two's complement format, right hand justified, with the sign bit extended across the most significant unused bits.

Cycle	+Max	– Max	Mid-Range
16	7FFF	8000	0000
13	0FFF	F000	0000
8	007F	FF80	0000

Calibration Holding Register —
This register is for diagnostic purposes only. It is one 16-bit wide register mapped into the write only secondary address space 0 to 7 (i.e., a write to any of the secondary addresses 0–7 will load the Calibration Holding register). This register is write only and cannot be read back directly. It is used when the mode field in the Instruction Word is set to CAL Write, and the Instruction is executed. This command takes the contents of the Calibration Holding register and loads it into the Calibration register of the A/D converter. Note that this will change the calibration of the A/D converter, and a calibration of the A/D converter should be done after a CAL Write command is issued.

Instruction RAM — Secondary Registers 8 to 15 (Read/Write)

OP	0	8
OP	1	9
OP	2	10
OP	3	11
OP	4	12
OP	5	13
OP	6	14
OP	7	15

8 x 16 OPERATION REGISTERS

The Instruction RAM, sometimes referred to as the Operation registers, consists of eight 16-bit wide registers broken up into seven different fields (see Figures 10 and 10A). Each Instruction or Operation defines a single conversion, where the converted data result is stored in the corresponding data output register. Note that when the SLFTST bit in the Control register is set, the Instruction Word is redefined for diagnostic mode. Figure 12 illustrates the redefinition when SLFTST is set. The following section defines the seven different fields making up the Instruction word when SLFTST = 0.

D15	D14	D13-11	D10-8	D7-5	D4,3	D2-0
LAST	ALRMEN	MODE	CHAN	CYCLE	GAIN	REF

REF (Bits 2, 1, 0 — Voltage Reference Selection) REF specifies the source of the voltage reference used for the A/D conversion.

GAIN (Bits 4 and 3 — Gain Settings) GAIN defines the gain of the precision instrumentation amplifier. The gain can be either 1, 2, 4, or 8. Each gain factor of 2 adds an additional 4 internal clock cycles ($1/f_{CLKI}$) to the conversion time. Therefore a gain of 8 adds an additional 12 internal clock cycles to the conversion time.

CYCLE (Bits 7, 6, 5 — Cycle Select) CYCLE defines one of five different cycles: 8-, 13-, or 16-bit conversions, and READ or WRITE CAL CODE. Choosing 8-, 13- or 16-bit cycles determines how many bits the A/D converter will convert. However, even though the converter has a 16-bit cycle, it may not have 16 bits of useful resolution. The useful resolution of the converter can be determined from the linearity specs.

Since the algorithmic converter is a successive approximation type of converter, an 8-bit cycle requires the least amount of time to convert, and the 16-bit cycle requires the most. Refer to Sampling Rates and Conversion Times for the exact number of clocks each cycle takes.

READ CAL CODE and WRITE CAL CODE cycles are for diagnostic purposes only. READ CAL CODE reads the Calibration register in the A/D converter and loads it into the corresponding data output register. WRITE CAL CODE transfers the contents of the Calibration Holding register into the A/D converter's Calibration register. The transfer is complete after the operation is executed. Refer to Diagnostics for more information on READ and WRITE CAL CODE.

CHAN (Bits 10, 9, 8 — Input Channel Number) defines the input channel to be converted.

ALRMEN (Bit 14 — Alarm Enable) When this bit is set the alarm criteria for the operation is enabled, otherwise the alarm is disabled for this operation. If ALRMEN is set and the alarm condition is met, the ALRM bit in the Status register will be set at the end of the operation.

LAST (Bit 15 — Last Operation) signifies that this operation is the last operation of the sequence. The chip will return to and begin the first operation of the sequence after execution of the current operation. If all eight operations are specified, the last one MUST have this bit set.

MODE (Bits 13, 12, 11 — Mode Selection) defines the condition that must be met for the operation to proceed. The mode field also has an effect on the Operation Execution Time.

000	Immediate Execute
001	Intra-Sequence Pause
010	Start on Next Time out
011	Preset Timer/Start on Time out
100	External Sync Start
101	External Sync/Timer Preset/Time out
110	ILLEGAL
111	ILLEGAL

Events That Occur Within an Operation

To better understand six modes of the ML2200 or ML2208 one must first understand the events that occur during an operation. This can be aided by referring to Figure 17.

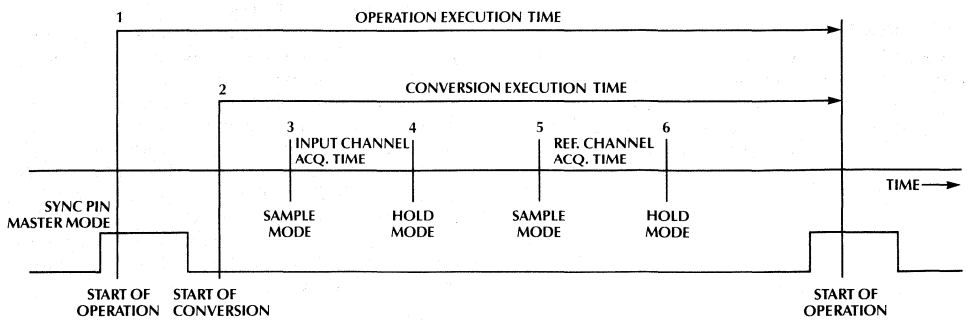


Figure 17. Events Within an Operation

The first event that occurs in the Operation is the Start of Operation. This may or may not be the beginning of the conversion, depending on the mode selected. The time between the Start of Operation and Start of Conversion is variable. When the conditions of the mode have been met, the Start of Conversion occurs.

The Conversion Execution time includes the input and reference acquisition times, the gain time, and the successive approximation conversion time. Shortly after the Start of Conversion the S/H goes into sample mode acquiring the input channel for eight internal clocks. After the input has been acquired the S/H goes into hold mode, disconnecting the S/H from the input channel, and transferring the charge into the A/D converter. A couple of clocks later the same S/H goes into sample mode on the reference voltage, either the internal V_{REF} or one of the input channels. The reference acquisition time for all six modes is the same; eight internal clocks. After the S/H goes into hold mode the successive approximation A/D conversion begins. When the conversion is complete the next operation begins.

Immediate Execute (000) — The Start of Conversion begins at the Start of Operation. In other words, the conversion begins the instant the operation begins. There is no gating item delaying the conversion. This mode allows the chip to convert at its maximum rate with no unnecessary delays. As an example of calculating the sequence time, if all eight operations used Immediate Execute with a gain of 1 and a 13-bit conversion, the time to execute one sequence (all eight operations) would be 8 * 110 = 880 internal clocks.

Intra-Sequence Pause (001) — This mode provides a way for the microprocessor to initiate conversions, rather than the other modes which either initiate conversions from internal timings or an external pulse. At the Start of Operation the ISQ status bit is set. The microprocessor will recognize the setting of the ISQ status bit either by polling the Status register, or having enabled the ISQ interrupt. The Start of Conversion is delayed until the ISQAK bit in the Interrupt Acknowledge register is set.

Start on Next Time out (010) — After the Start of Operation occurs the Start of Conversion is delayed until the internal timer decrements from 1 to 0. When using this mode the timer will be free-running. This means that the timer is initialized in the Halt mode and left alone to decrement and reload automatically when in the Run mode. This mode can be used to establish a specific sampling rate. Note that the timer value must be greater than the conversion time, therefore this mode can only slow the sampling rate down from its maximum rate. In the case where several operations are used, and only one of them uses this mode, the timer value must be greater than all the other Operation Execution times plus the current operation conversion time.

Preset Timer/Start on Time out (011) — At the Start of Operation the timer is loaded with its pre-programmed count. The delay between the Start of Operation and the Start of Conversion is the pre-programmed count. Execution time of the operation is the pre-programmed timer count plus the conversion time. As opposed to mode 2, the timer can be any value between 2 and 2^{16}; i.e., there is no restriction on the timer value being greater than the conversion time. One application of this mode would be when an external analog event is triggered by the SYNC pulse, and the conversion needs to be delayed by a programmable amount of time.

Using the External SYNC Input — The following description applies to modes 4 and 5, since these two modes use the external SYNC input. These modes should only be used when the SYNC pin is programmed as an input (MSTR bit in Control register is 0). If the external SYNC signal arrives before the Start of Operation, it may be latched depending upon the arrival time. If it arrives 22 clocks after the previous operation's Start of Conversion, external SYNC will be latched; any time before will miss the pulse. Therefore the external SYNC pulse rate should not be any faster than the frequency of the operations which use this mode, otherwise there will be more external SYNC pulses than conversions.

External SYNC Start (100) — After the Start of Operation, the Start of Conversion is delayed until the rising edge of the SYNC pulse and the next rising edge of the internal clock. Unless the rising edge of the external SYNC is synchronized with the internal clock (See t_{SYNCCK} Spec), the aperture uncertainty is one internal clock.

External SYNC/Timer Preset/Time out (101) — For this mode, the external SYNC pulse presets the timer, and when the timer times out the Start of Conversion begins. The timer is preset after the rising edge of the external SYNC and the next rising edge of the internal clock. When the timer transitions from 1 to 0, the Start of Conversion begins. As in the previous mode, unless the rising edge of the external SYNC is synchronized with the internal clock, the aperture uncertainty is one internal clock.

Timer Functions of the Different Modes — The on-chip timer is started when RUN is asserted. It then free-runs, pre-loads and restarts itself at the pre-programmed count unless one of the modes in an operation word specifies a timer preset. If "Start on Next Timeout" mode is selected for all operations, the timer free-runs and subsequently starts conversions on regular intervals, without the inclusion of any variable overhead timing requirements of any specific operation. The "preset timer" function that can be specified in any operation, functions as a "one-shot" time out feature; however it can upset the regularity of conversions. The use of the external SYNC start allows flexibility with asynchronous conditions outside the chip. In addition, the use of time out with external SYNC allows synchronous operation of multiple Micro Linear chips with interleaved operation. If a different rate is desired other than increments of one master clock cycle (1/2 the CLK pin frequency) or if external events need to be counted before starting an operation, then setting the t_{CLK} bit in the control register will divert the timer to the t_{CLK} pin for all operations.

Timer Holding Register — Secondary Register 16 — This register holds the pre-programmed value of the timer. The value is in 1 internal clock increments, or the period of t_{CLK} if this input is used. The timer is a countdown timer, therefore the realized delay will be the number loaded into the Timer Holding register multiplied by the clock period. The value is written as a 16-bit binary word, and either high or low bytes can be written first. These registers are both writable and

readable, with register writes executed only when the chip is in the Halt mode (RUN bit cleared in the control register). Reading the Timer Holding register will return the pre-programmed value for the timer, it will not provide the actual timer value. Timer Holding register values of 1 or 0 are illegal and will "hang up" the timer when placed in Run mode. Therefore the minimum value that can be loaded into the Timer holding register is 2. The timer is decrementing when in Run mode and idle when in Halt mode. When the chip is placed in Run mode, the timer is automatically loaded with the value in the Timer Holding Register, and begins to count down.

Alarm Registers — Secondary Registers 17, 18 (Read/Write) — These registers specify the alarm criteria against which the converted data of a current operation is compared. The comparison occurs only when the ALRMEN bit is set within the operation. Secondary register 17 is Alarm A and secondary register 18 is Alarm B. These values are written in two's complement format, right justified and sign extended (refer to Data Format for more information).

Alarm Criteria Register — Secondary Register 19 lower byte (Read/Write) — Specifies the compare criteria to be used with alarm registers A and B. Bit 0 specifies whether the comparison of alarm word A is to be greater than (setting the bit) or less than equal to (clearing the bit). Similarly, bit 1 specifies the same criteria for alarm word B. The criteria of the two groups can be "ANDed" or "ORed" together by clearing (OR) or setting (AND) bit 2. Bits 3 and 4 enable the alarm comparison for words A and B, respectively. Bits 5, 6, and 7 are unused and be can be any value when written, always read as ones. The following table illustrates all of the possible combinations, X signifies don't care.

Bit Number					
4	3	2	1	0	
ENB	ENA	AND	GB	GA	Test Done:
0	0	X	X	X	No Test
0	1	X	X	0	⩽A
0	1	X	X	1	>A
1	0	X	0	X	⩽B
1	0	X	1	X	>B
1	1	0	0	0	⩽B or ⩽A
1	1	0	0	1	⩽B or >A
1	1	0	1	0	>B or ⩽A
1	1	0	1	1	>B or >A
1	1	1	0	0	⩽B and ⩽A
1	1	1	0	1	⩽B and >A
1	1	1	1	0	>B and ⩽A
1	1	1	1	1	>B and >A

Using the various criteria, the chip can discern whether a certain channel is inside or outside a band, or greater than or less than a value. Notifying the microprocessor can be done through an interrupt or by polling the status register.

Interrupt Mask — Secondary Register 19 Upper Byte (Read/Write)

D15	D14	D13	D12	D11	D10	D9	D8
INTL	CLCPIE	RNERIE	ISQIE	OVRNIE	ALRMIE	OVRGIE	DBRIE

This register is used to define which interrupt conditions are capable of setting the hardware interrupt pin and the INT bit of the Status register. The bits in the Interrupt Mask register are interrupt enable bits, meaning when the bits are set they enable the corresponding status bit to activate the hardware interrupt pin as well as the INT bit in the Status register. The INTL bit determines the polarity of the INT pin. If set, the INT pin becomes active low, with an open drain output. If clear, the INT pin becomes active high, with driving capability in both directions.

Secondary Registers 20 to 31 — Undefined
These registers are undefined and will cause unpredictable results if read or written to.

4.0 SAMPLING RATES AND CONVERSION TIMES

To determine the sampling rate, one must first determine the sequence execution time. A sequence is defined as the number of operations or instructions used. Therefore the sequence execution time equals the sum of the individual operation execution times. The simplest case for determining the sampling rate is when only one operation is used in the sequence. Then the sampling period is the operation execution time. If all eight instructions are used in the sequence, the sampling rate would be the sequence rate multiplied by the number of times the channel was sampled in the sequence.

It is possible to sample one channel more frequently than another. For example, if every other operation sampled channel 0, while the remaining operations sampled channels 1, 2, and 3, the sampling rate for channel 0 would be four times the sampling rate of the other channels. If periodic sampling is important, one must be careful when sampling a channel multiple times in a sequence since different operations can have different execution times.

Example: Sampling Four Channels in a Burst Every 10 ms

Using Mode 2 "Start on Next Time out" for Instruction 0 will establish the 10 ms sampling rate, once the clock is initialized properly. Instructions 1, 2, and 3 can each use Mode 0 "Immediate Execution". For the ML2200, each instruction can sample a different channel, thus covering all four channels in a burst. For the ML2208, the same holds true except all eight channels can be sampled in a burst, periodically.

Assuming the external clock is 7 MHz and each conversion is 13 bits with a gain of 1, the conversion time for each operation will be 110 * 286 ns = 31.4 μs. Therefore four instructions will require 4 * 31.4 μs = 125.7 μs. The execution time is much less than the sampling rate, thus the timer can be used to set the sampling rate. The timer value for a 10 ms sample rate is: 10 ms/286 ns = 35,000 decimal or 88B8H.

Operation or Instruction Execution Time

Figure 17 illustrates the Operation Execution Time. The time between the Start of Operation and Start of Conversion is variable and depends on the Mode chosen. For more information on how to determine the time between Start of Operation and Start of Conversion refer to the Secondary registers Mode field description in the Instruction RAM.

The Conversion Execution time depends on the Cycle, the Gain, and the Mode chosen in the instruction word. Modes 0–5 all behave the same way when it comes to Conversion Execution Time. To help determine the Conversion Execution Time the following table gives the number of internal clocks used for Modes 0–5 based on the Cycle chosen.

Cycle	Number of Internal System Clocks Needed ($1/f_{CLKI}$)
16-Bit	128
13-Bit	110
8-Bit	80
Read CAL	80
Write CAL	52

Add 4 extra clocks to the Cycle time for each gain of 2 (including Read CAL and Write CAL). For a gain of 2 add 4 extra clocks, for gain of 4 add 8 extra clocks, for gain of 8 add 12 extra clocks. Example: Modes 0–5, Cycle = 13-bit conversion with a gain of 8. Conversion Execution time is 122 internal clocks.

5.0 MICROPROCESSOR INITIALIZATION PROCEDURE

The following sequence of steps is recommended when initializing the ML2200 from the microprocessor:

1) Keep reset active for at least 10 internal clock cycles after power supplies have stabilized. If a software reset is issued, hold off microprocessor communications with the chip until the RESET bit in the control register is read back as cleared, which takes 4 internal clock cycles.
2) If desired, check the data register path by performing a write and read of the calibration register for all 8 operations. (This step is optional, but does provide user assurance of the integrity of the on-chip data paths.) The calibration register is a full 16-bit data path.
3) Perform a calibration by first enabling the CLCP interrupt in the Interrupt Mask register, then start the calibration by asserting the CAL bit in the Control register. Alternately, if an interrupt driven system is not desired, the interrupt status register can be polled 8260 internal clocks after the CAL bit has been set. The chip should not be polled during calibration.
4) Upon receiving the CLCP interrupt, acknowledge it. If desired, read back the calibration code to verify a successful calibration. Other diagnostics may be run at this time, however diagnostics are optional and not required.
5) Load the Instruction RAM, alarm criteria, interrupt conditions, and timer. Set the proper data transfer mode up (DMA, interrupt driven or polled mode.) Clear all status bits before setting the RUN bit.
6) Start the chip running by setting the RUN bit in the Control register. This may be done by ORing the RUN bit with the other bits already configured in the Control register; *however* do not set the CAL bit again or another calibration will take place. Writing a 0 to the CAL bit has no effect; it will still read 1.

5.1 Reset/Power-On Conditions

When applying power to the ML2200, DV_{CC} and AV_{CC} should never be powered-on at different times.

It is OK to assert both $\overline{RD}$ and $\overline{WR}$ during RESET time, but not legal to do so otherwise; this may damage the chip internally.

The following list specifies the affected registers on the chip after a reset is performed. Note that both hardware and software reset of the chip have identical effects.

All registers shown below are cleared (all bits 0):

Primary Registers:
- Index register (register 2)
- Control register (register 3)
- Status register (register 4)
- Sequence status (register 5)

Secondary Registers:
- Interrupt bit mask (upper half, register 19)
- Alarm criteria register (lower half, register 19)

All other registers will have random data in them after power-on. If a hardware or software reset is performed later, registers which are not listed above will be unchanged.

Re-calibration after a hardware or software reset is not necessary, since the calibration register remains the same after a reset. Only after a power-up is a calibration necessary. However the CAL bit in the Control Register will be cleared after a reset. Setting the RUN bit while the CAL bit is clear will cause the RNER bit to be set. But, if a calibration had been done before the reset, the RNER may be ignored.

5.2 Timer

If any of the operations require a timer function, (either a one-shot or regular conversion interval) then the timer value must be written. This is done by writing the index register value to 10 hexadecimal and writing the proper 16-bit time value to the window registers. The timer value must be greater than 1. If using mode 2 "Start on Next Time out" the timer value must be greater than the conversion time.

5.3 Limit Alarm Operation

The chip may be set up to watch for certain data conditions by enabling the proper interrupt bits in the Interrupt Mask register. These conditions include A/D overrange/underrange and user-defined alarm criteria. In order to use the alarms, the A and B alarm values must be defined. Note that since alarm registers A and B are 16 bits wide, 13-bit two's complement sign extended values must be loaded. (Refer to Data Format for more information). In order to further qualify alarm registers A and B, the Alarm Criteria register must be initialized.

5.4 Defining Interrupt Conditions

If the chip is used in polled situations, the interrupt mask bits need not be set unless the "OR" of the interrupt conditions, bit 7 in the Status register is used.

If the chip is used in interrupt mode rather than polled mode, the desired interrupt conditions should be considered. In addition to the interrupts specified for data comparison operations, several other interrupts can be defined in the Interrupt Mask register. The DBR bit can be set if the DBR pin is not used. This enables interrupts at the end of sequences for data transfer via the INT pin. The intra-sequence interrupt bit should be enabled if intra-sequence pauses are desired in any of the operations. Overrun error and run-time error bits should be enabled if trapping of these errors is desired.

Note that alarm A and B and overrange interrupts occur at any time within the sequence of operations. Due to the interrupt latency time of the microprocessor, multiple interrupts of this type within a sequence may be indistinguishable from each other. The A and B alarms should generally be used on only one operation so that its source can be determined with no ambiguity. Overrange interrupts can be handled by examining the data in the chip at the end of the sequence.

The INT pin polarity can be defined to be active high (bit 15 cleared in the Interrupt Mask register) or active low (bit 15 set). When active low is chosen, the INT pin is open drain without a pull-up. When active high, the INT pin is driven actively in both directions. The default condition is active high, and the INT pin is actively driven low during reset time.

6.0 METHODS OF DATA TRANSFER TO THE MICROPROCESSOR

There are several ways to handle the data output; polling, interrupt, or DMA. If interrupts are the method chosen, method 5) may be preferable. Method 5) DMA/Interrupt mode, does not require a DMA controller. It simply uses the DMA mode of the ML2200 or ML2208 which can be interfaced to an interrupt controller.

1) Intra-Sequence pause instruction is used when the microprocessor is not going to periodically/continuously read the data, but it will read the data at arbitrary times. The Table 1 below shows the op codes to sample all eight channels.

Table 1. Channels in an ML2208 at Arbitrary Times

	Last	ALRMEN	Mode	CHAN	Cycle	Gain	REF
SEQ0	0	0	Intra Sequence Pause	CH0	13	1	Internal
SEQ1	0	0	Immed Execute	CH1	13	1	Internal
SEQ2	0	0	Immed Execute	CH2	13	1	Internal
SEQ3	0	0	Immed Execute	CH3	13	1	Internal
SEQ4	0	0	Immed Execute	CH4	13	1	Internal
SEQ5	0	0	Immed Execute	CH5	13	1	Internal
SEQ6	0	0	Immed Execute	CH6	13	1	Internal
SEQ7	1	0	Immed Execute	CH7	13	1	Internal

Using these instructions the program begins when the RUN bit is set in the control register. Immediately after RUN is set, before the first conversion takes place, the ISQ bit in the status register is set. This indicates that the sequencer has paused. When the microprocessor wants to read a value on one or more of the channels it sets the ISQAK bit in the Interrupt Acknowledge register. The ML2208 then performs eight conversions back-to-back, jumps back to sequence 0, and sets the ISQ and DBR bits in the status register. The data from all eight channels is now available in the Data RAM. The next time a conversion is desired, once again the microprocessor sets ISQAK in the interrupt acknowledge register.

2) **Polled mode transfer** is done simply by polling the status register and examining the DBR bit to see if a sequence has been completed. The DBRIE interrupt mask bit need not be set, but an acknowledge should be done by setting DBRAK in the Interrupt Acknowledge register, otherwise an overrun error will occur. The CPU can just poll the INT bit in the Status register. Only the bits which are enabled in the Interrupt Mask register will set the INT status bit. When the INT bit is set, the CPU can examine the other status bits to determine which requests are active.
3) **Interrupt mode** can be implemented using the INT pin and enabling the desired interrupt conditions in the Interrupt Mask register. The polarity of the INT pin can be selected at the same time. If desired, DBR can be used as a second interrupt pin to signify the transfer of data only. This may be useful in systems with multiple and prioritized interrupt structures. If DBR is used, the DBR mask bit in the interrupt mask register should be disabled or cleared.
4) **DMA mode** can be implemented by setting the DMA enable bit in the control register and selecting high byte or low byte first by setting or clearing the LOBYT bit. The DBR pin is utilized as the DMA request, and will remain asserted until all data from the sequence is read.
5) **DMA/Interrupt mode.** DMA mode can also be used in non-DMA applications. Although this appears to be unconventional, it may actually be preferred over the interrupt mode because of its convenience and speed. One way to do this would be to use the DBR pin as an interrupt request but enable DMA mode in the DAP. When data is ready DBR interrupts the microprocessor. The

microprocessor then reads either window register the required number of times to drain the Data RAM. Using the DMA mode interrupt method over non-DMA mode interrupt method saves a lot of overhead. For example in non-DMA mode interrupt method (assuming AUTOI is set), the index register would have to be set on entry, and the DBRAK bit would have to be set each service routine. In DMA interrupt mode, neither the Index register nor the DBRAK bit would have to be set. These are handled automatically in DMA mode.

7.0 POWER-DOWN MODE

The chip can be powered-down by asserting the P_{DN} pin. It is advisable to place the chip in HALT mode first by clearing the RUN bit in the control register, however the chip will automatically go into Halt mode when powered-down. All analog circuits are powered-off; digital circuits are left in an idle state. All registers within the chip will retain their values down to a level of 2V between V_{CC} and GND.

Powering-up the chip is done by bringing P_{DN} high. The chip will be in Halt mode upon power-up. Note, however, that the first 10ms of chip operation after a power-up will not be valid due to the settling of quiescent bias conditions within the on-chip's analog circuits. Any data that is returned for this period after power-up should be considered invalid. The user has the choice of either throwing away the first 10ms of data or waiting for 10ms and then setting the chip in RUN mode. The on-chip timer can be used for this purpose, if desired, by defining a sequence of dummy operations that last for the required delay, then re-writing the required operations for normal use.

Acknowledge register. D_{BRAK} should also be set sometime before the next sequence to prevent the OVRN bit from being set, however this is not necessary.

Note that the microprocessor cannot let the ML2200 sequencer run continuously, i.e., SEQ 0 would be changed to Immediate Execute and asynchronously read the Data RAM. The problem in this case would be that the microprocessor may read the data at the same time that the chip is updating it. That is why either polling, interrupt, or DMA transfer is required in a continuous run mode of operation.

2

APPENDIX A

Diagnostics

The ML2200 and ML2208 may be run through a diagnostic routine after power-up. The DAP provides software programmable diagnostics so that no external hardware is necessary. Diagnostics are not necessary. They are provided as an option to the user.

Self-Test Mode

Setting the SLFTST bit in the Control register redefines the CHAN field in the Instruction Word. This in effect changes the input to the Sample-and-Hold from the multiplexer input channels to internal points within the chip; such as V_{REF} and AGND. Conversions in the Self-Test Mode allow the user to determine how the Sample-and-Hold and A/D converter behave with known input signals. This can be useful as a diagnostic routine for a product in the field, or as a debugging feature during product development. Figure 16 illustrates the re-definition of the instruction word when SLFTST = 1.

1. **System Offset** - The positive and negative inputs to the Sample-and-Hold are tied to analog ground. With this setting, converted data will give the offset of the A/D converter and Sample-and-Hold combination.
2. **Internal Reference** - Connects the positive input of the Sample-and-Hold to V_{REF} and the negative input of the Sample-and-Hold to analog ground. The result of converting in this test mode is a value near positive full scale.
3. **Invert Internal Reference** - Connects the negative input of the Sample-and-Hold to V_{REF} and the positive input of the Sample-and-Hold to analog ground. The result of converting in this test mode is a value near negative full scale.
4. **Common Mode** - Both the positive and negative inputs of the Sample-and-Hold are tied to the internal V_{REF}. The result of a conversion in this test mode indicates how well the converter is rejecting a common mode signal.

Since setting the SLFTST bit merely changes the input to the Sample-and-Hold, conversions must be executed in order to read the results. This means placing the chip in the RUN mode and reading the results from the Data RAM. It is possible to run one sequence then halt the sequencer and read the results. The sequencer can be put in a "pause" via the Intra Sequence Pause Mode instruction. The following instructions accomplish this:

	LAST	ALRMEN	MODE	CHAN	CYCLE	GAIN	REF
SEQ 0	0	0	INTRA SEQ PAUSE	SYSTEM OFFSET	13	1	0
SEQ 1	0	0	IMMED EXECUTE	INT REF	13	1	0
SEQ 2	0	0	IMMED EXECUTE	MINUS INT REF	13	1	0
SEQ 3	1	0	IMMED EXECUTE	COMMON MODE	13	1	0

After the RUN bit is set, the ISQ bit in the status register is immediately set. Setting the ISQAK bit in the Interrupt Acknowledge register will allow the sequencer to continue. The next time the ISQ bit is set, the results may be read from the Data RAM.

Reading and Writing to the Calibration Register

The ML2200 and ML2208 architecture provides a way for the microprocessor to indirectly read and write to the A/D converter; specifically the Calibration register and the A/D's Data

register. Figure 18 illustrates this architecture.

The instructions that cause these transfers are READ CAL CODE and WRITE CAL CODE; selected in the Cycle field of the instruction word when SLFTST = 0. WRITE CAL CODE transfers the contents of the Calibration Holding register into the A/D converter's Calibration register. READ CAL CODE transfers the contents of the Calibration Holding register through the A/D's Data register, into the Data Output register with the same location as the operation.

As a result of providing READ and WRITE CAL, it is possible to execute digital loopbacks through the Calibration register, A/D registers, and all 8 Data Output registers. These loopbacks provides user assurance that all of the paths are clear and there are no stuck bits.

Writing to the Calibration register changes the calibration of the A/D converter. Therefore a self calibration should be performed after executing a WRITE CAL CODE to ensure the A/D is properly calibrated.

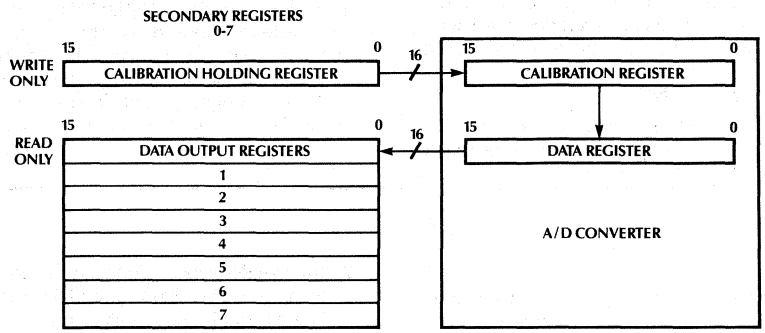


Figure 18. Digital Loopback Architecture

DIGITAL LOOPBACK ARCHITECTURE

Reading the calibration register provides a way for the microprocessor to determine that the self calibration was successful. The microprocessor configures the DAP to execute a READ CAL CODE after a self calibration has been performed. If the lower byte of data from the READ CAL CODE is anything other than all 1s, then the calibration was successful.

Even though the calibration register itself is a 16-bit register, and is capable of holding a 16-bit result, only the lower 9 bits are significant in determining the calibration code. These 9 bits have a sign magnitude format; in other words the 9th bit (MSB of the 9-bit word) is the sign bit, and the other eight bits are magnitude bits. An easy way to determine whether the calibration has passed or failed is to read the lower data byte after a READ CAL is executed. If it's not all 1s then the calibration was a success.

APPLICATIONS

Utilizing instruction RAM bits 0, 1, and 2, any of the differential input channels of the ML2200 can be programmed to sense the external reference (See Figure 13.) Only single ended channels 0 thru 5 can be used on the ML2208 (See Figure 14.)

Figure 19. Using a 2.5 V External Reference

The system gain errors can be nulled by applying 2.4991 V (the full-scale voltage minus 1.5 LSB) to one of the input channels and adjusting R1 until the digital output toggles between 0 1111 1111 1110 and 0 1111 1111 1111. If offset is not adjusted the full-scale voltage will be shifted by the amount of this unadjusted offset voltage.

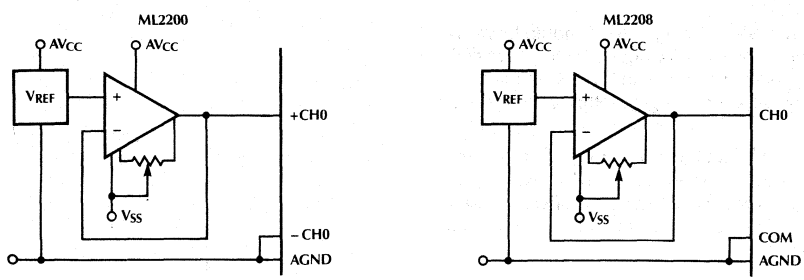


Figure 20. Adjusting Full-Scale Error

APPLICATIONS (Continued)

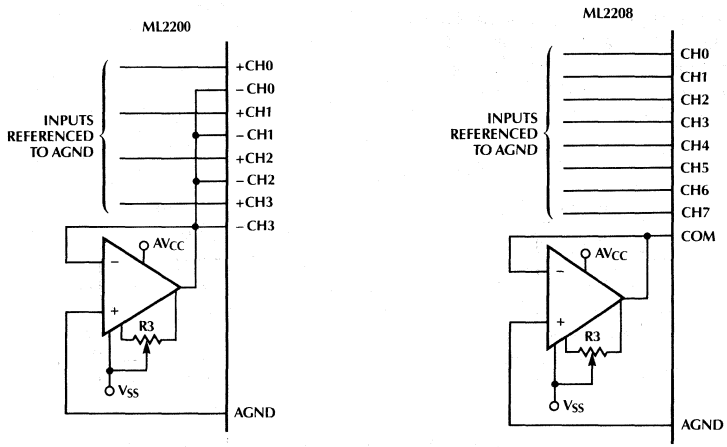


Figure 21. Adjusting Zero Error

An op amp with an offset adjustment with a range of at least ±1.3 mV is required, like an OP–27. The Zero Error can be nulled by first applying 305 μV to one of the input channels (referenced to AGND.) 305 μV is equivalent to ½ LSB which is the ideal input voltage which should cause the digital output to toggle from 0 0000 0000 0000 to 0 0000 0000 0001. Adjust R3 until this occurs.

If an external reference is also being used, it should be referenced to AGND, while the COM or negative inputs are tied to the offset op amp as shown above. In this configuration, the offset adjustment will effect the gain setting and so should be set first.

The Channel to Channel Zero Error and Full-Scale Error are very low and do not need to be adjusted seperately. If, however, the input signal sources have their own different offsets, a separate op amp, with an offset adjustment, can be placed at each channel input.

APPLICATIONS (Continued)

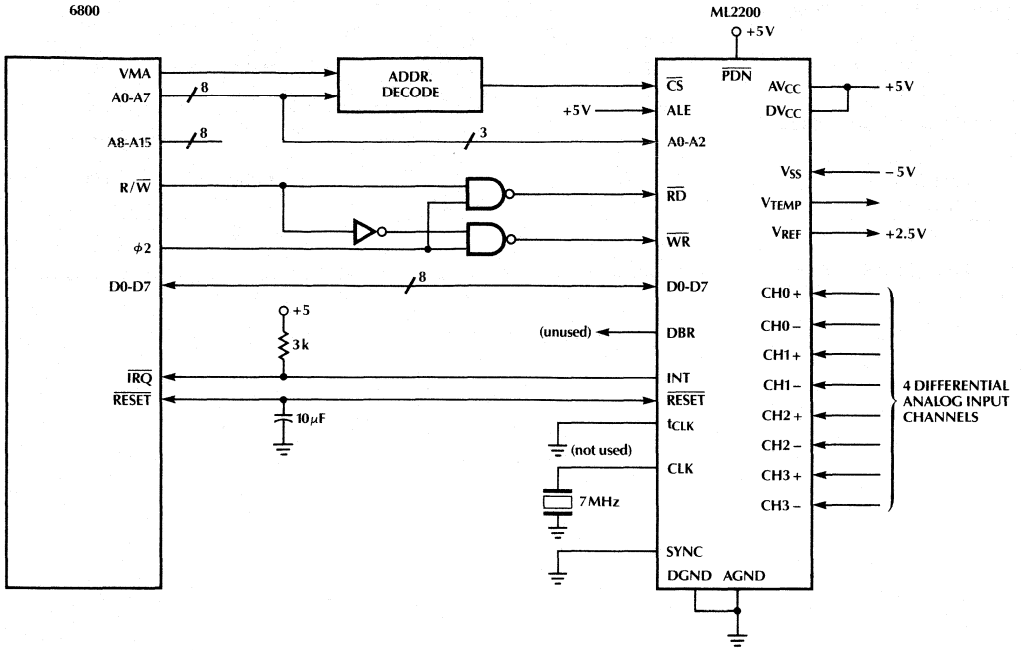


Figure 22. Interfacing ML2200 to 6800 Type Microprocessors

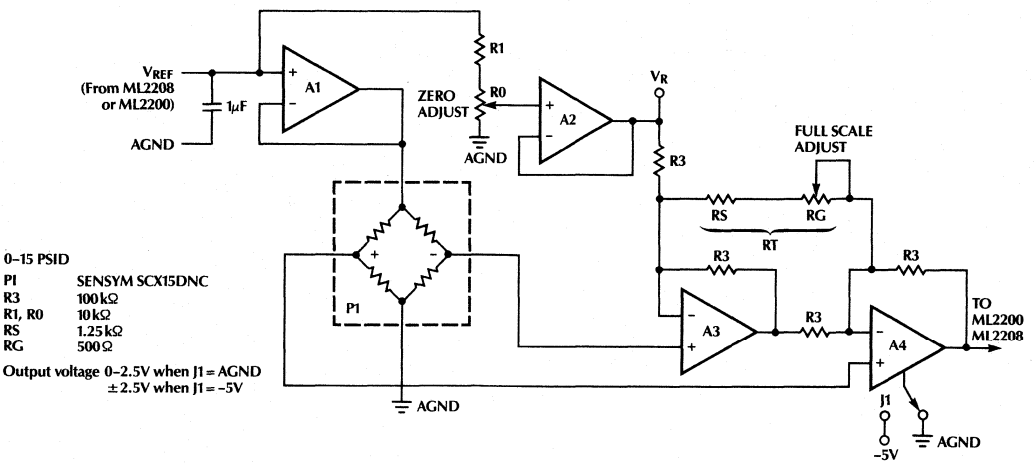


Figure 23. Pressure Sensor Application

ORDERING INFORMATION

PART NUMBER	LINEARITY ERROR	MINIMUM CONVERSION	PACKAGE	TEMPERATURE RANGE
Four Differential Analog Inputs				
ML2200BCJ	±¾ LSB	31.5μs	Hermetic DIP	0°C to +70°C
ML2200CCJ	±1 LSB	31.5μs		
ML2200DCJ	±1 LSB	44.0μs		
Eight Single Ended Analog Inputs				
ML2208BCJ	±¾ LSB	31.5μs	Hermetic DIP	0°C to +70°C
ML2208CCJ	±1 LSB	31.5μs		
ML2208DCJ	±1 LSB	44.0μs		

ML2200EX, ML2208EX

ML2200, ML2208 Exerciser

GENERAL DESCRIPTION

The ML2200, ML2208 Exerciser is a versatile development tool that shortens the development time and aids in the understanding of the ML2200, ML2208 Data Acquisition Peripherals. In a short period of time a user is able to reset and calibrate the part, start executing programs, and evaluate the performance and operation of the part.

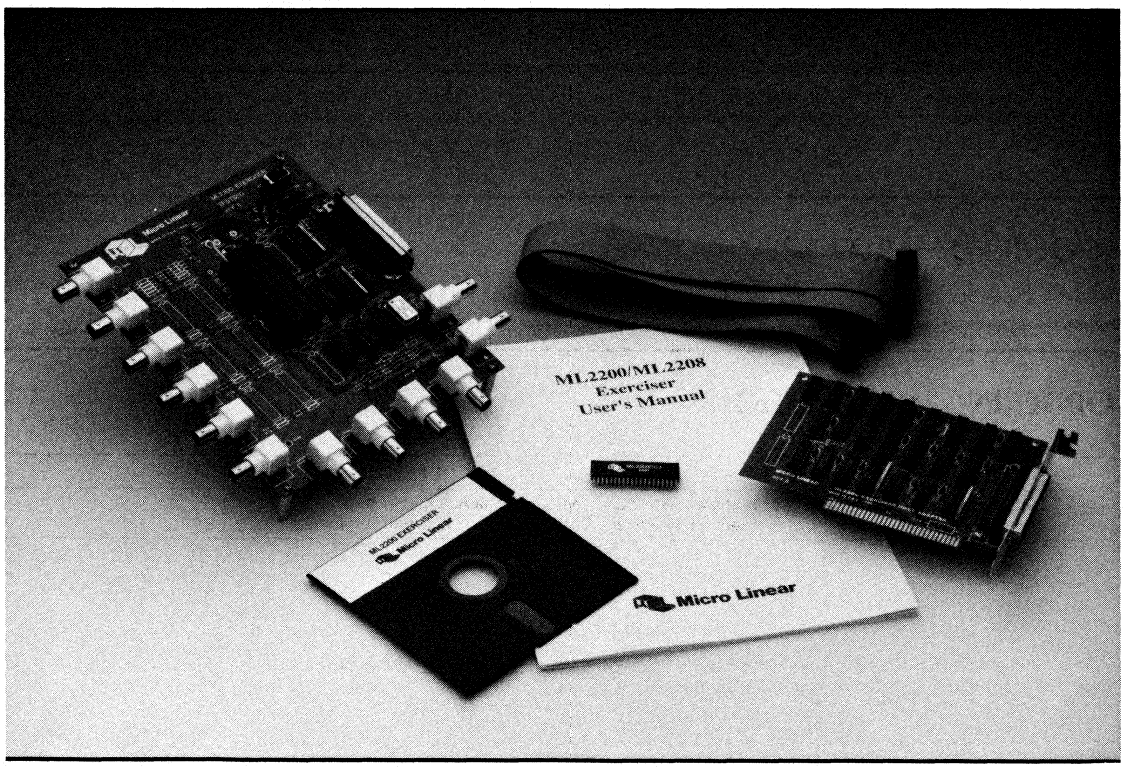
The Exerciser includes a hardware Testbed with prototyping board area, a Host Adapter Card which plugs into the IBM PC, XT, AT and compatibles, a ML2200 or ML2208 Data Acquisition Peripheral, and a user friendly interactive software package.

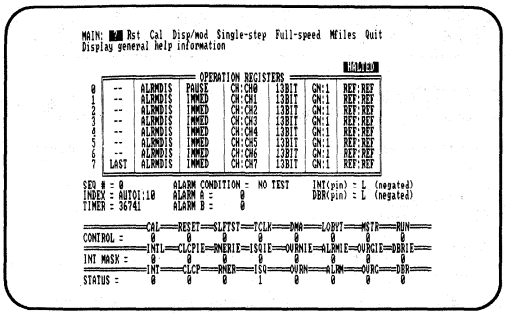
The interactive software is menu driven, providing helpful comments at each level. The complete operation of the ML2200, ML2208 can be explored including all possible register configurations. Once the registers are configured as desired, the part maybe run at full speed. Break conditions maybe setup to exit out of the run mode, and once again examine the registers.

FEATURES

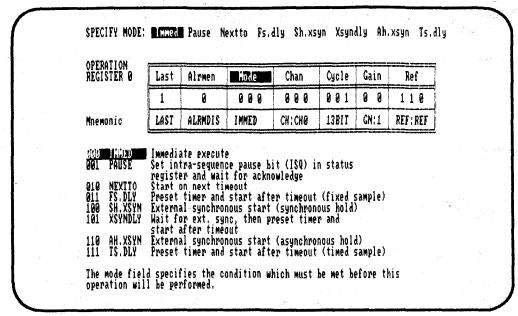
- On-Chip registers may be viewed and modified directly
- Testbed brings out all I/O signals and provides breadboard area for user specific circuits
- Full-speed operation captures data into a 20K word buffer in the PC
- 20K word buffer can be displayed graphically or in table form
- Single Step Operation
- Runs in an IBM PC, XT, AT or PC compatible Host

While the ML2200 is in the run mode, the A/D converted data is saved in a 20K word buffer in the PC's RAM memory. The data in the 20K word buffer can be displayed either graphically or in a table form for closer examination.

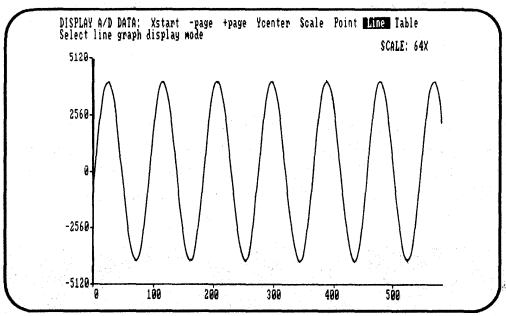




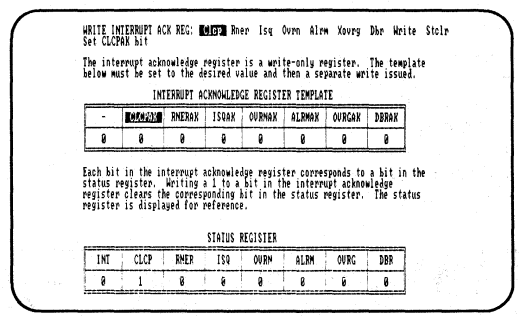
The main menu of the ML2200, ML2208 Exerciser software displays a summary of all of the registers on the chip. The contents of the Operation Registers are displayed in mnemonics while the contents of the timer and alarm registers are displayed in decimal. The top of the screen provides the main menu.



The Disp/mod menu allows individual access to each register for display or modification. The above screen shows how to modify the operation registers which changes the Instruction RAM.



After the data has been captured at full speed and stored in the 20K word buffer, it can be displayed in a table form or in graphic form as shown above.



Each bit can be individually modified for step by step programming. The above screen displays the Interrupt Acknowledge register and Status register.

REQUIRED HARDWARE

IBM PC, XT, AT or compatible, 1 floppy disk drive, 192K bytes of memory and a CGA, EGA or compatible graphics card.

ORDERING INFORMATION

PART NUMBER	DESCRIPTION
ML2200EX	Exerciser System and a ML2200 Data Acquisition Peripheral
ML2208EX	Exerciser System and a ML2208 Data Acquisition Peripheral

ML2221

Serial Peripheral Interface (SPI) 12-Bit Plus Sign A/D Converter with S/H

GENERAL DESCRIPTION

The ML2221 is a member of Micro Linear's 12-bit plus sign CMOS A/D converter family utilizing a self calibrating algorithmic SAR technique. All errors of the sample-and-hold are accounted for in the analog-to-digital converter's accuracy specification.

These A/D converters have a maximum nonlinearity error over temperature of ±0.009% or ±0.012% of minus full scale to plus full scale.

The serial interface is compatible with industry standard serial interfaces. The ML2221 has 4 modes of operation: gated serial data clock, gated chip select, chip select to initiate conversion with serial out data controlled by ML2221, and free run mode.

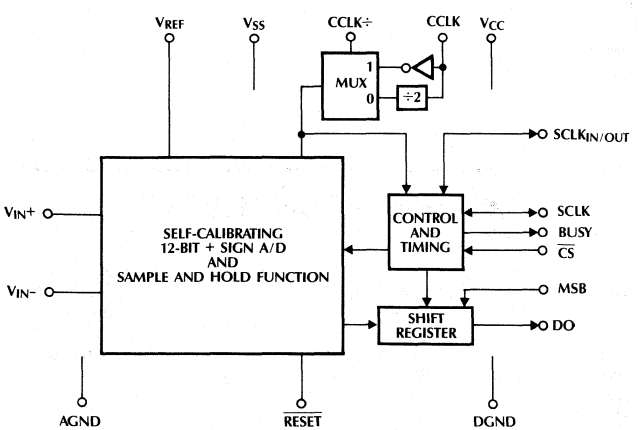
The serial interface allows either MSB or LSB first data with 2's complement output coding. For easy interface to microprocessors and shift registers the output data word is 16 bits.

FEATURES

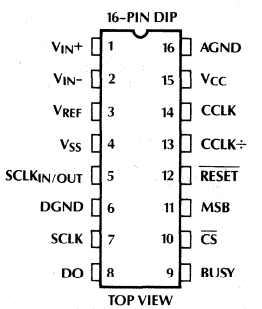
- Nonlinearity error ±¾ LSB and ±1 LSB max
- Conversion time (including S/H acquisition) 44μs max
- Harmonic distortion 0.01%
- No missing codes
- Self calibrating — maintains accuracy over time and temperature
- Inputs withstand |7V| beyond supplies
- Bipolar –5V to +5V analog input range
- Controlled or free run operation
- Direct 4-wire interface to μP (MPU) with synchronous serial formats
- 0°C to +70°C, –40°C to +85°C temperature range
- 16-pin DIP

2

BLOCK DIAGRAM



PIN CONNECTION



PIN DESCRIPTION

PIN NO.	NAME	FUNCTION
1	$V_{IN}+$	Positive Differential Analog Input; range = $V_{SS} \leq V_{IN} + \leq V_{CC}$, $\lvert(V_{IN}+) - (V_{IN}-)\rvert \leq V_{REF}$.
2	$V_{IN}-$	Negative Differential Analog Input; range = $V_{SS} \leq V_{IN} - \leq V_{CC}$, $\lvert(V_{IN}+) - (V_{IN}-)\rvert \leq V_{REF}$.
3	V_{REF}	Voltage Reference Input; referenced to analog ground.
4	V_{SS}	Negative Supply -5V ± 5%; decouple to AGND.
5	$SCLK_{IN/OUT}$	SCLK mode select $SCLK_{IN/OUT}$ = 5V; SCLK is an input serial CLK. $SCLK_{IN/OUT}$ = 0V; SCLK is an output serial CLK.
6	DGND	Digital Ground.
7	SCLK	Bi-Directional Serial Data Clock. Serial data always changes with the clock present at SCLK.
8	DO	Data Out. Digital output which contains result of A/D conversion. The serial data is clocked out on falling edges of SCLK.
9	BUSY	Three-state active high BUSY status output. Normally low. Goes high to indicate that a conversion is in progress; de-asserted when conversion is complete and data is available from the conversion just completed. A pulldown resistor is recommended on this pin.
10	$\overline{CS}$	Active Low Chip Select, starts a conversion and brings the BUSY and DO out of the three-state mode. $\overline{CS}$ is used in modes where conversion or transmission timing is controlled; held low in gated SCLK and FREERUN modes.
11	MSB	Most Significant Bit is transmitted first if MSB is tied to V_{CC}; Least Significant Bit transmitted first if MSB is tied to DGND.
12	$\overline{RESET}$	Active Low Reset. The RESET period is set by the time constant of the internal 50K pull up resistor and an external capacitor. After the RESET period the converter will be ready for accepting requests or will automatically start conversions/transmissions based upon the mode.
13	CCLK÷	Sets CCLK equal to internal clock if tied to 5V. If tied to 0V the internal clock equals CCLK/2. With CCLK equal to the internal CLK the user can synchronize to all internal timing events, although CCLK duty cycle must be controlled to meet the minimum clock high and low times specified.
14	CCLK	Clock Input. Internal clock can be generated by tying a crystal from this pin to DGND or applying a clock directly to the pin.
15	V_{CC}	Positive Supply. +5V ± 5% decouple to AGND.
16	AGND	Analog Ground 0 Volts. Common mode reference point of the internal differential circuitry.

ABSOLUTE MAXIMUM RATINGS
(Note 1)

Supply Voltage (V_{CC}) 6.0V
Negative Supply Voltage (V_{SS}) ..... -6.0V
Voltage at Analog Inputs ..... V_{SS} - 7V to V_{CC} + 7V
Voltage at V_{REF} ..... V_{SS} - 7V to V_{CC} + 7V
Input Current per Digital Pin ..... ±10mA
Input Current at Analog Inputs ..... ±20mA
Storage Temperature Range ..... -65°C to +150°C
Package Dissipation at 25°C (Board Mount) 875mW
Lead Temperature (soldering 10 seconds)
Dual-In-Line Package (Molded) ..... 260°C
Dual-In-Line Package (Ceramic) ..... 300°C

OPERATING CONDITIONS
(Note 2)

Temperature Range ..... $T_{MIN} \leq T_A \leq T_{MAX}$
ML2221BIJ, ML2221CIJ ..... -40°C to +85°C
ML2221BCP, ML2221CCP ..... 0°C to +70°C
Supply Voltage (V_{CC}) ..... $4.5V_{DC}$ to $6.0V_{DC}$
Negative Supply Voltage (V_{SS}) ..... $-4.5V_{DC}$ to $-6.0V_{DC}$
Reference Voltage (V_{REF}) ..... V_{CC}

ELECTRICAL CHARACTERISTICS

The following specifications apply for V_{CC} = +5V ± 5%, V_{SS} = -5V ± 5%, V_{REF} = +4.75V, V_{IN}- = AGND, V_{IN}+ = -4.75V to +4.75V, T_A = T_{MIN} to T_{MAX} unless otherwise specified.

PARAMETER	NOTES	CONDITIONS	ML2221BIJ, ML2221CIJ			ML2221BCP, ML2221CCP			UNITS
			MIN	TYP (Note 3)	MAX	MIN	TYP (Note 3)	MAX	
Converter Characteristics									
Linearity Error ML2221BXX ML2221CXX	4	f_{CCLK} = 0.1 ≤ 5MHz			 ±¾ ±1			 ±¾ ±1	 LSB LSB
Unadjusted Zero Error ML2221BXX ML2221CXX	4				 ±¾ ±2			 ±¾ ±2	 LSB LSB
Unadjusted Positive and Negative Full-Scale Error	4				±5			±4	LSB
Zero Error Temperature Coefficient				0.5			0.5		ppm/°C
Gain Temperature Coefficient				10			10		ppm/°C
Common Mode Rejection	5, 6		80			80			dB
Analog Input Source Resistance	4				2			2	kΩ
Analog Input Range	4	V_{IN}+ Referred to V_{IN}-	$-V_{REF}$		$+V_{REF}$	$-V_{REF}$		$+V_{REF}$	V
Analog Input Leakage Current	4				100			100	nA
Voltage Reference Input Source Impedance	4				0.5			0.5	kΩ
Reference Input Leakage Current	4				100			100	nA
Digital and DC Characteristics									
Power Supply Current I_{CC}, V_{CC} I_{SS}, V_{SS}	4			 30 18	 50 30		 30 18	 50 30	 mA mA
Power Supply Rejection V_{CC} V_{SS} 	7	 DC DC to 25kHz DC DC to 25kHz		 80 50 80 50			 80 50 80 50		 dB dB dB dB
V_{ILCLK}, Clock Input Low Voltage	4				0.8			0.8	V
V_{IHCLK}, Clock Input High Voltage	4		3.5		V_{CC}	3.5		V_{CC}	V
I_{L1}, Input Leakage Current (CCLK)	4	AGND ≤ V_{IN} ≤ V_{CC}			±200			±200	µA
V_{IL}, Input Low Voltage	4				0.8			0.8	V
V_{IH}, Input High Voltage	4		2.0		V_{CC}	2.0		V_{CC}	V
V_{OL}, Output Low Voltage	4	I_{OL} = 2.0mA			0.45			0.45	V
V_{OH}, Output High Voltage	4	I_{OH} = -400µA	2.4			2.4			V
I_L, Input Leakage Current (except CLK)	4	AGND ≤ V_{IN} ≤ V_{CC}			±10			±10	µA
I_{HI-Z}, Output Leakage Current	4	$\overline{CS}$ = V_{IH}			±10			±10	µA
C_I, Input Capacitance (all digital inputs)	5			10			10		pF
C_O, Output Capacitance	5			10			10		pF

2

ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	NOTES	CONDITIONS		MIN	TYP (Note 3)	MAX	UNITS
AC Electrical Characteristics (Note 8)								
t_C	Conversion Time	4, 9	f_{CCLK} = 5MHz (CCLK÷ = "0")		44			µs
	Sample and Hold Acquisition	4, 9	f_{CCLK} = 5MHz (CCLK÷ = "0")				3.2	µs
f_{CCLK0}	Clock Frequency	5, 9	Crystal (CCLK÷ = "0")		3		5	MHz
			Driven (CCLK÷ = "0")		.1		5	MHz
f_{CCLK0}	Clock Width	5, 9	Driven (CCLK÷ = "0")	High	50			ns
				Low	50			ns
f_{CCLK1}	Clock Frequency	5	Driven (CCLK÷ = "1")		0.5		(Note 10)	MHz
f_{CCLK1}	Clock Width	5	Driven (CCLK÷ = "1")	High	150			ns
				Low	150			ns
t_{CSB}	$\overline{CS}$ Low to BUSY Driven	4					85	ns
$t_{CSB}HZ$	$\overline{CS}$ High to BUSY, Hi-Z	4					85	ns
$t_{CSB}A$	$\overline{CS}$ Low to BUSY	5	$\overline{CS}$, $SCLK_{INT}$ or $SCLK_{EXT}$				270	ns
$t_{SCLKB}A$	SCLK High to BUSY	5	Gated SCLK				270	ns
$t_{CCLKB}D$	CCLK Low to BUSY, Deassert	5					160	ns
$t_{SCLK, DO}$	Serial Clock Low to DO Valid/Hold	4					190	ns
$t_{CS, DO}$	$\overline{CS}$ Low to DO Driven	4					85	ns
$t_{CS, DO}HZ$	$\overline{CS}$ High to DO Hi-Z	4					85	ns
$t_{CS, CCLK↑}$	$\overline{CS}$ Low Setup Time to CCLK↑	4	Immediate Conversion Start		0			ns
$t_{CS, SCLK}$	$\overline{CS}$ Low Setup to SCLK Low for No-Delay Data Transmit	5					75	ns
$t_{CCLK, SCLK}$	CCLK to SCLK Output Delay	5	$SCLK_{IN/OUT}$ = "0"				225	ns

Note 1: Absolute maximum ratings are limits beyond which the life of the integrated circuit may be impaired. All voltages unless otherwise specified are measured with respect to ground.

Note 2: 0°C to +70°C and –40°C to +85°C operating temperature range devices are 100% tested with temperature limits guaranteed by 100% testing, sampling, or by correlation with worst-case test conditions.

Note 3: Typicals are parametric norm at 25°C.

Note 4: Parameter guaranteed and 100% production tested.

Note 5: Parameter guaranteed. Parameters not 100% tested are not in outgoing quality level calculation.

Note 6: Common mode rejection is the ratio of the change in zero error to the change in common mode input range.

Note 7: Power supply rejection is the ratio of the change in zero error to the change in power supply voltage.

Note 8: All parameters measured from 0.8V to 2.0V, C_L = 50pF.

Note 9: Maximum frequency is $1/t_{CLK1}$ (high) + t_{CLK1} (low) + rise + fall times, which must be ≤ 2.5 MHz.

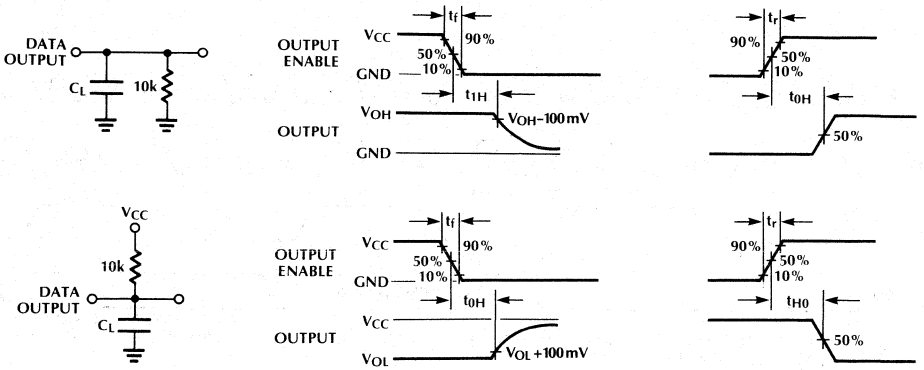


Figure 1. High Impedance Test Circuits and Waveforms

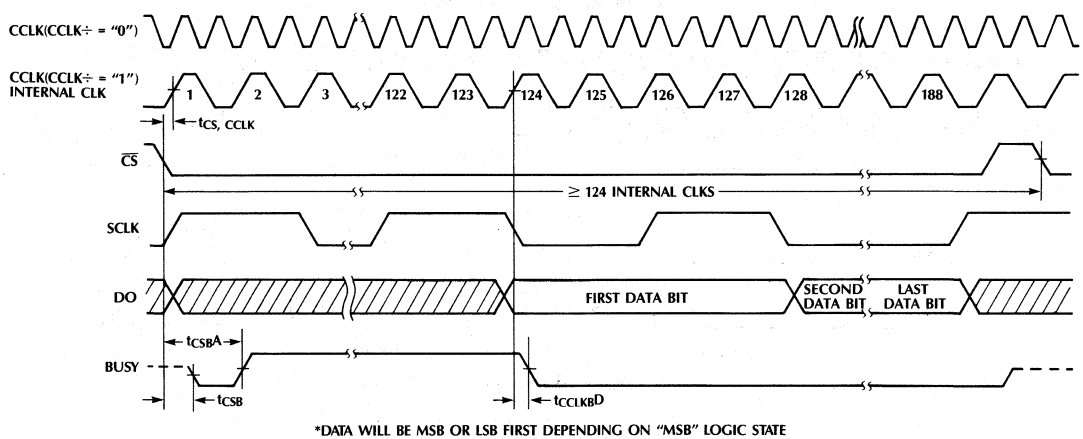


Figure 2. $\overline{CS}$, SCLK Sourced Mode

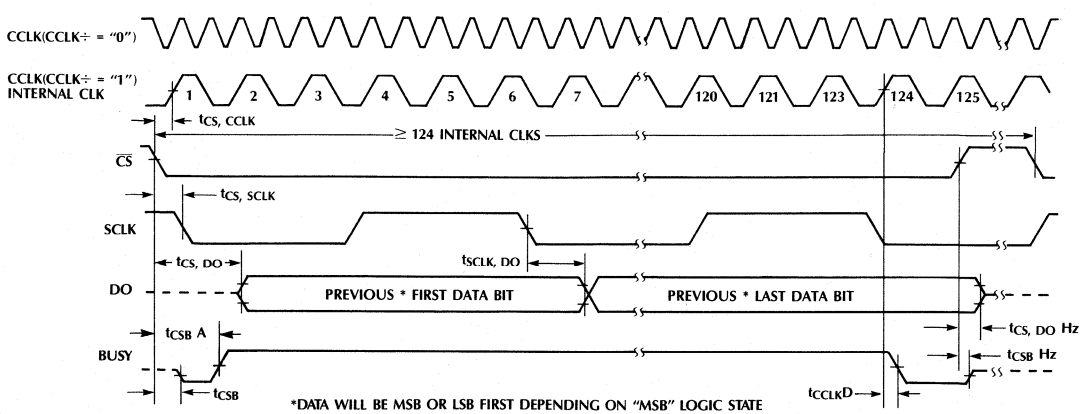


Figure 3. $\overline{CS}$, SCLK External Mode

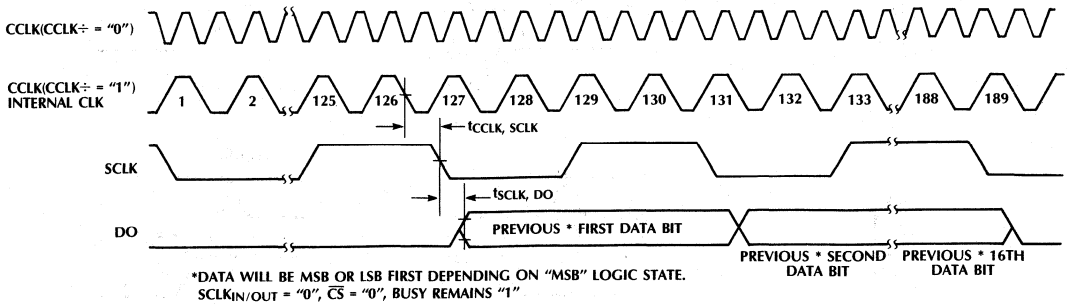


Figure 4. FREERUN Mode

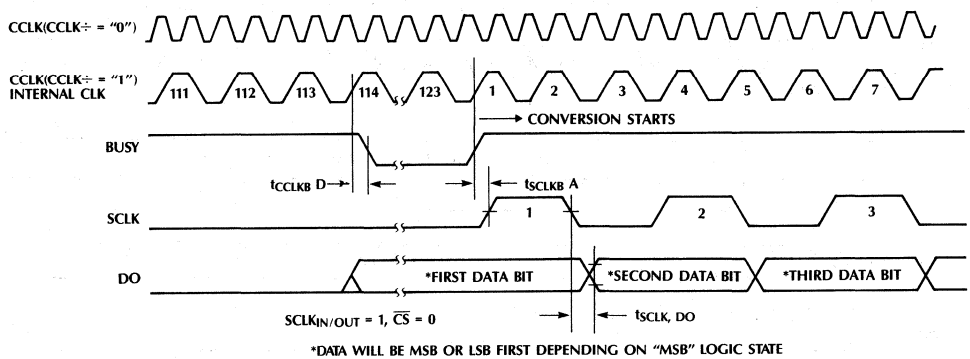


Figure 5. Gated SCLK Mode

1.0 FUNCTIONAL DESCRIPTION

1.1 ALGORITHMIC A/D CONVERTER

Micro Linear's algorithmic converter uses a successive approximation technique. Most of today's successive approximation converters use a DAC to feedback the approximated signal, however this technique requires more circuitry than algorithmic converters. In addition the values of all of the resistors or capacitors in the DAC must be matched to within the accuracy of the converter. This is difficult beyond 10 bits unless trimming is used. An algorithmic converter uses less circuitry and is more easily trimmed. Micro Linear's algorithmic converter is implemented using a 2x amplifier, a sample/hold amplifier and a comparator as shown in Figure 6.

The input sample is first multiplied by two then compared to the reference voltage. If the 2x input voltage is greater than the reference, the MSB is a 1 and the reference voltage is subtracted from the 2x input voltage. The remainder is stored in the sample and hold. If the 2x input voltage is less than the reference, the MSB is a 0 and the 2x input voltage is stored in the sample and hold. This process repeats again, however now the sample and hold voltage is multiplied by 2.

The algorithm involves multiplication by 2, comparison, and possibly subtraction. Referring to Figure 6, the algorithm for the circuit can be described as follows:

Step 1 If $(2 \times V_{IN}) - V_{REF} \geq 0$
then MSB = 1
$(2 \times V_{IN}) - V_{REF} \rightarrow S/H$
else MSB = 0
$(2 \times V_{IN}) \rightarrow S/H$

Step 2 If $(2 \times S/H) - V_{REF} \geq 0$
then next bit = 1
$(2 \times S/H) - V_{REF} \rightarrow S/H$
else next bit = 0
$(2 \times S/H) \rightarrow S/H$

Step 3 Repeat Step 2 until conversion complete.

Since the A/D converter handles bipolar inputs, negative inputs are handled slightly differently using the same principle.

1.1.1 Self Calibration

In order to maintain integral and differential linearity in an algorithmic converter, two critical parameters need to be controlled, loop offsets and the gain of the loop. Loop offsets are automatically nulled before each conversion using auto-zeroing circuitry on both the sampling amplifier and the 2x amplifier. The gain of the loop is adjusted using self calibration.

Self calibrating the algorithmic converter, once the offsets have been nulled, is performed by measuring the 2x gain of the loop and adjusting it. The gain can be measured by converting the reference voltage at the input as well as the reference (V_{REF}/V_{REF}), and examining the output code. Converting V_{REF} should yield plus full scale, since V_{REF}/V_{REF} should equal 1. If the gain of the loop is slightly less than 2, the resulting LSB of the conversion will be "0". If the magnitude bits of the resulting conversion are all "1s", the gain may be too great, therefore the gain is reduced to the point where the threshold of the LSB is reached.

Adjustment of the 2x gain is done with the binary weighted trim capacitor arrays connected to each of the 2C input capacitors. A small value of capacitance is either added to or subtracted from the 2C input caps until the gain of the loop is within 13-bit accuracy.

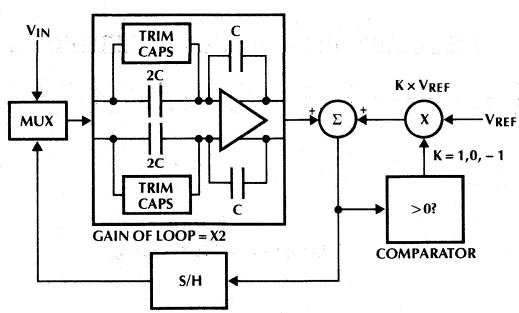


Figure 6. Self Calibrating A/D Converter

1.1.2 Conversion Times

The following table lists the conversion times which include the sample and hold acquisition time.

OPERATION MODE	INTERNAL CLOCKS*
$\overline{CS}$, SCLK External	124
$\overline{CS}$, SCLK Sourced	124
FREERUN	110
Gated SCLK	124

1.1.3 Sample and Hold Timing

Figure 8 shows the internal timing for the sample and hold circuitry. The relationship between the start of conversion and the input channel going into sample mode is fixed at 6 internal clocks*, regardless of the start mode. Six internal clocks after the start of conversion the sample and hold is switched into the sample mode, placing two 9pF capacitors in parallel with the input pins; one on $V_{IN}+$ and one on $V_{IN}-$. The sample switch is kept in the sample mode for 8 internal clocks (3.2μs at a 5MHz external clock), then placed in the hold mode. During the next 2 internal clocks the charge on the sample and hold is transferred into the A/D, after which the V_{REF} pin is sampled for 8 internal clocks.

1.2 ANALOG INPUTS

1.2.1 Differential Inputs and Common Mode Rejection

The differential inputs of the ML2221 eliminate the effects of common mode input noise (60Hz for example), as $V_{IN}+$ and $V_{IN}-$ are sampled at the same time.

* For a description of internal clocks see Clock section.

1.2.2 Noise

The leads to the analog inputs should be kept as short as possible to minimize output noise. Noise as well as digital clocks can couple into the inputs and cause errors. Input filters can be used to reduce the effects of these sources.

1.2.3 Power Supply Decoupling

Low inductance tantalum capacitors of 1μF or greater and 0.01μF disc ceramic capacitors are recommended for bypassing V_{CC} as well as V_{SS} to AGND. These capacitors should be placed close to the V_{CC} and V_{SS} pins.

1.3 CONVERTER CLOCK

The CCLK input can be driven with an external clock or a crystal referenced to DGND. The crystal must be parallel resonant with minimum capacitive loading. (i.e., no bypass caps should be used and leads should be kept short)

If driven with external clock and if the CCLK÷ pin is tied to V_{CC}, the frequency must be between 50KHz to 2.5MHz with the requirement that clock LOW (t_{CCLKL}) and clock HIGH (t_{CCLKH}) durations must be more than 150ns. If the CCLK÷ pin is tied to ground then the frequency can be from 100Hz to 5.0MHz.

For crystal operation with the divide by two flip flop bypassed, and there is a 30 to 70% variation in duty cycle of the oscillator, the maximum crystal frequency is 2.0MHz to insure that the minimum clock high and low times are greater than 150 nsec.

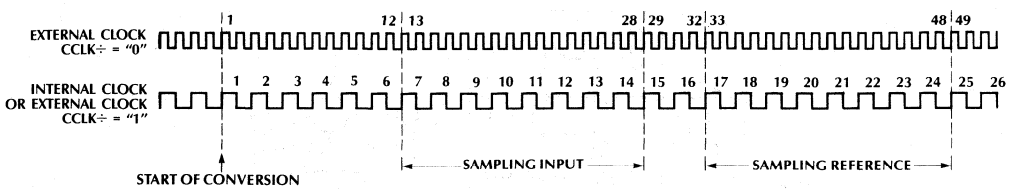


Figure 7. Sample and Hold Timing

1.4 RESET

The $\overline{\text{RESET}}$ pin has an internal 100K pullup resistor. Power supplies must be stable to within a ±5% tolerance before the reset condition is removed.

The active low hardware reset can be performed by a capacitor value (usually >6μF) tied to the $\overline{\text{RESET}}$ pin or by driving it with the system reset signal.

1.5 DIGITAL INTERFACE

All four synchronous interface modes of operation are determined by $\overline{\text{CS}}$ during reset period as follows:

Logic Level of $\overline{\text{CS}}$ During Reset	SCLK Mode Select ($SCLK_{IN/OUT}$)	Serial Interface Mode
0	0	FREERUN
0	1	Gated SCLK
1	0	$\overline{\text{CS}}$, SCLK Sourced
1	1	$\overline{\text{CS}}$, SCLK External

After the reset time, the $SCLK_{IN/OUT}$ pin can be changed to switch between either (FREERUN and Gated SCLK) or ($\overline{\text{CS}}$, SCLK Sourced and $\overline{\text{CS}}$, SCLK External).

The logic level of $\overline{\text{CS}}$ will not change the mode of operation of the ML2221 once the mode of operation is programmed during the RESET period.

1.5.1 $\overline{\text{CS}}$, SCLK External Mode

$\overline{\text{CS}}$ starts a conversion. The SCLK is continuously driven into the ML2221 and data from the previous conversion is shifted out at the SCLK rate starting at the first SCLK falling edge from the $\overline{\text{CS}}$ assertion. $\overline{\text{CS}}$ is normally kept low for all 16 bits of data, but can be brought back high after the desired number of bits have been shifted out. Conversions should be requested every 124 internal converter clocks.

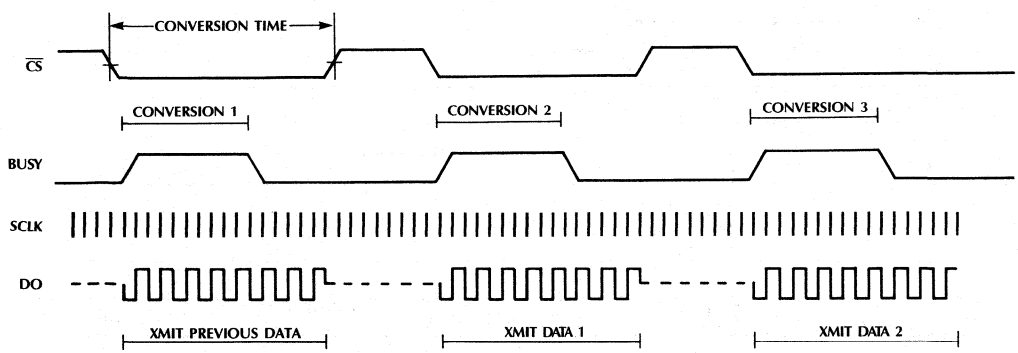
It takes 110 internal clocks to convert an analog signal into 13 bits of data plus 13 more clock periods to make data available. At a 5.0MHz clock and CCLK÷ = 0V, the maximum conversion rate is 49.6 microseconds or 124 internal converter clocks.

When $\overline{\text{CS}}$ is asserted (LOW) a conversion begins and the DO output becomes active. The ML2221 is ready to shift out the data serially.

The BUSY output is in the high impedance state when the ML2221 is not selected. When $\overline{\text{CS}}$ input goes low, the BUSY output is driven high or low depending on if a conversion is in progress. Once a conversion begins, BUSY is held active for 123 internal converter clocks.

The DO output is high impedance when the ML2221 is not selected. When $\overline{\text{CS}}$ input goes low, it is driven with the first bit of data initially, and then begins to put out all subsequent data bits on each FALLING edges of the serial clock (SCLK). Data is always output in 16 bit format: if the LSB is output first, the data is sign extended after 13 bits; if the MSB is output first, the data is zero-filled after 13 bits. DO remains driven as long as $\overline{\text{CS}}$ remains low.

a. Serial Transmission < Conversion Time



NOTE: CONVERSION TIME EQUALS 124 INTERNAL CLOCK OR CCLK'S IF CCLK÷ = "1"

Notes:
1. Use 10k pulldown resistor on BUSY pin to get "true" convert busy.
2. If $\overline{\text{CS}}$ is brought high in the middle of a serial data transmission, the data transmission is aborted and the data is reloaded into the output shifter.

Figure 8. $\overline{\text{CS}}$, SCLK External Mode

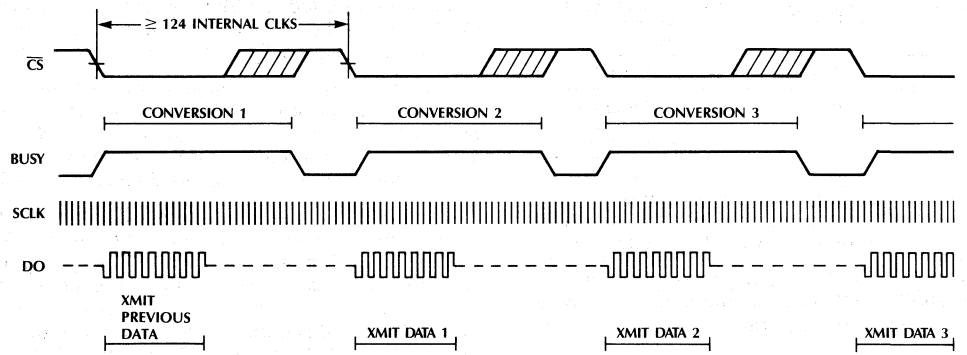
1.5.2 $\overline{CS}$, SCLK Sourced Mode

$\overline{CS}$ starts a conversion. At the end of the conversion (123 internal converter clocks after start of conversion), the chip outputs 16 bits of data and 16 SCLKS at the rate of 4 internal converter clocks per bit. Chip select is normally held low for the entire conversion and transmission sequence, although $\overline{CS}$ can be brought back high during the serial data transmission after the desired number of bits have been shifted out. This mode always shifts out data from the current conversion.

It takes 110 internal clocks to convert an analog signal into 13 bits of data plus 13 more clock periods to make data available. To send out 16 bits serially, 64 internal clocks are needed to complete a transmission. At a 5.0MHz clock and CCLK÷ = 0V, the maximum conversion rate is 75.2 microseconds or 188 internal converter clocks. The maximum frequency for selecting the ML2221 is 18.8KHz.

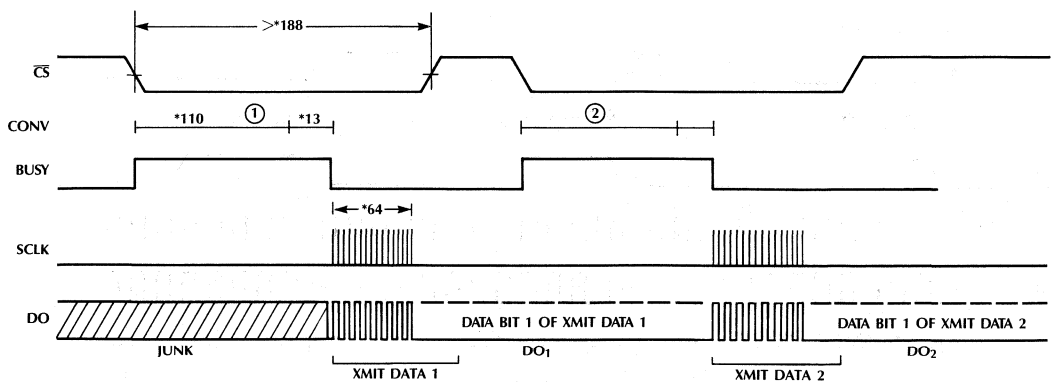
When $\overline{CS}$ is asserted (LOW) a conversion begins and the DO output becomes active. The ML2221 is ready to shift out the data serially after 124 internal clocks.

b. Serial Transmission > Conversion Time



Notes:
1. Use 10K pulldown resistor on BUSY pin to get "TRUE" convert BUSY status.
2. If $\overline{CS}$ is brought HIGH in the middle of a serial data transmission, the data transmission is aborted and the data is reloaded into the output shifter.

Figure 8. $\overline{CS}$, SCLK External Mode



*NUMBER OF INTERNAL CONVERTER CLOCKS OR CCLKS WITH CCLK÷ = "1"

Notes:
1. Use 10K pulldown resistor on BUSY pin to get "TRUE" convert BUSY status.
2. If $\overline{CS}$ is brought HIGH in the middle of a serial data transmission, the data transmission is aborted and the data is reloaded into the output shifter.

Figure 9. $\overline{CS}$, SCLK Sourced Mode

1.5.3 FREERUN Mode

The FREERUN mode executes continuous back-to-back conversions at the rate of 110 internal converter clocks per conversion, and outputs 16 bits of data and 16 corresponding SCLKS at the rate of 4 internal converter clocks per bit. The ML2221 immediately begins converting after reset and starts outputting data after the first conversion. A conversion rate of 44 microseconds is achieved using the maximum SCLK frequency.

In the FREERUN mode, BUSY is always asserted, since the A/D converter is continuously busy. In the FREERUN mode an external shifter or FIFO can be used to store data on the fly and no SCLK input is required.

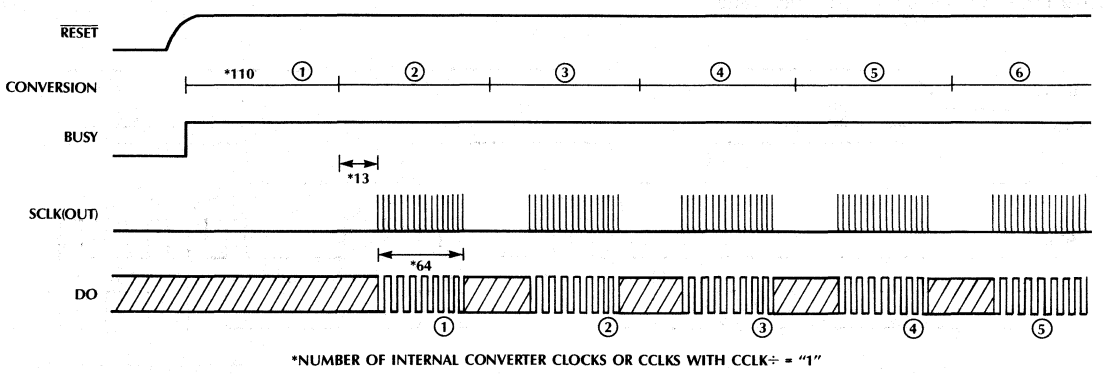
1.5.4 Gated SCLK Mode

In the Gated SCLK mode a burst of 16 clocks at the SCLK input is used to simultaneously shift 16 bits of data out from the previous conversion and start a conversion at the first of the 16 SCLKS. Requests for conversions should be held off for at least 1 conversion time (124 internal converter clocks) after the reset condition is removed. This is to allow the chip to execute one conversion immediately after reset.

In order to maintain proper timing 16 clocks must always be given. Conversion requests should be made once every 124 internal converter clocks.

A conversion begins at the reception of the first SCLK. It takes 110 internal clocks to convert an analog signal into 13 bits of data plus 13 more clock periods to make data available. At a 5.0MHz clock and BYPASS = 0V, the maximum conversion rate is 49.6 microseconds or 124 internal converter clocks. Conversion requests should not be made more often than this number.

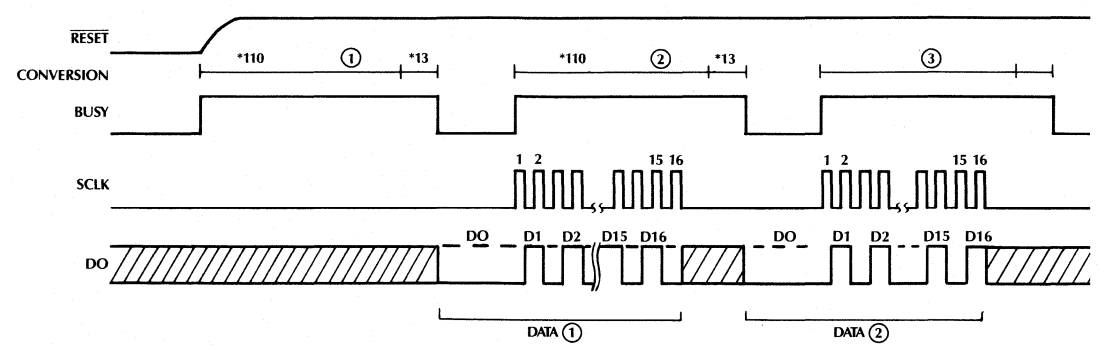
The BUSY output never floats and is asserted at the first SCLK and deasserted after 123 internal converter clocks. BUSY is held active for 123 internal converter clocks. DO is always driven.



Note: DO is always driven.

Figure 10. FREERUN Mode

a. Serial Data Transmission < Conversion Time

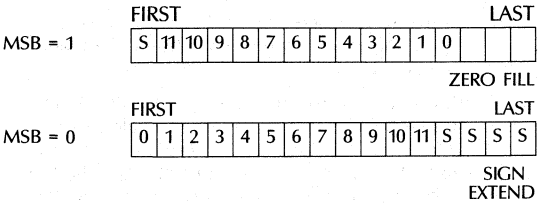


Note: Time from first SCLK↑ to seventeenth SCLK↑ must be greater than 124 internal converter clocks.

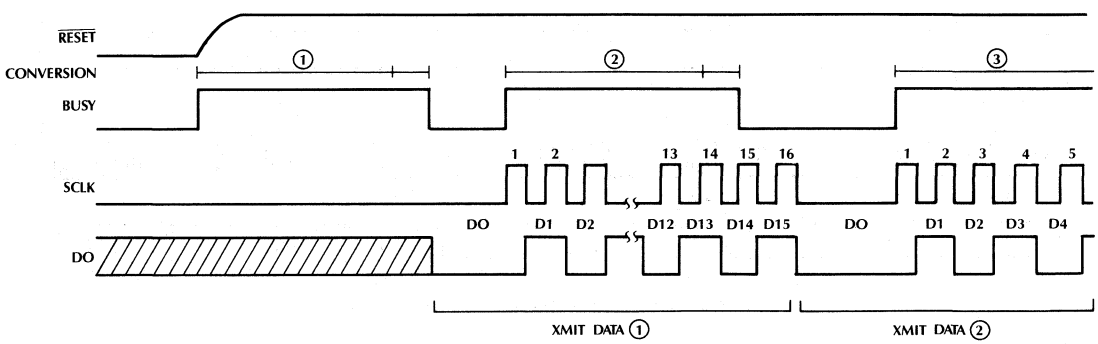
Figure 11. Gated SCLK Mode

1.6 DATA FORMAT

The MSB pin determines if the MSB or LSB data is transmitted first and in the following format. If more than 13 SCLK's occur.



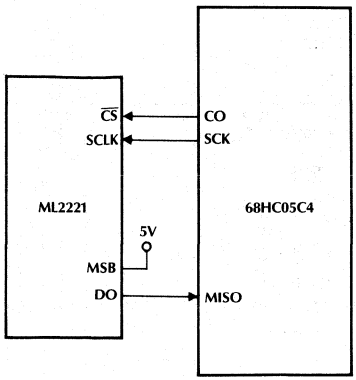
b. Serial Data Transmission > Conversion Time



Note: Time from first SCLK↑ to seventeenth SCLK↑ must be greater than 124 internal converter clocks.

Figure 11. Gated SCLK Mode

APPLICATIONS



START	MNEMONIC	INSTRUCTION
START	BCLRn	Bit 0 Port C goes low ($\overline{CS}$ goes low)
	LDA	Load contents of SPI data register into Acc. (D_{OUT} MSBs)
	STA	Start next SPI cycle
	AND	Clear 3 MSBs of first D_{OUT} word
	STA	Store in memory location A (MSBs)
	TST	Test status of SPIF
	BPL	Loop to previous instruction if not done with transfer
	BSETn	Set B0 of Port C ($\overline{CS}$ goes high)
	LDA	Load contents of SPI data register into Acc. (D_{OUT} LSBs)
	STA	Store in memory location A + 1 (LSBs)

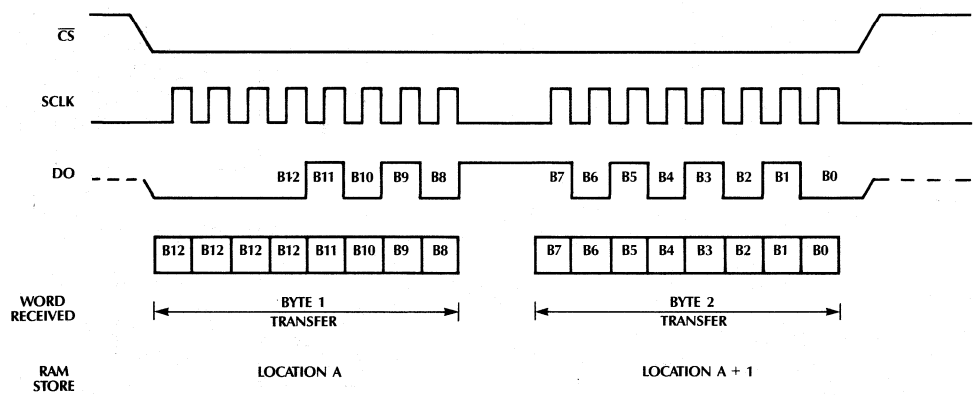


Figure 12. Interfacing to 68HC05C4 with a Dedicated Serial Port

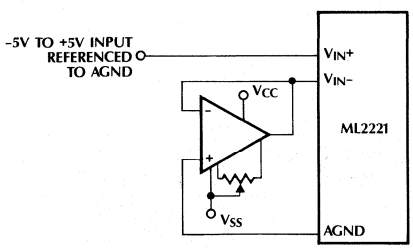


Figure 13. Adjusting Zero Error

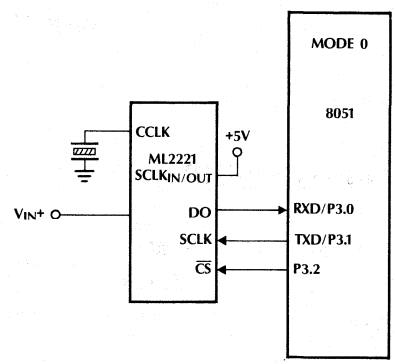


Figure 14. 1 Mbps 8051 Interface

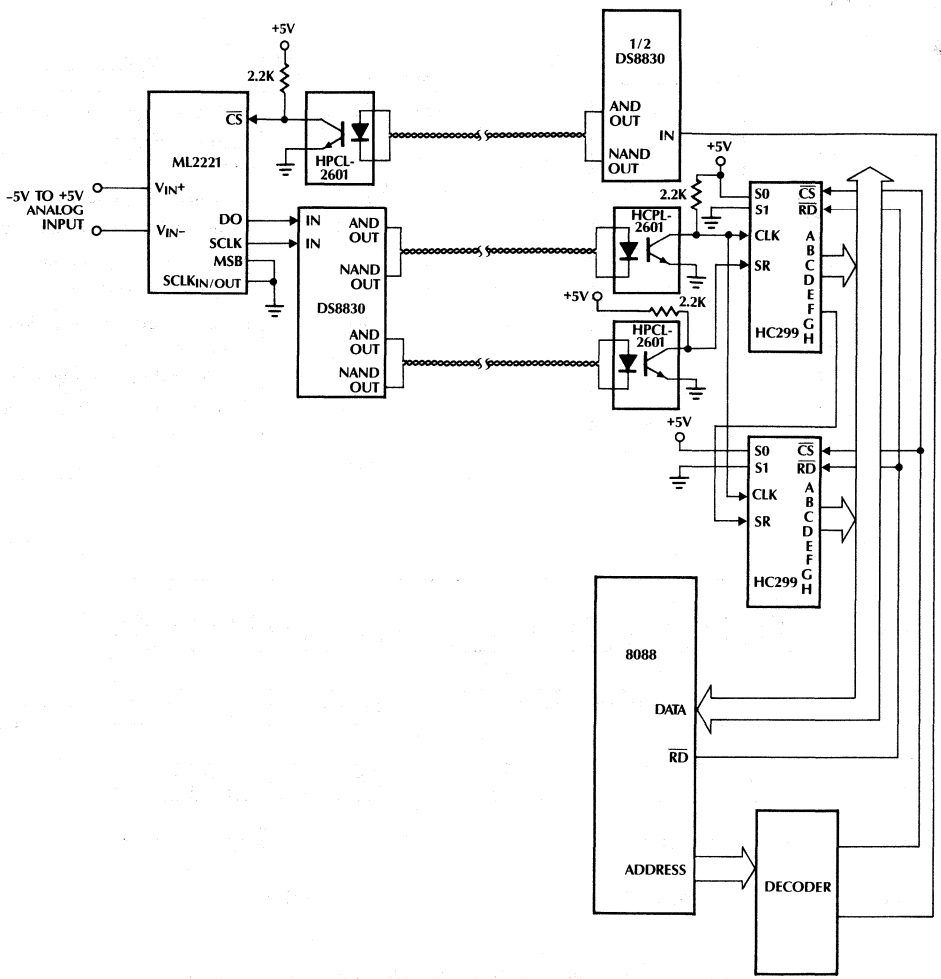


Figure 15. Optical Isolated 8088 Interface

ORDERING INFORMATION

PART NUMBER	LINEARITY ERROR	TOTAL UNADJUSTED ERROR	TEMPERATURE RANGE	PACKAGE
ML2221BCP	±¾ LSB	±1½	0°C to +70°C	MOLDED DIP
ML2221BIJ			-40°C to +85°C	HERMETIC DIP
ML2221CCP	±1 LSB	±2½	0°C to +70°C	MOLDED DIP
ML2221CIJ			-40°C to +85°C	HERMETIC DIP

Micro Linear

ML2222

Serial, CODEC/DSP Interface 12-Bit Plus Sign A/D Converter with S/H

GENERAL DESCRIPTION

The ML2222 is a member of Micro Linear's 12-bit plus sign CMOS A/D converter family utilizing a self calibrating algorithmic SAR technique. All errors of the sample-and-hold are accounted for in the analog-to-digital converter's accuracy specification.

These A/D converters have a maximum nonlinearity error over temperature of ±0.012% or ±0.024% of full scale.

The CODEC serial interface is compatible with the communication industry standard protocol of PCM (Pulse Code Modulation). The ML2222 upon receiving the transmit frame synchronization pulse (FSX), shifts 16 bits of data.

The transmit clock may vary from 64 KHz to 2.048 MHz.

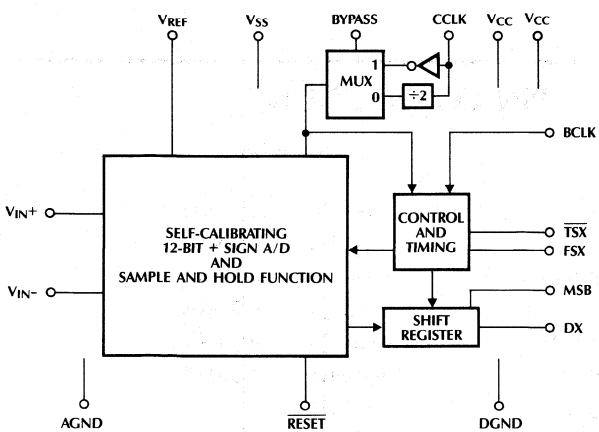
The serial interface allows either MSB or LSB first data with 2's complement output coding. For easy interface to microprocessors and shift registers the output data word is 16 bits.

FEATURES

- Standard communication industry protocol for timing and frame sync
- Transmit clock from 64 KHz to 2.048 MHz
- Nonlinearity error ±½ LSB and ±1 LSB max
- Conversion time (including S/H acquisition) 31.5μs max
- Harmonic distortion 0.01%
- No missing codes
- Self calibrating — maintains accuracy over time and temperature
- Inputs withstand |7V| beyond supplies
- Bipolar –2.5V to +2.5V analog input range
- 0°C to +70°C, –40°C to +85°C temperature range
- 16-pin DIP

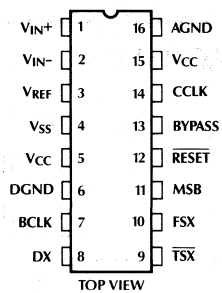
2

BLOCK DIAGRAM



PIN CONNECTION

16-Pin DIP



TOP VIEW

Micro Linear

ML2223

Asynchronous Serial Interface 12-Bit Plus Sign A/D Converter with S/H

GENERAL DESCRIPTION

The ML2223 is a member of Micro Linear's 12-bit plus sign CMOS A/D converter family utilizing a self calibrating algorithmic SAR technique. All errors of the sample-and-hold are accounted for in the analog-to-digital converter's accuracy specification.

These A/D converters have a maximum nonlinearity error over temperature of ±0.012% or ±0.024% of full scale.

For easy interface to microprocessors, the ML2223 is designed to transmit data into RS-232 type ports.

The ML2223 operates in two asynchronous modes of operation. In one mode, the A/D continuously transmits 2 bytes in a 24-bit stream, inserting 8 idle bits between transmissions. The second mode of operation utilizes chip select to start a conversion or transmit the previous conversion result in the 24-bit stream data format. If the CURR input pin is tied high, transmission begins immediately upon receiving a conversion start request. When CURR is low, transmission is started after a new conversion is complete.

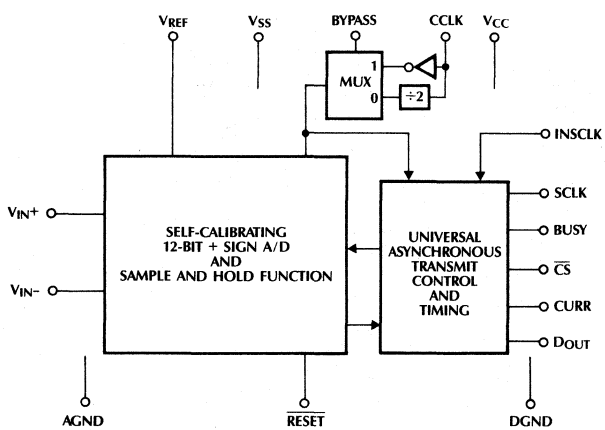
The serial data clock can be generated by the ML2223 or it can be provided by an external source.

The serial interface provides LSB first data with 2's complement output coding.

FEATURES

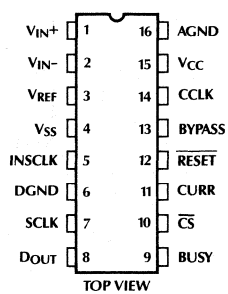
- RS-232 compatible asynchronous interface
- One- or two-wire data transmission
- Continuous or on-command conversions
- Nonlinearity error ±½ LSB and ±1 LSB max
- Conversion time (including S/H acquisition) 35.5μs max
- Bipolar –5V to +5V analog input range with ±5V power supplies
- Harmonic distortion 0.01%
- No missing codes
- Self calibrating — maintains accuracy over time and temperature
- Inputs withstand |7V| beyond supplies
- 0°C to +70°C, –40°C to +85°C temperature range
- Standard .3" 16-pin DIP

BLOCK DIAGRAM



PIN CONNECTION

16-Pin DIP



TOP VIEW

October 1990
PRELIMINARY

ML2230

μP Compatible 12-Bit Plus Sign A/D Converter with Sample and Hold

GENERAL DESCRIPTION

The ML2230 is a member of Micro Linear's 12-bit plus sign CMOS A/D converter family utilizing a self calibrating algorithmic technique. The sample-and-hold, incorporated on the ML2230, has a differential input for noise immunity and power supply rejection. All errors of the sample-and-hold are accounted for in the analog-to-digital converter's accuracy specification.

The ML2230B has a maximum non-linearity error over temperature of 0.018% of full-scale, and the ML2230C and ML2230D have a maximum non-linearity error over temperature of 0.024% of full scale.

Designed to interface to an 8-bit microprocessor bus without additional components, the ML2230 outputs the 13-bit data result in two 8-bit bytes. Data format is 2's complement. All digital signals are fully TTL and CMOS compatible.

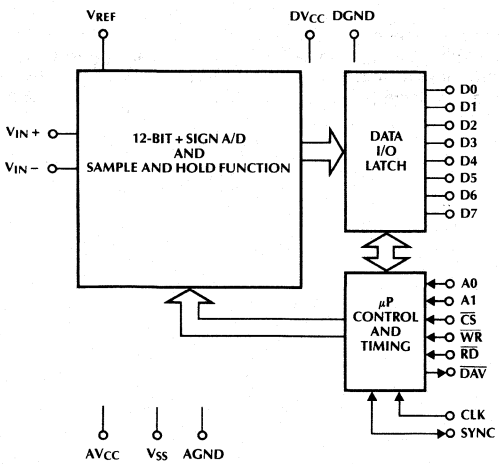
For interfacing to a 16-bit microprocessor bus the ML2233 provides a 13-bit data result.

FEATURES

- Resolution 12-bits + sign
- Conversion time (including S/H acquisition) 31.5μs max
- Sample and hold acquisition 2.3μs max
- Non-linearity error ±¾LSB and ±1LSB max
- Low harmonic distortion 0.01%
- No missing codes
- Self calibrating—maintains accuracy over time and temperature
- Inputs withstand |7V| beyond supplies
- Data transfer options—interrupt, DMA, or polling
- Outputs data in two 8-bit bytes
- Standard 24-pin DIP

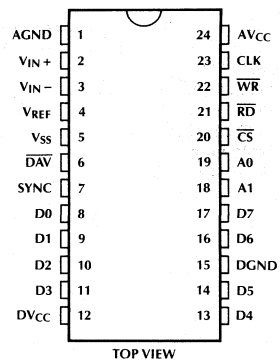
2

BLOCK DIAGRAM



PIN CONNECTIONS

ML2230
24-PIN DIP



TOP VIEW

PIN DESCRIPTION

DIP	PCC	NAME	FUNCTION
1	1	AGND	Analog ground.
2	2	$V_{IN}+$	Positive differential analog input; range = $V_{SS} \le V_{IN}+ \le AV_{CC}$, $\lvert(V_{IN}+)-(V_{IN}-)\rvert \le V_{REF}$.
3	3	$V_{IN}-$	Negative differential analog input; range = $V_{SS} \le V_{IN}- \le AV_{CC}$, $\lvert(V_{IN}+)-(V_{IN}-)\rvert \le V_{REF}$.
4	4	V_{REF}	Voltage reference input; referenced to analog ground.
5	5	V_{SS}	Negative power supply; decouple to AGND.
6	8	$\overline{DAV}$	Data available; indicates a conversion has completed and data is available or calibration completed.
7	9	SYNC	In the slave mode, SYNC is a positive edge triggered input used to start a conversion. In master mode, SYNC is an output and indicates a conversion has occurred.
8	10	D0	Bidirectional data bit.
9	11	D1	Bidirectional data bit.
10	13	D2	Bidirectional data bit.
11	14	D3	Bidirectional data bit.
12	15	DV_{CC}	Digital power supply. Tie to AV_{CC} from same power supply.
13	16	D4	Bidirectional data bit.
14	17	D5	Bidirectional data bit.
15	18, 19	DGND	Digital ground.
16	20	D6	Bidirectional data bit.
17	21	D7	Bidirectional data bit.
18	22	A1	Address for the microprocessor interface to access any one of the four registers.
19	23	A0	Address for the microprocessor interface to access any one of the four registers.
20	24	$\overline{CS}$	Chip select; enables writing to or reading from.
21	25	$\overline{RD}$	Read; enables ML2230 to drive data bus.
22	26	$\overline{WR}$	Write; allows writing into the registers.
23	27	CLK	Clock input. Drive with an external clock or crystal referenced to DGND. The crystal must be parallel resonant with minimum capacitive loading. (i.e., no bypass caps should be used and leads should be kept short.)
24	28	AV_{CC}	Positive analog power supply. Decouple to AGND. Tie to DV_{CC} from same power supply.

ABSOLUTE MAXIMUM RATINGS
(Note 1)

Supply Voltages (AV_{CC} and DV_{CC}) 6.0V
Negative Supply Voltage (V_{SS}) ..... −6.0V
Voltage at Analog
Inputs ..... V_{SS} − 7V to AV_{CC} + 7V
Voltage at V_{REF} ..... V_{SS} − 7V to AV_{CC} + 7V
Input Current per Digital Pin ..... ±10mA
Input Current at Analog Inputs ..... ±20mA
Storage Temperature Range ..... −65°C to +150°C
Package Dissipation @ 25°C 875mW
Lead Temperature soldering,
Dual-In-Line Package (Ceramic) ..... 300°C

OPERATING CONDITIONS (Note 2)

Temperature Range ..... 0°C to 70°C
Supply Voltage (AV_{CC} and DV_{CC}) ..... $4.5V_{DC}$ to $6.0V_{DC}$
Negative Supply Voltage (V_{SS}) ..... $-4.5V_{DC}$ to $-6.0V_{DC}$
Reference Voltage (V_{REF}) 2.60V

ELECTRICAL CHARACTERISTICS

The following specifications apply for V_{CC} = +5V ± 5%, V_{SS} = –5V ± 5%, V_{REF} = +4.75V, V_{IN}– = AGND, V_{IN}+ = –4.75V to +4.75V, T_A = T_{MIN} to T_{MAX} unless otherwise specified.

PARAMETER	NOTES	CONDITIONS	MIN	TYP (Note 3)	MAX	UNITS
Converter Characteristics						
Linearity Error ML2230BXX ML2230CXX ML2230DXX	4	 f_{CCLK} = 0.1 ≤ 7MHz f_{CCLK} = 0.1 ≤ 7MHz f_{CCLK} = 0.1 ≤ 5MHz			 ±¾ ±1 ±1	 LSB LSB LSB
Unadjusted Zero Error ML2230BXX ML2230CXX ML2230DXX	4				 ±¾ ±2 ±2	 LSB LSB LSB
Unadjusted Positive and Negative Full Scale Error	5				±4	LSB
Zero Error Temperature Coefficient				0.5		ppm/°C
Gain Temperature Coefficient				10		ppm/°C
Common-Mode Rejection	5, 6		80			dB
Analog Input Source Resistance	5				2	kΩ
Analog Input Range	4	V_{IN}+ Refer to V_{IN}–	$-V_{REF}$		$+V_{REF}$	V
Analog Input Leakage Current	4				100	nA
Voltage Reference Input Source Impedance	5				0.5	kΩ
Reference Input Leakage Current	4				100	nA
Digital and DC Characteristics						
Power Supply Current AI_{CC}, Analog V_{CC} DI_{CC}, Digital V_{CC} I_{SS}, V_{SS}	4			 30 10 18	 50 30	 mA µA mA
Power Supply Rejection AV_{CC} V_{SS}	7	 DC DC to 25kHz DC DC to 25kHz		 80 50 80 50		 dB dB dB dB
V_{ILCLK}, Clock Input Low Voltage	4				0.8	V
V_{IHCLK}, Clock Input High Voltage	4		3.5		AV_{CC}	V
I_{L1}, Input Leakage Current (CLK)	4	AGND ≤ V_{IN} ≤ AV_{CC}		±200	µA	
V_{IL}, Input Low Voltage	4				0.8	V
V_{IH}, Input High Voltage	4		2.0		DV_{CC}	V
V_{OL}, Output Low Voltage	4	I_{OL} = 2.0mA			0.45	V
V_{OH}, Output High Voltage	4	I_{OH} = –400µA	2.4			V
I_L, Input Leakage Current (except CLK)	4	AGND ≤ V_{IN} ≤ AV_{CC}			±10	µA
I_{HI-Z}, Output Leakage Current (D0–D7)	4	$\overline{RD}$ = $\overline{CS}$ = V_{IH}			±10	µA
C_I, Input Capacitance (all digital inputs)				10		pF
C_O, Output Capacitance (outputs D0 to D7, and DAV)				10		pF

ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER		CONDITIONS		MIN	TYP (Note 3)	MAX	UNITS
AC Electrical Characteristics (Note 8)								
t_C	Conversion Time	4, 9	CLK Mode = 0	f_{CLK} = 7.0MHz f_{CLK} = 5.0MHz	31.5 44.0			µs µs
	Sample and Hold Acquisition	4, 9	CLK Mode = 0	f_{CLK} = 7.0MHz f_{CLK} = 5.0MHz			2.3 3.2	µs µs
f_{CLK0}	Clock Frequency	5, 9	Crystal (CLK Mode = 0) Driven (CLK = Mode 0)		3 1		7 7	MHz MHz
t_{CLK0}	Clock Width	5, 9	Driven (CLK Mode = 0)	High Low	50 50			ns ns
f_{CLK1}	Clock Frequency	5, 10	Driven (CLK Mode = 1)		0.5		(Note 11)	MHz
t_{CLK1}	Clock Width	5, 10	Driven (CLK Mode = 1)	High Low	125 125			ns ns
t_{AD}	Address Stable to Valid Data	4			150			ns
t_{AR}	Address Stable Before Read	4			0			ns
t_{RA}	Address Hold After Read	4			0			ns
t_{RR}	Read Pulse Width	5			150			ns
t_{RD}	Read Access	4					150	ns
t_{1Z}, t_{0Z}	Data Read to Hi-Z	4			0		50	ns
t_{RV}	Recovery Between Two Reads or Writes	5			250			ns
t_{RDCK}	Read to Clock Setup Time	5, 12			40			ns
t_{AW}	Address Stable Before Write	4			0			ns
t_{WA}	Address Hold After Write	4			0			ns
t_{WW}	Write Pulse Width	4			150			ns
t_{DW}	Data Setup Before Write Trailing Edge	4			100			ns
t_{WD}	Data Hold After Write Trailing Edge	4			0			ns
t_{WRCK}	Write to Clock Setup Time	5, 12			40			ns
t_{CKDAV}	Clock to $\overline{DAV}$ Assert	4, 13	C_L = 50pF			120	220	ns
t_{SYNCCK}	SYNC Input to Clock Setup	5, 12			40			ns
t_{SYNCN}	SYNC Input Width	5	(CLK Mode = 0) (CLK Mode = 1)		6 3			$1/f_{CLK0}$ $1/f_{CLK1}$
t_{CKSYNC}	External Clock to SYNC Output Delay	5, 13	C_L = 50pF			150	200	ns
t_{SYNCO}	SYNC Output Pulse Width	5, 13	(CLK Mode = 0) (CLK Mode = 1)				8 4	$1/f_{CLK0}$ $1/f_{CLK1}$
t_{WRDAV}	Write Reg2 to $\overline{DAV}$ Rising Edge	4, 14	C_L = 50pF				170	ns
t_{RDDAV}	Read Reg0 to $\overline{DAV}$ Rising Edge	4, 15	C_L = 50pF				170	ns
t_r, t_f	Rise and Fall		All Inputs				25	ns

Note 1: Absolute maximum ratings are limits beyond which the life of the integrated circuit may be impaired. All voltages unless otherwise specified are measured with respect to ground.
Note 2: Devices are 100% tested with temperature limits guaranteed by 100% testing, sampling or by correlation with worst-case test conditions.
Note 3: Typicals are parametric norm at 25°C.
Note 4: Parameter guaranteed and 100% production tested.
Note 5: Parameter guaranteed. Parameters not 100% tested are not in outgoing quality level calculation.
Note 6: Common mode rejection is the ratio of the change in zero error to the change in common mode input range.
Note 7: Power supply rejection is the ratio of the change in zero error to the change in power supply voltage.
Note 8: All parameters measured from 0.8V to 2.0V, C_L = 100pF.
Note 9: CK1X bit in control register = 0.
Note 10: CK1X bit in control register = 1.
Note 11: Maximum frequency is $1/t_{CLK1}$ (high) + t_{CLK1} (low) + rise + fall times and $\leq$ 3.5MHz.
Note 12: Setup time required for synchronous start of conversion.
Note 13: In CLK mode = 0 (CK1X bit in control register = 0) start of conversion will occur at specified time; or time plus one f_{CLK0} period (see Figure 5).
Note 14: Writing a control register bit 0 with a one will acknowledge the $\overline{DAV}$ condition and de-assert DAV output.
Note 15: In start mode = 1, a read from location "0" will start the next conversion and de-assert the DAV output.

TIMING DIAGRAMS

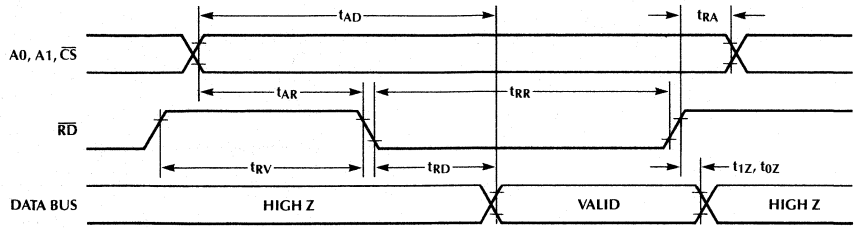


Figure 1. Read Cycle

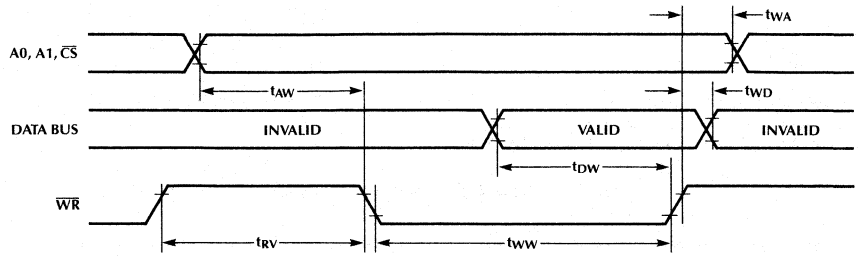
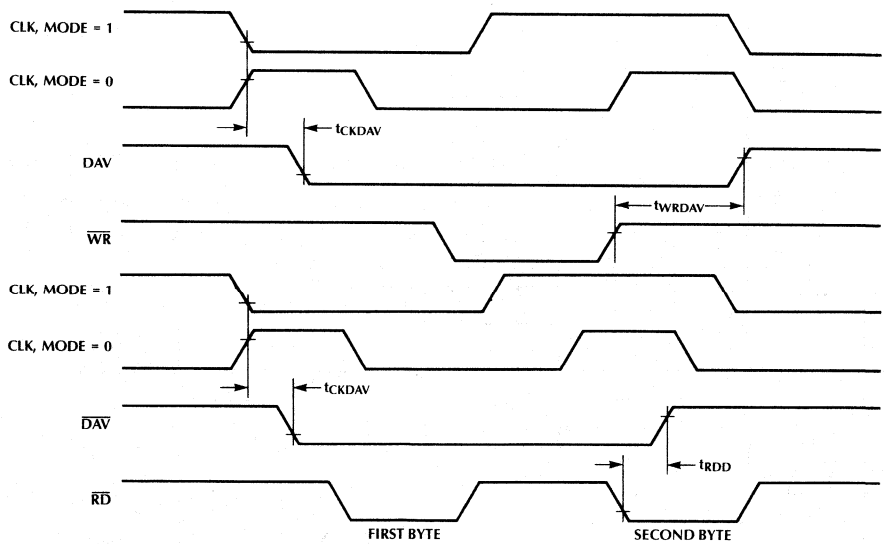


Figure 2. Write Cycle



DAV IS SET AND CLEARED BY INTERNAL CIRCUITRY.
NOTE: DMA BIT IN THE CONTROL REGISTER MUST BE SET FOR THIS OPERATION.

Figure 3. Data Available

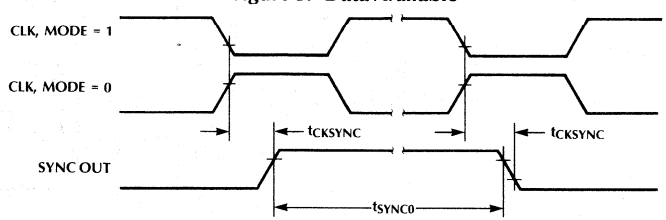
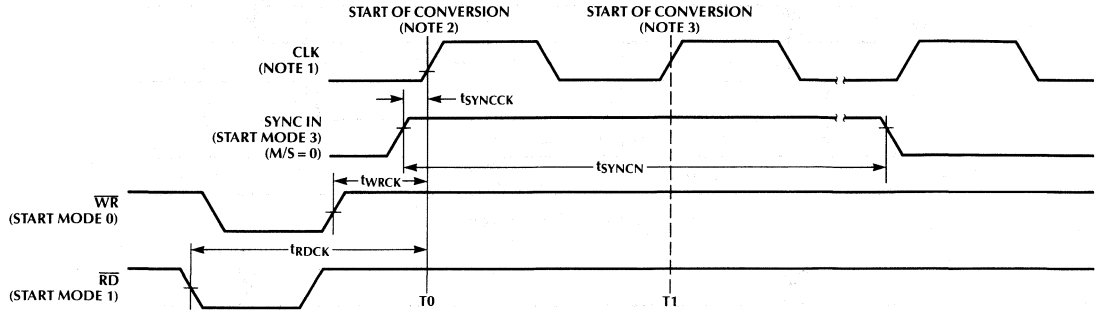


Figure 4. SYNC Output

TIMING DIAGRAMS (Continued)



NOTES:
1. CLK IS THE CLOCK DRIVEN AT THE CLOCK PIN.
2. IN CLK MODE 1, WILL ALWAYS OCCUR AT T0 IF SETUP TIMES ARE MET.
3. IN CLOCK MODE 0, WILL OCCUR EITHER AT T0 OR T1 IF SETUP TIMES ARE MET.

Figure 5. Start of Conversion (Start Mode 0,1,3)

BLOCK DIAGRAM

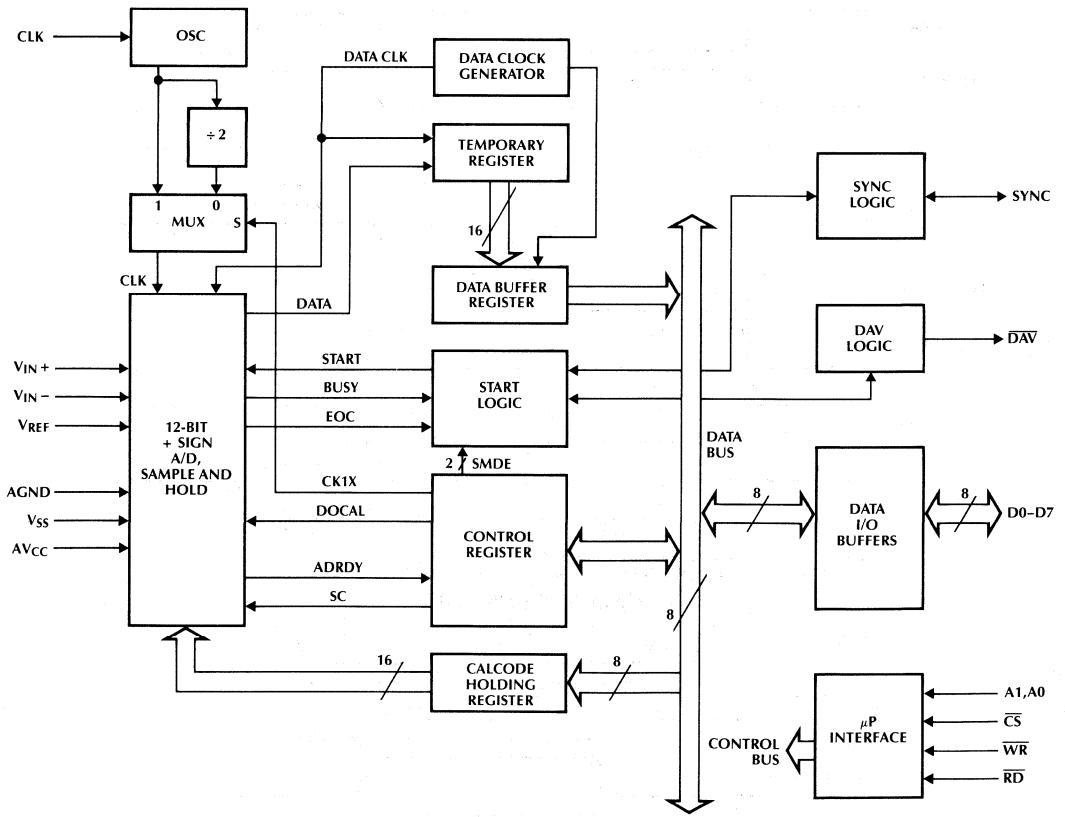


Figure 6. Block Schematic Diagram

FUNCTIONAL DESCRIPTION

ALGORITHMIC A/D CONVERTER

Micro Linear's algorithmic converter uses a successive approximation technique. Most of today's successive approximation converters use a DAC to feedback the approximated signal, however this technique requires more circuitry than algorithmic converters. In addition the values of all of the resistors or capacitors in the DAC must be matched to within the accuracy of the converter. This is difficult to do in silicon beyond 10 bits unless trimming is used. An algorithmic converter uses less circuitry and is more easily trimmed. Micro Linear's algorithmic converter is implemented using a 2x amplifier, a sample/hold amp, and a comparator as shown in Figure 7.

The input sample is first multiplied by two then compared to the reference voltage. If the 2x input voltage is greater than the reference, the MSB is a 1 and the reference voltage is subtracted from the 2x input voltage. The remainder is stored in the sample and hold. If the 2x input voltage is less than the reference, the MSB is a 0 and the 2x input voltage is stored in the sample and hold. This process repeats again, however now the sample and hold voltage is multiplied by 2.

The algorithm involves multiplication by 2, comparison, and possibly subtraction. Referring to Figure 6, the algorithm for the circuit can be described as follows:

Step 1 If $(2 \times V_{IN}) - V_{REF} \geq 0$
then MSB = 1
$(2 \times V_{IN}) - V_{REF} \rightarrow S/H$
else MSB = 0
$(2 \times V_{IN}) \rightarrow S/H$

Step 2 If $(2 \times S/H) - V_{REF} \geq 0$
then next bit = 1
$(2 \times S/H) - V_{REF} \rightarrow S/H$
else next bit = 0
$(2 \times S/H) \rightarrow S/H$

Step 3 Repeat Step 2 until conversion complete.

Since the A/D converter handles bipolar inputs, negative inputs are handled slightly differently using the same principle.

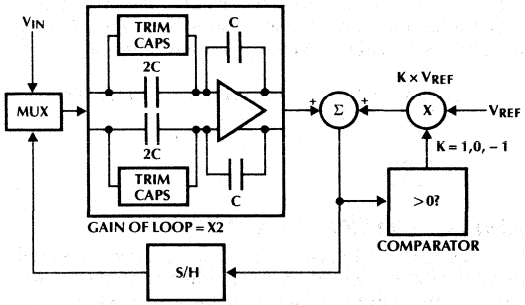


Figure 7. Self Calibrating A/D Converter

SELF CALIBRATION

In order to maintain integral and differential linearity to the 1/2 LSB level in an algorithmic converter, two critical parameters need to be controlled, loop offsets and the gain of the loop. Loop offsets are automatically nulled before each conversion using auto-zeroing circuitry on both the sampling amp and the 2x amp. The gain of the loop is adjusted using self calibration.

Self calibrating the algorithmic converter, once the offsets have been nulled, is performed by measuring the 2x gain of the loop and adjusting it. The gain can be measured by converting the reference voltage as the input as well as the reference (V_{REF}/V_{REF}), and examining the output code. Converting V_{REF} should yield plus full scale, since V_{REF}/V_{REF} should equal 1. If the gain of the loop is slightly less than 2, the resulting LSB of the conversion will be "0". If the magnitude bits of the resulting conversion are all "1s", the gain may be too great, therefore the gain is reduced to the point where the threshold of the LSB is reached.

Adjustment of the 2x gain is done with the binary weighted trim capacitor arrays connected to each of the 2C input capacitors. A small value of capacitance is either added to or subtracted from the 2C input caps until the gain of the loop is within 13 bit accuracy of 2.

FUNCTIONAL DESCRIPTION (Continued)

CONVERSION TIMES

The following table lists the conversion times which include the sample and hold acquisition time. For a CALRD and CALWR no A/D conversion actually takes place.

OPERATION	# OF INTERNAL CLOCKS*
8 bit A/D	80
13 bit A/D	110
CALWR	52
CALRD	80

SAMPLE AND HOLD TIMING

Figure 8 shows the internal timing for the sample and hold circuitry. The relationship between the "Start of Conversion" and the input channel going into sample mode is fixed at 6 internal clocks*, regardless of the Start Mode. Six internal clocks after the Start of Conversion the Sample and Hold is switched into the sample mode, placing two 9pF capacitors in parallel with the inputs pins; one on $V_{IN}+$ and one on $V_{IN}-$. The sample switch is kept in the sample mode for 8 internal clocks (2.3μs at a 7MHz external clock), then placed in the hold mode. During the next 2 internal clocks the charge on the sample and hold is transferred into the A/D, after which the V_{REF} pin is sampled for 8 internal clocks.

Figure 8 also illustrates the timing of the SYNC pin in Master Mode during a conversion (M/S = 1 Control High Byte register) and Start Mode 0, 1, or 2. SYNC is activated one internal clock cycle after the Start of Conversion and lasts for four internal clocks.

*For a description of internal clocks see Clock section.

ANALOG INPUTS

DIFFERENTIAL INPUTS AND COMMON MODE REJECTION

The differential inputs of the ML2230 eliminate the effects of common mode input noise (60Hz for example), as $V_{IN}+$ and $V_{IN}-$ are sampled at the same time.

NOISE

The leads to the analog inputs should be kept as short as possible to minimize output noise. Noise as well as digital clocks can couple into the inputs and cause errors. Input filters can be used to reduce the effects of these sources.

POWER SUPPLY DECOUPLING

Low inductance tantalum capacitors of 1μF or greater and 0.01μF disc ceramic capacitors are recommended for bypassing AV_{CC} as well as V_{SS} to AGND. These capacitors should be placed close to the AV_{CC} and V_{SS} pins.

MICROPROCESSOR INTERFACE

There are four 8 bit directly addressable registers; two Data Buffer registers, and two Control registers. The data buffer registers provide the conversion results. The data registers are double buffered, allowing one result to be read while the next sample is being converted. The data registers also allow access to the algorithmic converter's calibration code. Normally the ML2230 is operated without ever accessing these registers. (Refer to Diagnositcs for more information). The two Control registers provide complete control and status information. The four registers are addressed by pins A0 and A1.

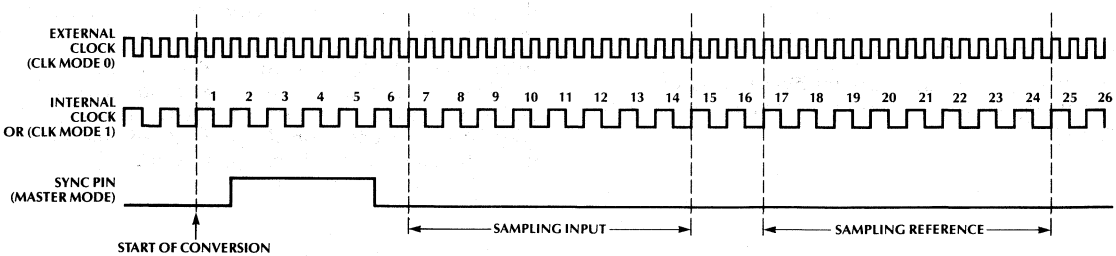


Figure 8. Sample and Hold Timing

FUNCTIONAL DESCRIPTION (Continued)

All data is returned from the converter in sixteen bit two's complement format, right hand justified, with the sign bit extended across the most significant bits.

Cycle	+Max	−Min	Zero
13	0FFF	F000	0000
8	007F	FF80	0000

REGISTER DESCRIPTION

Register 0—Data Buffer Low Byte:
Register 0 contains the low byte result of the latest conversion when read. Depending on the Start Mode selected, reading or writing to this register may start the next conversion.

Register 1—Data Buffer High Byte:
Register 1 contains the high byte result of the latest conversion when read.

Register 2—CONTROL Register Low Byte:

Bit 0 (DAV status when READ/DAVACK acknowledge when a ONE is written):
Reading DAV = 1 indicates that new data is available or a calibration is complete. If both data bytes have been read, DAV will be cleared automatically. This bit can be explicitly acknowledged by writing a ONE to it; writing a zero has no effect. The $\overline{DAV}$ output pin always reflects the DAV status bit.

Bit 1 (BUSY status when READ/RESET when a ONE is written):
Reading BUSY = 1 indicates that a conversion or calibration is in progress. Writing a ONE will force a chip reset. Writing a zero has no effect.

RESET Default Conditions:

Both Control registers will automatically be cleared. Both Data Buffer registers will be unchanged. The Calibration register is not cleared after a reset, however the ADRDY bit is cleared. Since the DAV status bit is cleared, the DAVB output is inactivated (high). The SYNC pin is forced to be an input as a result of clearing the M/S bit in the Control High Byte register.

Bit 2 (ADRDY status when READ/DOCAL request when a ONE is written):
Reading ADRDY = 0 indicates that the converter has not been calibrated since the last reset, and ADRDY = 1 indicates that it has been calibrated since the last reset. Writing a ONE will force the converter to do a calibration; writing a zero has no effect.

Bit 3 (SC: Short cycle select):
Selects 8 or 13 bit conversions.

SC = 0: 13-bit conversion (default)
SC = 1: 8-bit conversion (short cycle)

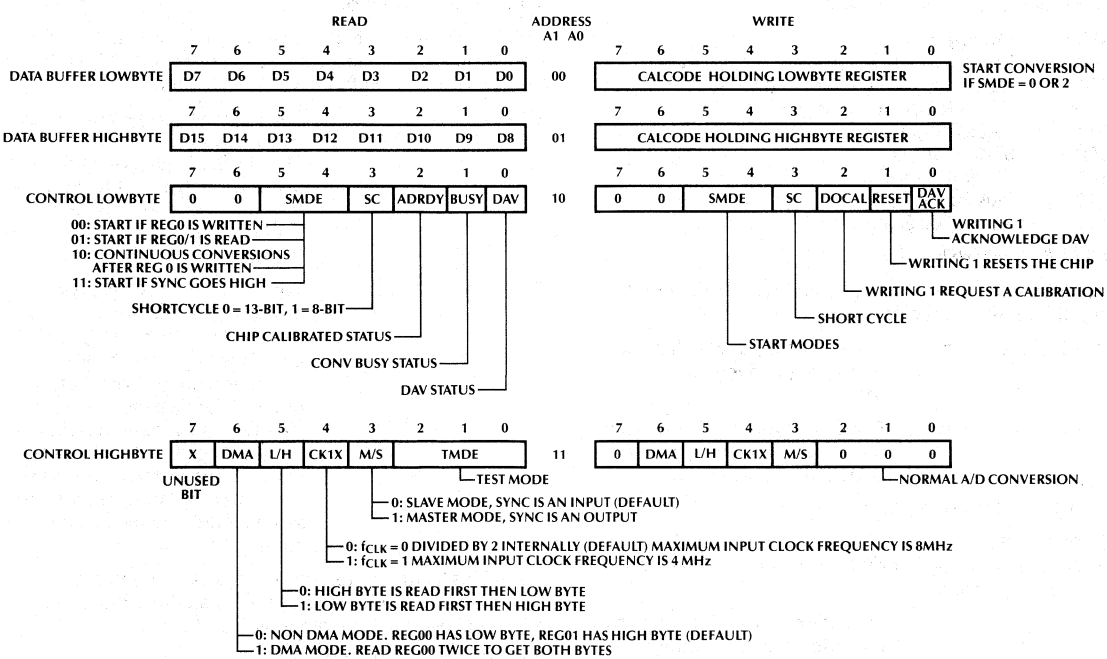


Figure 9. Register Description

FUNCTIONAL DESCRIPTION (Continued)

Note: For 8-bit conversions in non-DMA mode, only one byte needs to be read. This can be accomplished by setting L/H = 0, DMA = 0 and reading the Data Low Byte register. In DMA mode both bytes need to be read.

Bits 4,5 (SMDE: Start Mode):
Defines Start Conversion mode.

Bits 5,4

00	Start Conversion upon writing to register 0 (default)
01	Start Conversion upon reading register 0 if L/H = 0, or Start Conversion upon reading register 1 if L/H = 1. In DMA mode both bytes need to be read. The second byte read will Start Conversion.
10	Start Continuous Conversions upon writing to register 0.
11	Start on external SYNC input going high (Requires Slave mode: M/S = 0)

Bits 7,6 (reserved):
These bits are reserved by Micro Linear and must be written as zero.

Register 3 (Control Register High Byte):

Bits 2,1,0 (TMDE: test mode select bits)

These bits are used for diagnostic purposes only and normally not accessed during operation. The default value of TMDE is 000 which selects a normal A/D conversion. See Diagnostics for more information.

TMDE	Description
000	Normal A/D Conversion
001	Reserved by Micro Linear (Do Not Use)
010	CALWR Operation
011	CALRD Operation
100	System Offset
101	Common-mode
110	Plus Full Scale
111	Minus Full Scale

Bit 3 (M/S: Master/Slave bit):

Dictates whether the SYNC pin is an input or an output. Upon RESET, this bit is cleared.

M/S = 0: Slave Mode	SYNC is an input which is used to trigger a conversion if SMDE = 11.
M/S = 1: Master Mode	SYNC is an output. At the beginning of every conversion, SYNC is high for 4 internal clocks.

Bit 4 (CK1X: clock select bit):

Selects whether the external clock will be divided by two or used directly as the internal clock. See Clock section for a detailed explanation.

CK1X = 0:	the external clock is divided by two and used as the internal clock. This is referred to as CLK Mode = 0.
CK1X = 1:	the external clock input is used directly as the internal clock. This is referred to as CLK Mode = 1.

Bit 5 (L/H: Low Byte/High Byte):

In non-DMA mode the L/H bit defines whether DAVB is deactivated by reading the Data Low Byte or Data High Byte. In DMA mode, the L/H bit defines the order in which the Low/High Data Bytes are presented to the data bus. DMA mode automatically deactivates DAVB after both bytes are read.

*non-DMA mode: DMA = 0

L/H = 0:	reading register 0 (Low Byte) will de-assert DAVB
L/H = 1:	reading register 1 (High Byte) will de-assert DAVB

*DMA mode: DMA = 1

L/H = 0:	the first read is the Data High Byte, and the second read is the Data Low Byte, then DAVB output is de-asserted
L/H = 1:	the first read is the Data Low Byte, and the second read is the Data High Byte, then DAVB output is de-asserted

Bit 6 (DMA: DMA mode bit):

This bit allows both high and low bytes from the 13 bit conversion to be read from one address; either Data Buffer Low Byte or Data Buffer High Byte registers.

DMA = 0:	The high byte of the conversion will always be read from the Data Buffer High Byte register and the low byte of the conversion will always be read from the Data Buffer Low Byte Register.
DMA = 1:	Both high and low bytes of the conversion can be read from either the Data Buffer High or Low Byte Registers. A DMA controller, microprocessor, or other I/O device can use a single I/O address to read both the low and high bytes of the conversion. The order in which the high and low data bytes are presented is defined by the L/H control bit.

Note: This feature is not restricted to DMA controllers. It is an I/O option which may be used by a DMA controller, microprocessor, or any other type of I/O device.

Bit 7 (Reserved by Micro Linear)

This bit is not used. When written use zero.

FUNCTIONAL DESCRIPTION (Continued)

GENERAL OPERATING INFORMATION

CONVERSION-START PROTOCOL

There are four different ways to start a conversion. They are defined by SMDE bits 4 and 5 in the Control Low Byte Register.

SMDE Bits 5,4

00: A write to register 0 will start a conversion. During a conversion, if another write is issued to register 0, the "Start Conversion" command will be latched and another conversion will immediately follow the current one. To insure that the second write will be latched, it must occur at least 3 internal clocks after the first write. Only one additional write will be latched; multiple writes within a conversion will only yield one more conversion.

01: Reading the data from the previous conversion starts the next conversion. Start Conversion upon reading register 0 if L/H = 0, or Start Conversion upon reading register 1 if L/H = 1. In DMA mode both bytes need to be read. The second byte read will Start the Conversion.

10: This mode causes continuous conversions; the next conversion begins immediately after the previous conversion ends. Writing to register 0 will start the first conversion; thereafter the converter runs continuously. This mode yields the maximum conversion rate.

11: The Sync input triggers the start of a conversion. The M/S bit in the Control High Byte Register must be cleared, placing the chip in the slave mode.

Note: The external activation signals for Start Modes 0, 1, and 3 are synchronized internally to the system clock. If periodic sampling is required using these Start Modes, the SYNC, $\overline{RD}$, or $\overline{WR}$ pulses must be synchronized to the system clock. Start Mode 2 guarantees periodic sampling.

DOUBLE-BUFFERED DATA REGISTER

The A/D conversion result is double-buffered using the Data Buffer registers and the A/D Data register. The actual End-Of-Conversion (EOC) does not correspond with the DAVB output going low. The DAVB output goes low 16 internal clocks after the EOC. From the time DAVB output goes LOW, the user has one full conversion time (80 or 110 internal clocks) minus 16 internal clocks to read two data bytes as shown in Figure 10.

SELF CALIBRATION

Setting the DOCAL bit issues a calibration request to the chip. When calibration is done, the DAV status bit is set and the DAVB output goes low.

A calibration requires 8,260 internal clocks. Using a 7MHz clock (CLK Mode = 0), this is approximately 2 ms. Power supplies and external voltage reference must be stable before issuing a request for calibration.

The ML2230 should be calibrated before any conversions are attempted. Calibrations must not be performed simultaneously with conversions. Before requesting a calibration, the user may want to read the Busy status bit to make sure that the converter is idle. Polling the chip while the calibration is in progress is not recommended.

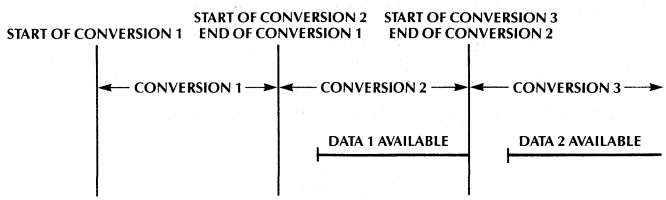


Figure 10

FUNCTIONAL DESCRIPTION (Continued)

CLOCK

The ML2230 has the option of dividing the clock at the CLK pin by 2, or using it directly to drive the internal logic. This option is selected through the CK1X bit in the Control register. When CK1X = 0 the clock is divided by 2. This is referred to as CLK Mode = 0. The clock at the CLK pin is referred to as the External clock, and the Internal Clock is the External clock divided by 2. When CK1X = 1, the clock at the CLK pin drives the internal logic directly, therefore this clock is referred to as the Internal clock. This is also known as CLK Mode = 1. All internally clocked logic is positive edge triggered.

CLK Mode = 0:

There are two advantages to CLK Mode 0. This is the only Mode that allows an external crystal to be used. CLK Mode 1 cannot operate with an external crystal, the CLK pin must be driven. The second advantage of CLK Mode 0 is that the duty cycle for a driven clock is less stringent than in CLK Mode 1. (Refer to t_{CLK0} and t_{CLK1} in AC Electrical Characteristics for CLK Mode 0 and 1 timing requirements, respectively.)

On power up the state of the divide by two flip-flop is indeterminate. Therefore the relationship between the internal clock and the external clock at the CLK pin can have one of two possibilities as shown in Figure 11. As a result the following should be considered.

t_{WRCK}, t_{RDCK}, and t_{SYNCCK} specs, ($\overline{RD}$, $\overline{WR}$, and SYNC setup times to Start of Conversion), will be as shown in the data sheet, or the data sheet specs plus one external clock period. Since these specifications are with respect to the rising edge of the external clock, it is not known whether this rising edge corresponds to the rising edge or falling edge of the internal clock. Therefore there is an uncertainty of one external clock period.

If periodic sampling is necessary and Start Mode 0,1, or 3 is used, the external start pulse (either $\overline{RD}$, $\overline{WR}$, or SYNC) must be synchronous to the external clock, meet the setup time, and be an even number of external clock periods. If the start pulse were an odd number of external clock periods, half the pulses would correspond with the rising edge of the internal clock, and the other half would correspond with the falling edge of the internal clock. Therefore the sampling period would change by one external clock period every sample. Start Mode 2 guarantees periodic sampling regardless of the CLK mode.

CLK Mode = 1:

This mode eliminates the requirement that external start pulses must be an even number of external clock periods. However periodic sampling still requires that the start pulse be synchronous to the external clock, and the setup time must be met. CLK Mode 1 also eliminates the uncertainty of the t_{WRCK}, t_{RDCK}, and t_{SYNCCK} requirements.

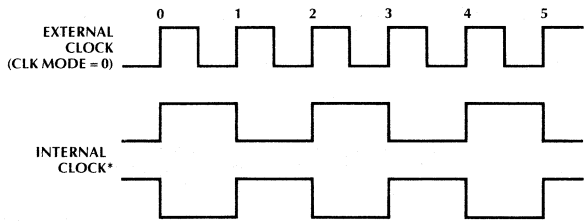


Figure 11

FUNCTIONAL DESCRIPTION (Continued)

DIAGNOSTICS

Diagnostic routines may be run after power up or any other time to ensure proper operation. The diagnostic features, which are software selectable, don't require external hardware. Both the analog and digital sections can be tested.

The ML2230 is placed in the diagnostic mode via the TMDE field in the Control High Byte Register. Once the ML2230 is placed in one of the diagnostic modes, a conversion must be executed before the results can be read. As with all conversions, DAVB will be activated upon completion.

ANALOG CONVERSION DIAGNOSTICS

TMDE = 000: Normal Operation
Selects normal A/D conversion. Default condition after a software reset.

TMDE = 001: Reserved by Micro Linear.

TMDE = 010: CALWR operation
The data in Write register 0 and 1 (CALCODE Holding Register), are transferred into the converter's Calibration register when a "Start Conversion" is issued. A dummy conversion occurs and the DAVB output goes LOW to indicate that the operation is complete.

TMDE = 011: CALRD operation
The contents of the Calibration register are transferred through the A/D Data register and loaded into the Data Buffer registers. A dummy 8-bit conversion occurs and DAVB output goes LOW to indicate that the CALRD operation is complete.

TMDE = 100: System Offset
The positive and negative inputs to the Sample and Hold are tied to analog ground. With this setting, converted data will give the offset of the A/D converter and Sample/Hold combination. The $V_{IN}+$ and $V_{IN}-$ pins will remain in a high impedance state while in this mode.

TMDE = 101: Common-mode
Both the positive and negative inputs of the Sample and Hold are tied to V_{REF}. The results of a conversion in this test mode indicates how well the converter is rejecting a common mode signal.

TMDE = 110: Positive Full Scale
This test mode connects the positive input of the Sample and Hold to V_{REF} and the negative input of the Sample and Hold to analog ground. The result of converting in this test mode is a value near positive full scale.

TMDE = 111: Negative Full Scale
This test mode connects the positive input of the Sample and Hold to analog ground and the negative input to V_{REF}. The result of converting in this test mode is a value near negative full scale.

DIGITAL LOOPBACK

The ML2230's architecture provides a way for the microprocessor to indirectly read and write to the A/D converter's calibration register and data register via a CALRD and CALWR. Figure 12 illustrates this architecture. This in effect allows a digital loopback.

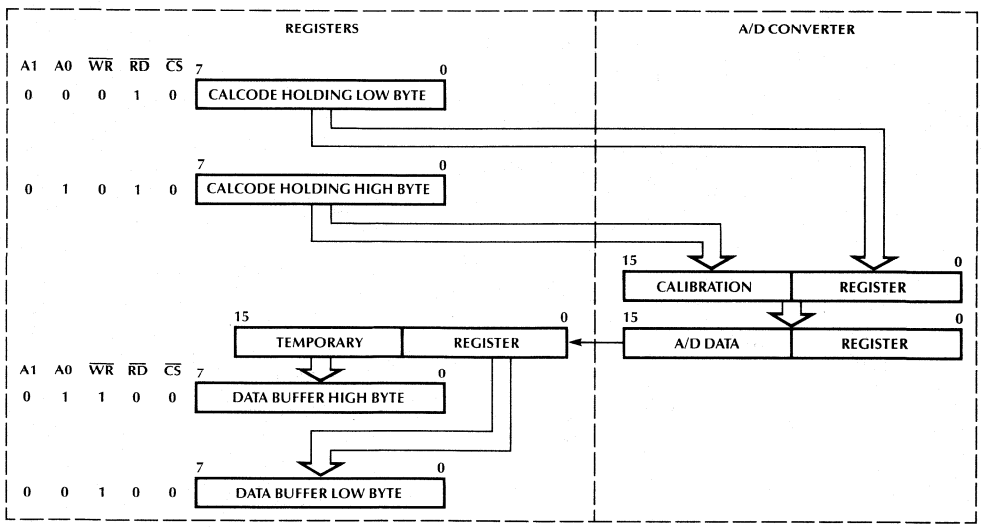


Figure 12. Digital Loopback

FUNCTIONAL DESCRIPTION (Continued)

When the TMDE bits are set to 010 CAL WRITE (CALWR), and a Start Conversion is issued in any one of the four modes, the contents of the CALCODE Holding Low Byte and High Byte registers are transferred into the A/D converter's Calibration register. When the TMDE bits are set to 011 CAL READ (CALRD), and a Start Conversion is issued, the contents of the Calibration register are transferred through the A/D's Data register into the Data Buffer Low Byte and Data Buffer High Byte registers. The result of these two operations is a complete loopback from the CALCODE Holding registers through the A/D converter and back into the Data buffer registers. This loopback provides user assurance that all the paths are clear and there are no stuck bits.

Note: When a CALWR is done, the previous calibration value is lost. The correct calibration value must be restored before the converter is used to convert data.

CALIBRATION PASS/FAIL TEST

The CALRD can be used as a way to verify a successful calibration. After a calibration is completed, the CALRD may be issued in order to read the contents of the Calibration register. If the Low Byte of the data buffer register is all ones after executing a CALRD, the calibration failed; otherwise the calibration is successful.

FUNCTIONAL DESCRIPTION (Continued)

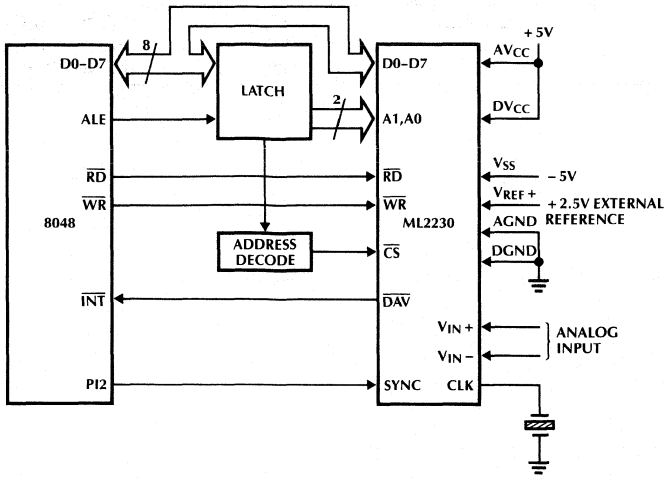


Figure 13. Interfacing to 8048 Microcontroller

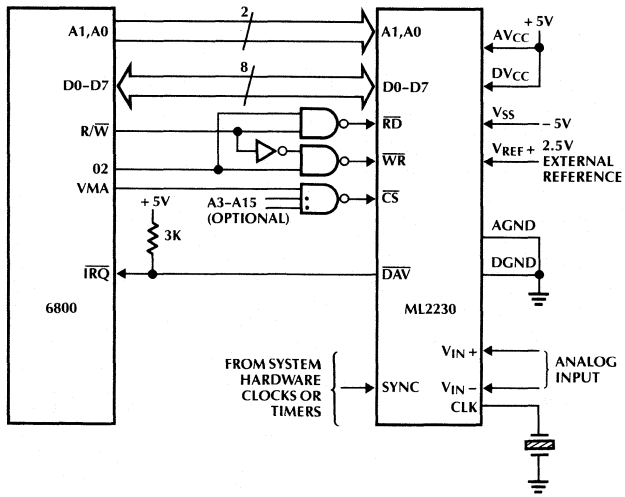


Figure 14. Interfacing to 6800 Microprocessor

ORDERING INFORMATION

PART NUMBER	LINEARITY ERROR	MINIMUM CONVERSION	TEMPERATURE RANGE	PACKAGE
ML2230BCJ	±¾ LSB	31.5μs	0°C to +70°C	Hermetic DIP
ML2230CCJ	±1 LSB	31.5μs	0°C to +70°C	Hermetic DIP
ML2230DCJ	±1 LSB	44.0μs	0°C to +70°C	Hermetic DIP

October 1990
PRELIMINARY

ML2233

μP Compatible 12-Bit Plus Sign A/D Converter with Sample and Hold

GENERAL DESCRIPTION

The ML2233 is a member of Micro Linear's 12-bit plus sign CMOS A/D converter family utilizing a self calibrating algorithmic technique. The sample-and-hold, incorporated on the ML2233, has a differential input for noise immunity and power supply rejection. All errors of the sample-and-hold are accounted for in the analog-to-digital converter's accuracy specification.

The ML2233B has a maximum non-linearity error over temperature of 0.018% of full-scale, and the ML2233C and ML2233D have a maximum non-linearity error over temperature of 0.024% of full scale.

Designed to interface to a 16-bit microprocessor bus without additional components, the ML2233 outputs the 13-bit data result in one word. Data format is 2's complement. All digital signals are fully TTL and CMOS compatible.

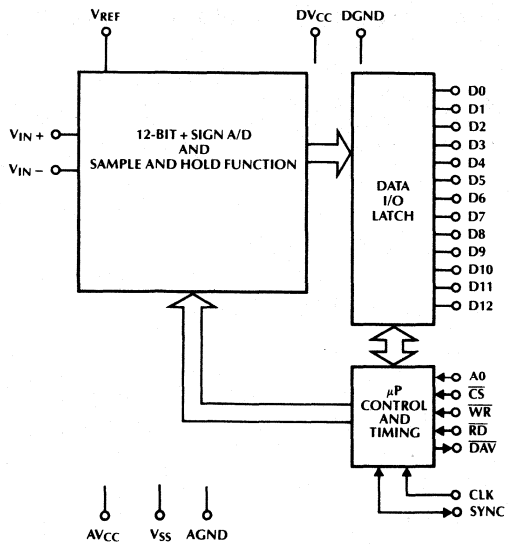
For interfacing to an 8-bit microprocessor bus the ML2230 provides a 13-bit data result in two 8-bit bytes.

FEATURES

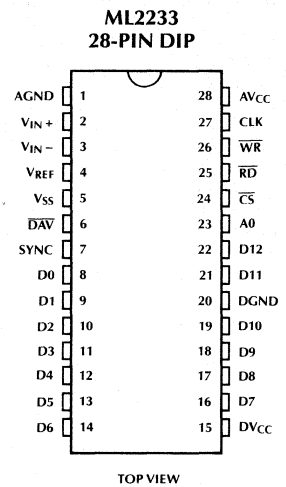
- Resolution 12-bits + sign
- Conversion time (including S/H acquisition) 31.5μs max
- Sample and hold acquisition 2.3μs max
- Non-linearity error ±¾LSB and ±1LSB max
- Low harmonic distortion 0.01%
- No missing codes
- Self calibrating—maintains accuracy over time and temperature
- Inputs withstand |7V| beyond supplies
- Data transfer options—interrupt, DMA, or polling
- 13-bit result for 16-bit bus interface
- Standard 28-pin DIP

2

BLOCK DIAGRAM



PIN CONNECTIONS



PIN DESCRIPTION

PIN NO.	NAME	FUNCTION
1	AGND	Analog ground.
2	$V_{IN}+$	Positive differential analog input; range = $V_{SS} \le V_{IN}+ \le AV_{CC}$, $\lvert(V_{IN}+)-(V_{IN}-)\rvert \le V_{REF}$.
3	$V_{IN}-$	Negative differential analog input; range = $V_{SS} \le V_{IN}- \le AV_{CC}$, $\lvert(V_{IN}+)-(V_{IN}-)\rvert \le V_{REF}$.
4	V_{REF}	Voltage reference input; referenced to analog ground.
5	V_{SS}	Negative power supply; decouple to AGND.
6	$\overline{DAV}$	Data available; indicates a conversion has completed and data is available or calibration completed.
7	SYNC	In the slave mode, SYNC is a positive edge triggered input used to start aconversion. In master mode, SYNC is an output and indicates conversion start.
8	D0	Bidirectional data bit.
9	D1	Bidirectional data bit.
10	D2	Bidirectional data bit.
11	D3	Bidirectional data bit.
12	D4	Bidirectional data bit.
13	D5	Bidirectional data bit.
14	D6	Bidirectional data bit.
15	DV_{CC}	Digital power supply.
16	D7	Bidirectional data bit.
17	D8	Bidirectional data bit.
18	D9	Bidirectional data bit.
19	D10	Bidirectional data bit.
20	DGND	Digital ground.
21	D11	Bidirectional data bit.
22	D12	Bidirectional data bit.
23	A0	Address for the microprocessor interface to access registers.
24	$\overline{CS}$	Chip select; enables writing to or reading from.
25	$\overline{RD}$	Read; enables ML2233 to drive data bus.
26	$\overline{WR}$	Write; allows writing into the registers.
27	CLK	Clock input. Driven with an external clock or crystal referenced to DGND. The crystal must be parallel resonant with minimum capacitive loading. (i.e., no bypass caps should be used and leads should be kept short.)
28	AV_{CC}	Positive analog power supply. Decouple to AGND. Tie to DV_{CC} from same power supply.

ABSOLUTE MAXIMUM RATINGS
(Note 1)

Supply Voltages (AV_{CC} and DV_{CC}) 6.0V
Negative Supply Voltage (V_{SS}) ..... −6.0V
Voltage at Analog Inputs ..... V_{SS} − 7V to AV_{CC} + 7V
Voltage at V_{REF} ..... V_{SS} − 7V to AV_{CC} + 7V
Input Current per Digital Pin ..... ±10mA
Input Current at Analog Inputs ..... ±20mA
Storage Temperature Range ..... −65°C to +150°C
Package Dissipation @ 25°C 875mW
Lead Temperature (soldering, 10 seconds)
Dual-In-Line Package (Ceramic) ..... 300°C

OPERATING CONDITIONS (Note 2)

Temperature Range ..... 0°C to 70°C
Supply Voltage (AV_{CC} and DV_{CC}) ..... $4.5V_{DC}$ to $6.0V_{DC}$
Negative Supply Voltage (V_{SS}) ..... $-4.5V_{DC}$ to $-6.0V_{DC}$
Reference Voltage (V_{REF}) 2.60V

ELECTRICAL CHARACTERISTICS

The following specifications apply for AV_{CC} = DV_{CC} = 5V ± 5%, V_{SS} = –5V ± 5%, V_{REF} = 2.500V, V_{IN}– = AGND, V_{IN}+ = –2.5V to +2.5V, T_A = T_{MIN} to T_{MAX} unless otherwise specified.

PARAMETER	NOTES	CONDITIONS	MIN	TYP (Note 3)	MAX	UNITS
Converter Characteristics						
Linearity Error ML2233BCJ ML2233CCJ ML2233DCJ	4	 f_{CCLK} = 0.1 ≤ 7MHz f_{CCLK} = 0.1 ≤ 7MHz f_{CCLK} = 0.1 ≤ 5MHz			 ±¾ ±1 ±1	 LSB LSB LSB
Unadjusted Zero Error ML2233BCJ ML2233CCJ ML2233DCJ	4				 ±¾ ±2 ±2	 LSB LSB LSB
Unadjusted Positive and Negative Full Scale Error	5				±4	LSB
Zero Error Temperature Coefficient				0.5		ppm/°C
Gain Temperature Coefficient				10		ppm/°C
Common-Mode Rejection	5, 6		80			dB
Analog Input Source Resistance	5				2	kΩ
Analog Input Range	4	V_{IN}+ Referred to V_{IN}–	$-V_{REF}$		$+V_{REF}$	V
Analog Input Leakage Current	4				100	nA
Voltage Reference Input Source Impedance	5				0.5	kΩ
Reference Input Leakage Current	4				100	nA
Digital and DC Characteristics						
Power Supply Current AI_{CC}, Analog V_{CC} DI_{CC}, Digital V_{CC} I_{SS}, V_{SS}	4			 30 10 18	 50 30	 mA µA mA
Power Supply Rejection AV_{CC} V_{SS}	7	 DC DC to 25kHz DC DC to 25kHz		 80 50 80 50		 dB dB dB dB
V_{ILCLK}, Clock Input Low Voltage	4				0.8	V
V_{IHCLK}, Clock Input High Voltage	4		3.5		AV_{CC}	V
I_{L1}, Input Leakage Current (CLK)	4	AGND ≤ V_{IN} ≤ AV_{CC}			±200	µA
V_{IL}, Input Low Voltage	4				0.8	V
V_{IH}, Input High Voltage	4		2.0		DV_{CC}	V
V_{OL}, Output Low Voltage	4	I_{OL} = 2.0mA			0.45	V
V_{OH}, Output High Voltage	4	I_{OH} = –400µA	2.4			V
I_L, Input Leakage Current (except CLK)	4	AGND ≤ V_{IN} ≤ AV_{CC}			±10	µA
I_{HI-Z}, Output Leakage Current (D0–D12)	4	$\overline{RD}$ = $\overline{CS}$ = V_{IH}			±10	µA
C_I, Input Capacitance (all digital inputs)				10		pF
C_O, Output Capacitance (outputs D0 to D12, SYNC and $\overline{DAV}$)				10		pF

ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER		CONDITIONS		MIN	TYP (Note 3)	MAX	UNITS
AC Electrical Characteristics (Note 8)								
t_C	Conversion Time	4, 9	CLK Mode = 0	f_{CLK} = 7.0MHz f_{CLK} = 5.0MHz	31.5 44.0			μs μs
	Sample and Hold Acquisition	4, 9	CLK Mode = 0	f_{CLK} = 7.0MHz f_{CLK} = 5.0MHz			2.3 3.2	μs μs
f_{CLK0}	Clock Frequency	5, 9	CLK Mode = 0	Crystal Driven	3 1		7 7	MHz MHz
t_{CLK0}	Clock Width	5, 9	Driven (CLK Mode = 0)	High Low	50 50			ns ns
f_{CLK1}	Clock Frequency	5, 10	Driven (CLK Mode = 1)		0.5		(Note 11)	MHz
t_{CLK1}	Clock Width	5, 10	Driven (CLK Mode = 1)	High Low	125 125			ns ns
t_{AD}	Address Stable to Valid Data	4			150			ns
t_{AR}	Address Stable Before Read	4			0			ns
t_{RA}	Address Hold After Read	4			0			ns
t_{RR}	Read Pulse Width	4			150			ns
t_{RD}	Read Access	4					150	ns
t_{1Z}, t_{0Z}	Data Read to Hi-Z	4			0		50	ns
t_{RV}	Recovery Between Two Reads or Writes	5			250			ns
t_{RDCK}	Read to Clock Setup Time	5, 12			40			ns
t_{AW}	Address Stable Before Write	4			0			ns
t_{WA}	Address Hold After Write	4			0			ns
t_{WW}	Write Pulse Width	4			150			ns
t_{DW}	Data Setup Before Write Trailing Edge	4			100			ns
t_{WD}	Data Hold After Write Trailing Edge	4			0			ns
t_{WRCK}	Write to Clock Setup Time	5, 12			40			ns
t_{CKDAV}	Clock to $\overline{DAV}$ Assert	4, 13	C_L = 50pF			120	220	ns
t_{SYNCCK}	SYNC Input to Clock Setup	5, 12			40			ns
t_{SYNCN}	SYNC Input Width	5	(CLK Mode = 0) (CLK Mode = 1)		6 3			$1/f_{CLK0}$ $1/f_{CLK1}$
t_{CKSYNC}	External Clock to SYNC Output Delay	5, 13	C_L = 50pF			150	200	ns
t_{SYNCO}	SYNC Output Pulse Width	5, 13	(CLK Mode = 0) (CLK Mode = 1)				8 4	$1/f_{CLK0}$ $1/f_{CLK1}$
t_{WRDAV}	Write Reg2 to $\overline{DAV}$ Rising Edge	4, 14	C_L = 50pF				170	ns
t_{RDDAV}	Read Reg0 to $\overline{DAV}$ Rising Edge	4, 15	C_L = 50pF				170	ns
t_r, t_f	Rise and Fall		All Inputs				25	ns

Note 1: Absolute maximum ratings are limits beyond which the life of the integrated circuit may be impaired. All voltages unless otherwise specified are measured with respect to ground.
Note 2: Devices are 100% tested with temperature limits guaranteed by 100% testing, sampling or by correlation with worst-case test conditions.
Note 3: Typicals are parametric norm at 25°C.
Note 4: Parameter guaranteed and 100% production tested.
Note 5: Parameter guaranteed. Parameters not 100% tested are not in outgoing quality level calculation.
Note 6: Common mode rejection is the ratio of the change in zero error to the change in common mode input range.
Note 7: Power supply rejection is the ratio of the change in zero error to the change in power supply voltage.
Note 8: All parameters measured from 0.8V to 2.0V, C_L = 100pF.
Note 9: CK1X bit in control register = 0.
Note 10: CK1X bit in control register = 1.
Note 11: Maximum frequency is $1/t_{CLK1}$ (high) + t_{CLK1} (low) + rise + fall times and $\leq$ 3.5MHz.
Note 12: Setup time required for synchronous start of conversion.
Note 13: In CLK mode = 0 (CK1X bit in control register = 0) start of conversion will occur at specified time; or time plus one f_{CLK0} period (see Figure 5).
Note 14: Writing a control register bit 0 with a one will acknowledge the $\overline{DAV}$ condition and de-assert DAV output.
Note 15: In start mode = 1, a read from location "0" will start the next conversion and de-assert the DAV output.

TIMING DIAGRAMS

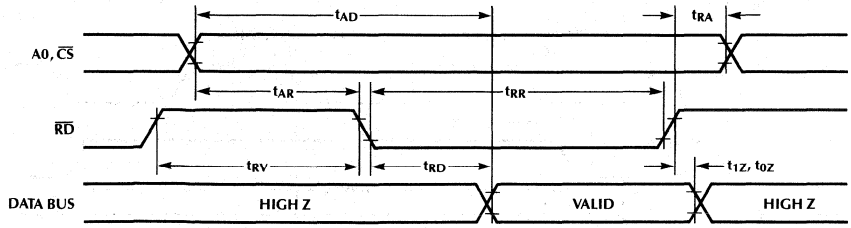


Figure 1. Read Cycle

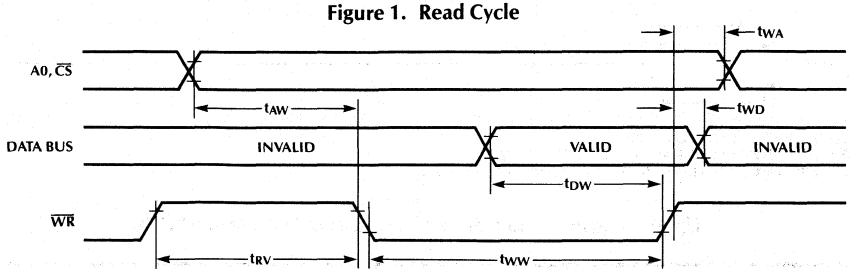
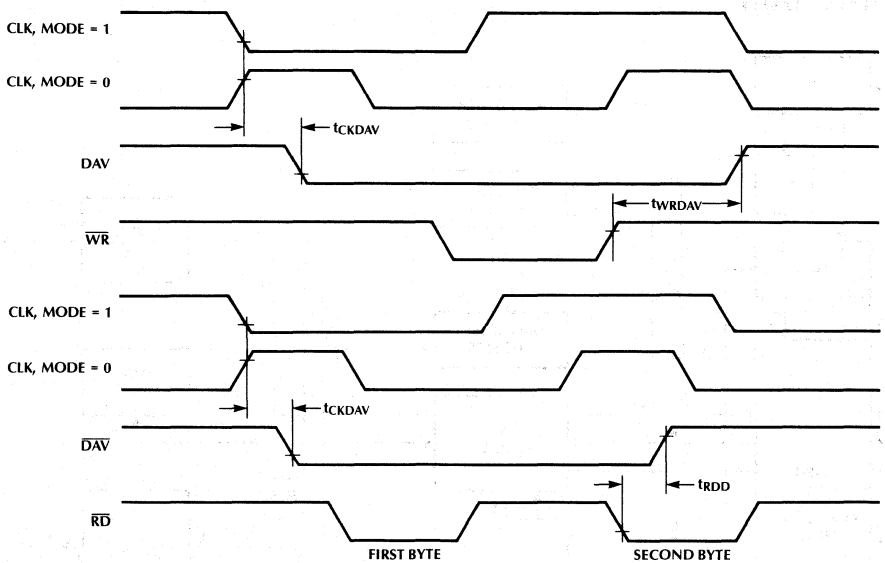


Figure 2. Write Cycle



DAV IS SET AND CLEARED BY INTERNAL CIRCUITRY.
NOTE: DMA BIT IN THE CONTROL REGISTER MUST BE SET FOR THIS OPERATION.

Figure 3. Data Available

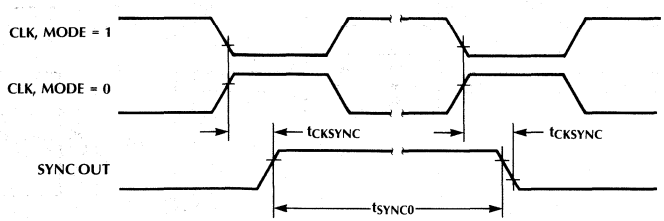
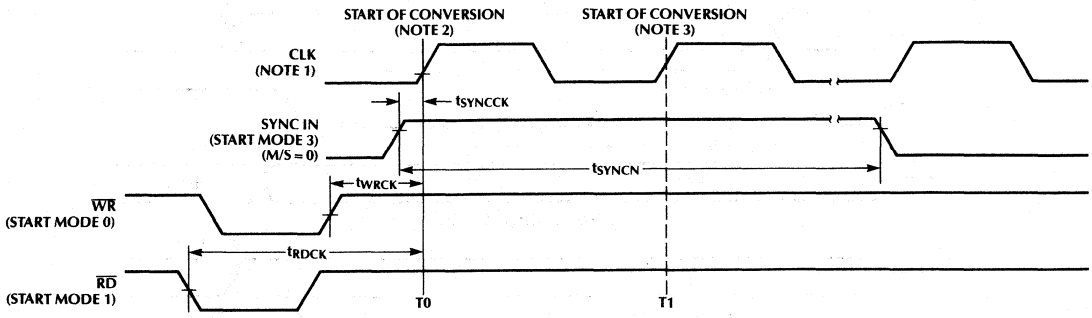


Figure 4. SYNC Output

TIMING DIAGRAMS (Continued)



NOTES:
1. CLK IS THE CLOCK DRIVEN AT THE CLOCK PIN.
2. IN CLK MODE 1, WILL ALWAYS OCCUR AT T0 IF SETUP TIMES ARE MET.
3. IN CLK MODE 0, WILL OCCUR EITHER AT T0 OR T1 IF SETUP TIMES ARE MET.

Figure 5. Synchronous Start of Conversion (Start Mode 0,1,3)

BLOCK DIAGRAM

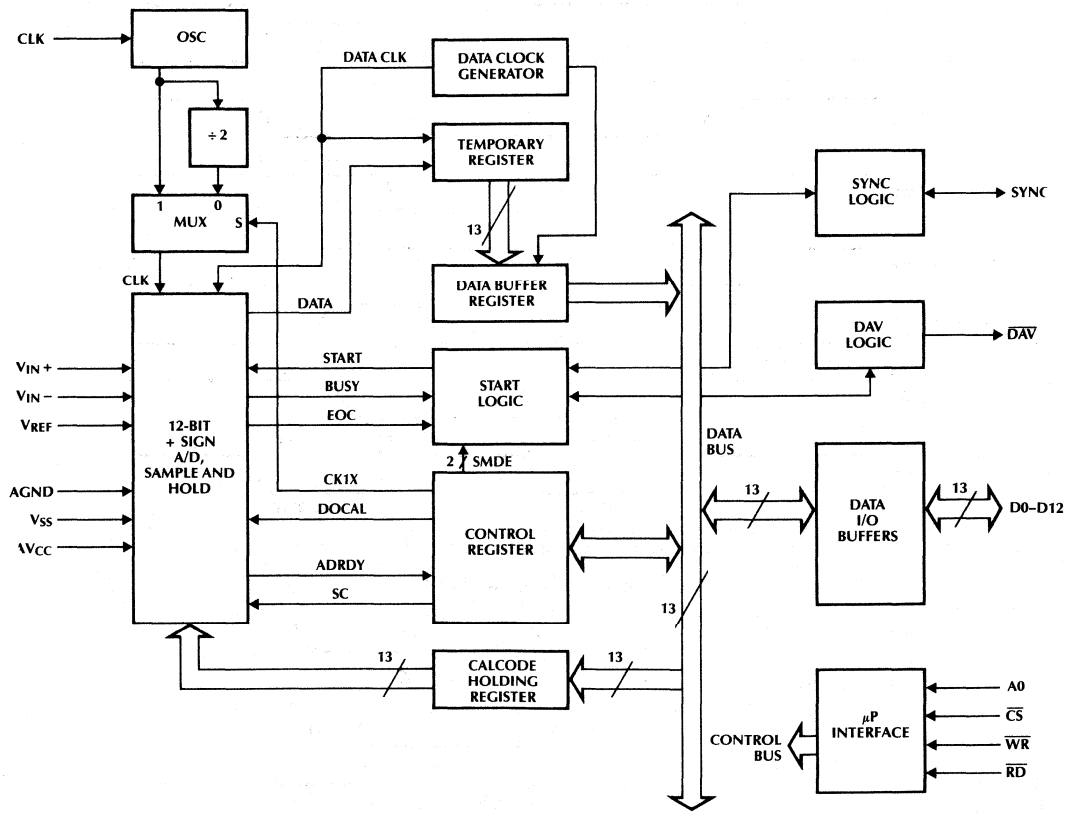


Figure 6. Block Schematic Diagram

FUNCTIONAL DESCRIPTION

ALGORITHMIC A/D CONVERTER

Micro Linear's algorithmic converter uses a successive approximation technique. Most of today's successive approximation converters use a DAC to feedback the approximated signal, however this technique requires more circuitry than algorithmic converters. In addition the values of all of the resistors or capacitors in the DAC must be matched to within the accuracy of the converter. This is difficult to do in silicon beyond 10 bits unless trimming is used. An algorithmic converter uses less circuitry and is more easily trimmed. Micro Linear's algorithmic converter is implemented using a 2x amplifier, a sample/hold amp, and a comparator as shown in Figure 7.

The input sample is first multiplied by two then compared to the reference voltage. If the 2x input voltage is greater than the reference, the MSB is a 1 and the reference voltage is subtracted from the 2x input voltage. The remainder is stored in the sample and hold. If the 2x input voltage is less than the reference, the MSB is a 0 and the 2x input voltage is stored in the sample and hold. This process repeats again, however now the sample and hold voltage is multiplied by 2.

The algorithm involves multiplication by 2, comparison, and possibly subtraction. Referring to Figure 6, the algorithm for the circuit can be described as follows:

Step 1 If $(2 \times V_{IN}) - V_{REF} \geq 0$
then MSB = 1
$(2 \times V_{IN}) - V_{REF} \rightarrow S/H$
else MSB = 0
$(2 \times V_{IN}) \rightarrow S/H$

Step 2 If $(2 \times S/H) - V_{REF} \geq 0$
then next bit = 1
$(2 \times S/H) - V_{REF} \rightarrow S/H$
else next bit = 0
$(2 \times S/H) \rightarrow S/H$

Step 3 Repeat Step 2 until conversion complete.

Since the A/D converter handles bipolar inputs, negative inputs are handled slightly differently using the same principle.

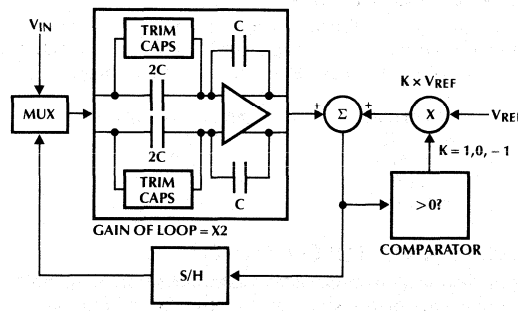


Figure 7. Self Calibrating A/D Converter

SELF CALIBRATION

In order to maintain integral and differential linearity to the 1/2 LSB level in an algorithmic converter, two critical parameters need to be controlled, loop offsets and the gain of the loop. Loop offsets are automatically nulled before each conversion using auto-zeroing circuitry on both the sampling amp and the 2x amp. The gain of the loop is adjusted using self calibration.

Self calibrating the algorithmic converter, once the offsets have been nulled, is performed by measuring the 2x gain of the loop and adjusting it. The gain can be measured by converting the reference voltage as the input as well as the reference (V_{REF}/V_{REF}), and examining the output code. Converting V_{REF} should yield plus full scale, since V_{REF}/V_{REF} should equal 1. If the gain of the loop is slightly less than 2, the resulting LSB of the conversion will be "0". If the magnitude bits of the resulting conversion are all "1s", the gain may be too great, therefore the gain is reduced to the point where the threshold of the LSB is reached.

Adjustment of the 2x gain is done with the binary weighted trim capacitor arrays connected to each of the 2C input capacitors. A small value of capacitance is either added to or subtracted from the 2C input caps until the gain of the loop is within 13 bit accuracy of 2.

FUNCTIONAL DESCRIPTION (Continued)

CONVERSION TIMES

The following table lists the conversion times which include the sample and hold acquisition time. For a CALRD and CALWR no A/D conversion actually takes place.

OPERATION	# OF INTERNAL CLOCKS*
8 bit A/D	80
13 bit A/D	110
CALWR	52
CALRD	80

SAMPLE AND HOLD TIMING

Figure 8 shows the internal timing for the sample and hold circuitry. The relationship between the "Start of Conversion" and the input channel going into sample mode is fixed at 6 internal clocks*, regardless of the Start Mode. Six internal clocks after the Start of Conversion the Sample and Hold is switched into the sample mode, placing two 9pF capacitors in parallel with the inputs pins; one on $V_{IN}+$ and one on $V_{IN}-$. The sample switch is kept in the sample mode for 8 internal clocks (2.3μs at a 7MHz external clock), then placed in the hold mode. During the next 2 internal clocks the charge on the sample and hold is transferred into the A/D, after which the V_{REF} pin is sampled for 8 internal clocks.

Figure 8 also illustrates the timing of the SYNC pin in Master Mode during a conversion (M/S = 1 Control register) and Start Mode 0, 1, or 2. SYNC is activated one internal clock cycle after the Start of Conversion and lasts for four internal clocks.

*For a description of internal clocks see Clock section.

ANALOG INPUTS

DIFFERENTIAL INPUTS AND COMMON MODE REJECTION

The differential inputs of the ML2233 eliminate the effects of common mode input noise (60Hz for example), as $V_{IN}+$ and $V_{IN}-$ are sampled at the same time.

NOISE

The leads to the analog inputs should be kept as short as possible to minimize output noise. Noise as well as digital clocks can couple into the inputs and cause errors. Input filters can be used to reduce the effects of these sources.

POWER SUPPLY DECOUPLING

Low inductance tantalum capacitors of 1μF or greater and 0.01μF disc ceramic capacitors are recommended for bypassing AV_{CC} as well as V_{SS} to AGND. These capacitors should be placed close to the AV_{CC} and V_{SS} pins.

MICROPROCESSOR INTERFACE

There are two 13-bit directly addressable registers; a Data Buffer register and a Control register. The data buffer register provides the conversion results. The data register is double buffered, allowing one result to be read while the next sample is being converted. The data register also allows access to the algorithmic converter's calibration code. Normally the ML2233 is operated without ever accessing these registers. (Refer to Diagnostics for more information). The Control register provides complete control and status information. The two registers are addressed by pin A0.

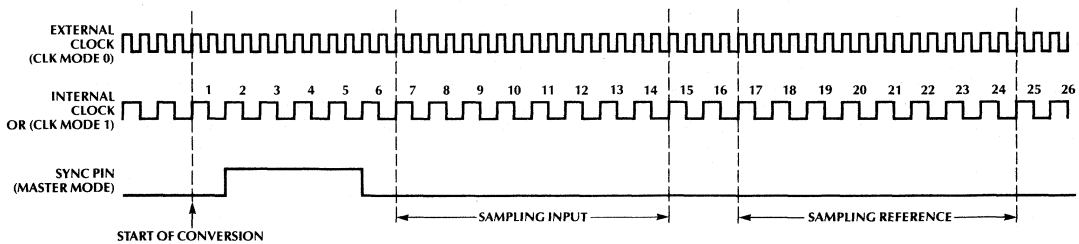


Figure 8. Sample and Hold Timing

FUNCTIONAL DESCRIPTION (Continued)

All data is returned from the converter in two's complement format.

Cycle	+Max	−Min	Zero
13	0FFF	1000	0000
8	007F	1F80	0000

REGISTER DESCRIPTION

Register 0—Data Buffer:
Register 0 contains the results of the latest conversion when read. Depending on the Start Mode selected, reading or writing to this register may start the next conversion.

Register 1—CONTROL Register:

Bit 0 (DAV status when READ/DAVACK acknowledge when a ONE is written):
Reading DAV = 1 indicates that new data is available or a calibration is complete. DAV will be cleared automatically when the data is read. This bit can be explicitly acknowledged by writing a ONE to it; writing a zero has no effect. The $\overline{DAV}$ output pin always reflects the DAV status bit.

Bit 1 (BUSY status when READ/RESET when a ONE is written):
Reading BUSY = 1 indicates that a conversion or calibration is in progress. Writing a ONE will force a chip reset. Writing a zero has no effect.

RESET Default Conditions:

The Control register will automatically be cleared. The Data Buffer register will be unchanged. The Calibration register is not cleared after a reset, however the ADRDY bit is cleared. Since the DAV status bit is cleared, the $\overline{DAV}$ output is inactivated (high). The SYNC pin is forced to be an input as a result of clearing the M/S bit in the Control register.

Bit 2 (ADRDY status when READ/DOCAL request when a ONE is written):
Reading ADRDY = 0 indicates that the converter has not been calibrated since the last reset, and ADRDY = 1 indicates that it has been calibrated since the last reset. Writing a ONE will force the converter to do a calibration; writing a zero has no effect.

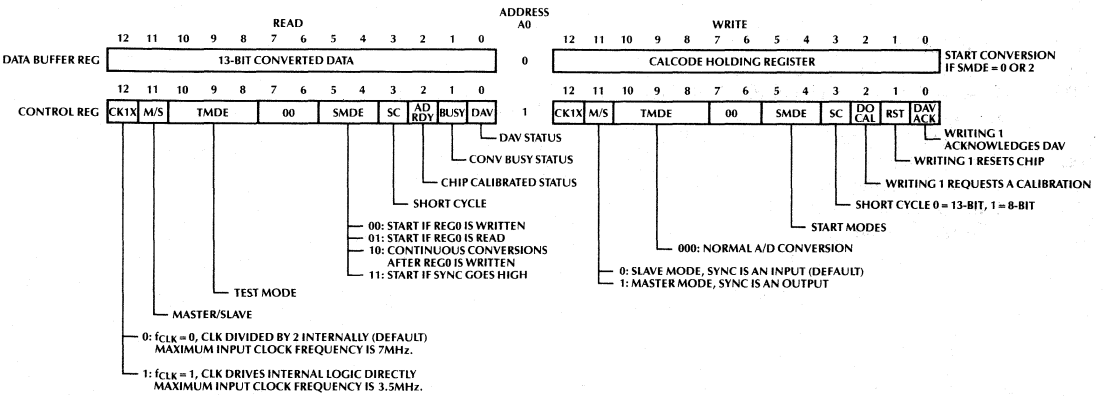


Figure 9. Register Description

FUNCTIONAL DESCRIPTION (Continued)

Bit 3 (SC: Short cycle select):
Selects 8 or 13 bit conversions.

SC = 0: 13-bit conversion (default)
SC = 1: 8-bit conversion (short cycle)

Bits 4,5 (SMDE: Start Mode):
Defines Start Conversion mode.

Bits 5,4

00	Start Conversion upon writing to register 0 (default)
01	Start Conversion upon reading register 0
10	Start Continuous Conversions upon writing to register 0.
11	Start on external SYNC input going high (Requires Slave mode: M/S = 0)

Bits 7,6 (reserved):
These bits are reserved by Micro Linear and must be written as zero.

Bits 10,9,8 (TMDE: test mode select bits)

These bits are used for diagnostic purposes only and normally not accessed during operation. The default value of TMDE is 000 which selects a normal A/D conversion. See Diagnostics for more information.

TMDE	Description
000	Normal A/D Conversion
001	Reserved by Micro Linear (Do Not Use)
010	CALWR Operation
011	CALRD Operation
100	System Offset
101	Common-mode
110	Plus Full Scale
111	Minus Full Scale

Bit 11 (M/S: Master/Slave bit):

Dictates whether the SYNC pin is an input or an output. Upon RESET, this bit is cleared.

M/S = 0: Slave Mode	SYNC is an input which is used to trigger a conversion if SMDE = 11.
M/S = 1: Master Mode	SYNC is an output. At the beginning of every conversion, SYNC is high for 4 internal clocks.

Bit 12 (CK1X: clock select bit):

Selects whether the external clock will be divided by two or used directly as the internal clock. See Clock section for a detailed explanation.

CK1X = 0:	the external clock is divided by two and used as the internal clock. This is referred to as CLK Mode = 0.
CK1X = 1:	the external clock input is used directly as the internal clock. This is referred to as CLK Mode = 1.

FUNCTIONAL DESCRIPTION (Continued)

GENERAL OPERATING INFORMATION

CONVERSION-START PROTOCOL

There are four different ways to start a conversion. They are defined by SMDE bits 4 and 5 in the Control Register.

SMDE Bits 5,4

00: A write to register 0 will start a conversion. During a conversion, if another write is issued to register 0, the "Start Conversion" command will be latched and another conversion will immediately follow the current one. To insure that the second write will be latched, it must occur at least 3 internal clocks after the first write. Only one additional write will be latched; multiple writes within a conversion will only yield one more conversion.

01: Reading the data from the previous conversion starts the next conversion.

10: This mode causes continuous conversions; the next conversion begins immediately after the previous conversion ends. Writing to register 0 will start the first conversion; thereafter the converter runs continuously. This mode yields the maximum conversion rate.

11: The SYNC input triggers the start of a conversion. The M/S bit in the Control Register must be cleared, placing the chip in the slave mode.

Note: The external activation signals for Start Modes 0, 1, and 3 are synchronized internally to the system clock. If periodic sampling is required using these Start Modes, the SYNC, $\overline{RD}$, or $\overline{WR}$ pulses must be synchronized to the system clock. Start Mode 2 guarantees periodic sampling.

DOUBLE-BUFFERED DATA REGISTER

The A/D conversion result is double-buffered using the Data Buffer register and the A/D Data register. The actual End-Of-Conversion (EOC) does not correspond with the $\overline{DAV}$ output going low. The $\overline{DAV}$ output goes low 16 internal clocks after the EOC. From the time $\overline{DAV}$ output goes LOW, the user has one full conversion time (80 or 110 internal clocks) minus 16 internal clocks to read the data as shown in Figure 10.

SELF CALIBRATION

Setting the DOCAL bit issues a calibration request to the chip. When calibration is done, the DAV status bit is set and the $\overline{DAV}$ output goes low.

A calibration requires 8,260 internal clocks. Using a 7MHz clock (CLK Mode = 0), this is approximately 2 ms. Power supplies and external voltage reference must be stable before issuing a request for calibration.

The ML2233 should be calibrated before any conversions are attempted. Calibrations must not be performed simultaneously with conversions. Before requesting a calibration, the user may want to read the Busy status bit to make sure that the converter is idle. Polling the chip while the calibration is in progress is not recommended.

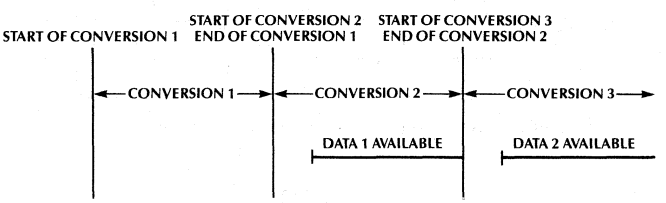


Figure 10

FUNCTIONAL DESCRIPTION (Continued)

CLOCK

The ML2233 has the option of dividing the clock at the CLK pin by 2, or using it directly to drive the internal logic. This option is selected through the CK1X bit in the Control register. When CK1X = 0 the clock is divided by 2. This is referred to as CLK Mode = 0. The clock at the CLK pin is referred to as the External clock, and the Internal Clock is the External clock divided by 2. When CK1X = 1, the clock at the CLK pin drives the internal logic directly, therefore this clock is referred to as the Internal clock. This is also known as CLK Mode = 1. All internally clocked logic is positive edge triggered.

CLK Mode = 0:

There are two advantages to CLK Mode 0. This is the only Mode that allows an external crystal to be used. CLK Mode 1 cannot operate with an external crystal, the CLK pin must be driven. The second advantage of CLK Mode 0 is that the duty cycle for a driven clock is less stringent than in CLK Mode 1. (Refer to t_{CLK0} and t_{CLK1} in AC Electrical Characteristics for CLK Mode 0 and 1 timing requirements, respectively.)

On power up the state of the divide by two flip-flop is indeterminate. Therefore the relationship between the internal clock and the external clock at the CLK pin can have one of two possibilities as shown in Figure 11. As a result the following should be considered.

t_{WRCK}, t_{RDCK}, and t_{SYNCCK} specs, ($\overline{RD}$, $\overline{WR}$, and SYNC set-up times to Start of Conversion), will be as shown in the data sheet, or the data sheet specs plus one external clock period. Since these specifications are with respect to the rising edge of the external clock, it is not known whether this rising edge corresponds to the rising edge or falling edge of the internal clock. Therefore there is an uncertainty of one external clock period.

If periodic sampling is necessary and Start Mode 0,1, or 3 is used, the external start pulse (either $\overline{RD}$, $\overline{WR}$, or SYNC) must be synchronous to the external clock, meet the setup time, and be an even number of external clock periods. If the start pulse were an odd number of external clock periods, half the pulses would correspond with the rising edge of the internal clock, and the other half would correspond with the falling edge of the internal clock. Therefore the sampling period would change by one external clock period every sample. Start Mode 2 guarantees periodic sampling regardless of the CLK mode.

CLK Mode = 1:

This mode eliminates the requirement that external start pulses must be an even number of external clock periods. However periodic sampling still requires that the start pulse be synchronous to the external clock, and the setup time must be met. CLK Mode 1 also eliminates the uncertainty of the t_{WRCK}, t_{RDCK}, and t_{SYNCCK} requirements.

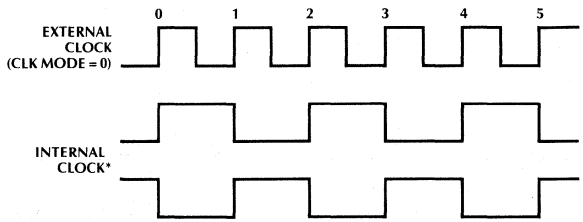


Figure 11

FUNCTIONAL DESCRIPTION (Continued)

DIAGNOSTICS

Diagnostic routines may be run after power up or any other time to ensure proper operation. The diagnostic features, which are software selectable, don't require external hardware. Both the analog and digital sections can be tested.

The ML2233 is placed in the diagnostic mode via the TMDE field in the Control Register. Once the ML2233 is placed in one of the diagnostic modes, a conversion must be executed before the results can be read. As with all conversions, $\overline{DAV}$ will be activated upon completion.

ANALOG CONVERSION DIAGNOSTICS

TMDE = 000: Normal Operation
Selects normal A/D conversion. Default condition after a software reset.

TMDE = 001: Reserved by Micro Linear.

TMDE = 010: CALWR operation
The data in Write register 0 (CALCODE Holding Register), is transferred into the converter's Calibration register when a "Start Conversion" is issued. A dummy conversion occurs and the $\overline{DAV}$ output goes LOW to indicate that the operation is complete.

TMDE = 011: CALRD operation
The contents of the Calibration register are transferred through the A/D Data register and loaded into the Data Buffer register. A dummy 8-bit conversion occurs and $\overline{DAV}$ output goes LOW to indicate that the CALRD operation is complete.

TMDE = 100: System Offset
The positive and negative inputs to the Sample and Hold are tied to analog ground. With this setting, converted data will give the offset of the A/D converter and Sample/Hold combination. The $V_{IN}+$ and $V_{IN}-$ pins will remain in a high impedance state while in this mode.

TMDE = 101: Common-mode
Both the positive and negative inputs of the Sample and Hold are tied to V_{REF}. The results of a conversion in this test mode indicates how well the converter is rejecting a common mode signal.

TMDE = 110: Positive Full Scale
This test mode connects the positive input of the Sample and Hold to V_{REF} and the negative input of the Sample and Hold to analog ground. The result of converting in this test mode is a value near positive full scale.

TMDE = 111: Negative Full Scale
This test mode connects the positive input of the Sample and Hold to analog ground and the negative input to V_{REF}. The result of converting in this test mode is a value near negative full scale.

DIGITAL LOOPBACK

The ML2233's architecture provides a way for the microprocessor to indirectly read and write to the A/D converter's calibration register and data register via a CALRD and CALWR. Figure 12 illustrates this architecture. This in effect allows a digital loopback.

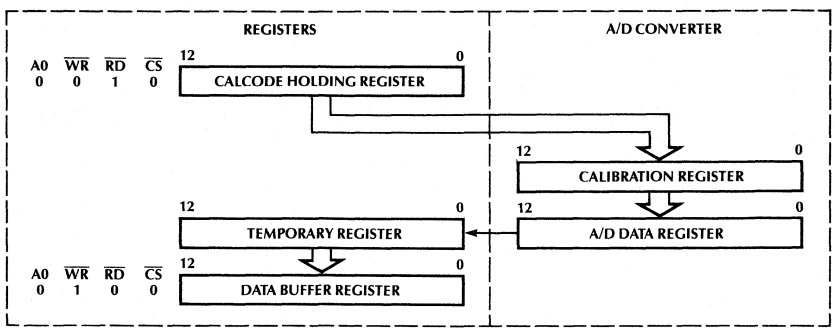


Figure 12. Digital Loopback

FUNCTIONAL DESCRIPTION (Continued)

When the TMDE bits are set to 010 CAL WRITE (CALWR), and a Start Conversion is issued in any one of the four modes, the contents of the CALCODE Holding register is transferred into the A/D converter's Calibration register. When the TMDE bits are set to 011 CAL READ (CALRD), and a Start Conversion is issued, the contents of the Calibration register are transferred through the A/D's Data register into the Data Buffer register. The result of these two operations is a complete loopback from the CALCODE Holding register through the A/D converter and back into the Data buffer register. This loopback provides user assurance that all the paths are clear and there are no stuck bits.

Note: When a CALWR is done, the previous calibration value is lost. The correct calibration value must be restored before the converter is used to convert data.

CALIBRATION PASS/FAIL TEST

The CALRD can be used as a way to verify a successful calibration. After a calibration is completed, the CALRD may be issued in order to read the contents of the Calibration register. If the Low Byte (lower 8 bits) of the data buffer register are ones after executing a CALRD, the calibration failed; otherwise the calibration is successful.

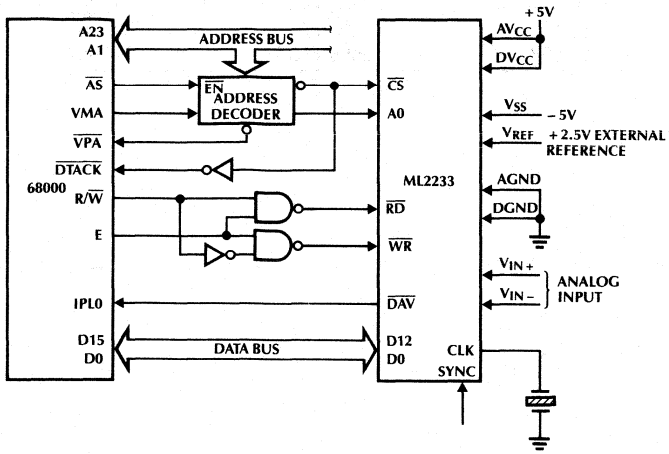


Figure 13. Interfacing to 68000 Microprocessor

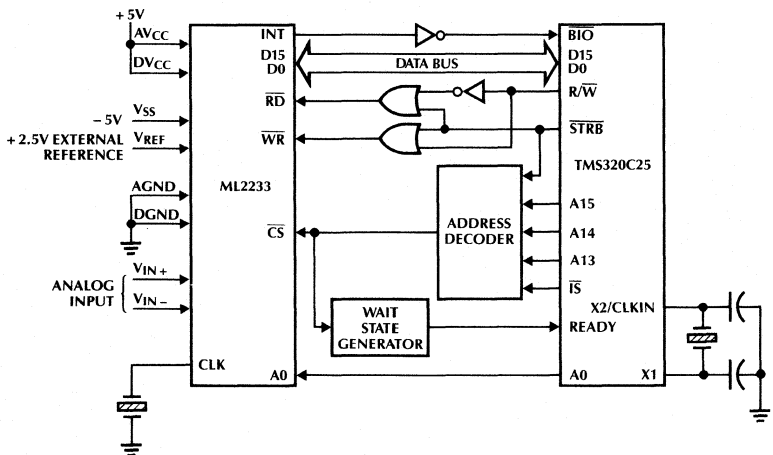


Figure 14. Interfacing to TMS320C25 Digital Signal Processor

ORDERING INFORMATION

PART NUMBER	MAXIMUM LINEARITY ERROR	MAXIMUM TOTAL UNADJUSTED ERROR	MINIMUM CONVERSION	PACKAGE
ML2233BCJ	±¾ LSB	±1½ LSB	31.5μs	Hermetic DIP
ML2233CCJ	±1 LSB	±2½ LSB	31.5μs	Hermetic DIP
ML2233DCJ	±1 LSB	±2½ LSB	44.0μs	Hermetic DIP

ML2252, ML2259

μP Compatible 8-Bit A/D Converters with 2- or 8-Channel Multiplexer

GENERAL DESCRIPTION

The ML2252 and ML2259 combine an 8-bit A/D converter, 2- or 8-channel analog multiplexer, and a microprocessor compatible 8-bit parallel interface and control logic in a single monolithic CMOS device.

Easy interface to microprocessors is provided by the latched and decoded multiplexer address inputs and a double buffered three-state data bus. These analog-to-digital converters allow the microprocessor to operate completely asynchronous to the converter clock.

The built in sample and hold function provides the ability to digitize a 5V, 50kHz sine wave to 8-bit accuracy. The differential comparator design provides low power supply sensitivity to DC and AC variations. The voltage reference can be externally set to any value between ground and V_{CC}, thus allowing a full conversion over a relatively small span if desired. All parameters are guaranteed over temperature with a power supply voltage of 5V ±10%.

The device is suitable for a wide range of applications from process and machine control to consumer, automotive, and telecommunication applications.

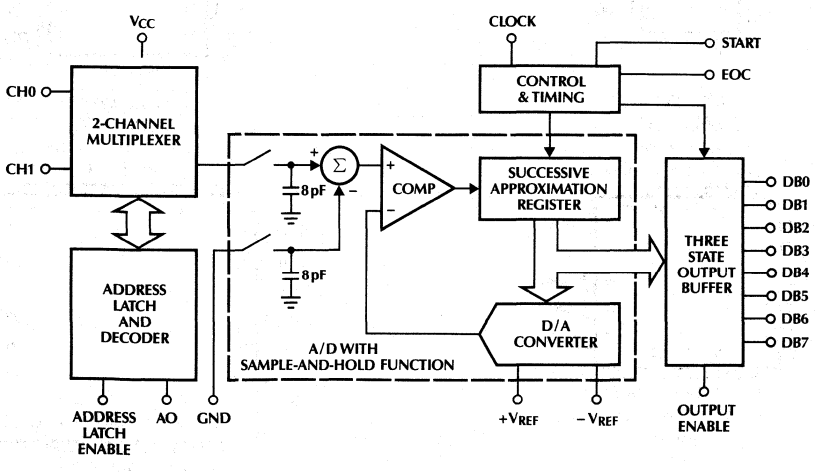
FEATURES

- Conversion time (f_{CLK} = 1.46MHz) 6.6μs
- Total unadjusted error ±1/2LSB or ±1LSB
- No missing codes
- Sample and hold 390ns acquisition
- Capable of digitizing a 5V, 50kHz sine wave
- 2- or 8-channel input multiplexer
- 0V to 5V analog input range with single 5V power supply
- Operates ratiometrically or with up to 5V voltage reference
- No zero or full scale adjust required
- Analog input protection 25mA (min) per input
- Continuous conversion mode
- Low power dissipation 15mW MAX
- TTL and CMOS compatible digital inputs and outputs
- Standard 20-pin or 28-pin DIP or PCC
- Temperature range 0°C to +70°C, or −40°C to +85°C, or −55°C to +125°C

2

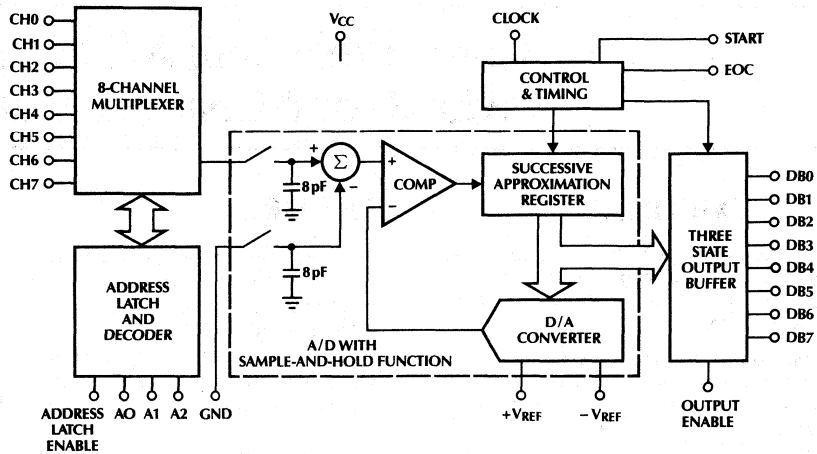
BLOCK DIAGRAMS

ML2252



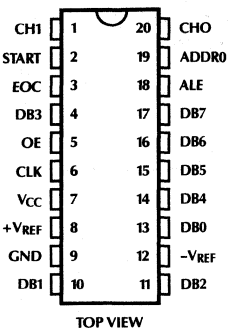
BLOCK DIAGRAMS (Continued)

ML2259



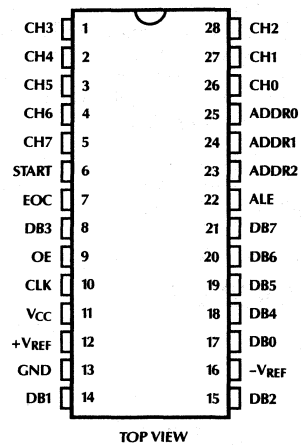
PIN CONNECTIONS

ML2252
20-Pin DIP



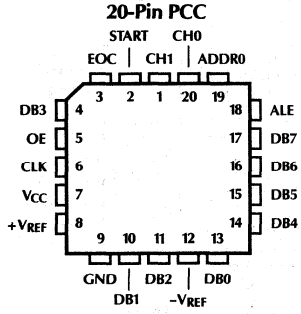
TOP VIEW

ML2259
28-Pin DIP



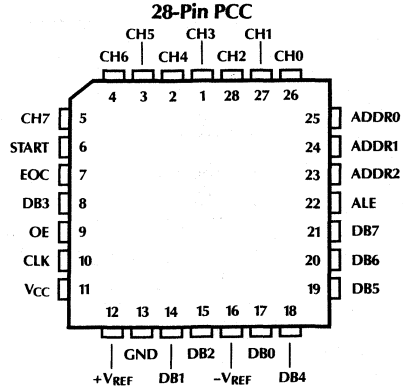
TOP VIEW

ML2252
20-Pin PCC



TOP VIEW

ML2259
28-Pin PCC



TOP VIEW

PIN DESCRIPTION

PIN # ML2252	PIN # ML2259	NAME	FUNCTION
	1	CH3	Analog input 3.
	2	CH4	Analog input 4.
	3	CH5	Analog input 5.
	4	CH6	Analog input 6.
	5	CH7	Analog input 7.
2	6	START	Start of conversion. Active high digital input pulse initiates conversion.
3	7	EOC	End of conversion. This output goes low after a START pulse occurs, stays low for the entire A/D conversion, and goes high after conversion is completed. Data on DB0-DB7 is valid on rising edge of EOC and stays valid until next EOC rising edge.
4	8	DB3	Data output 3.
5	9	OE	Output enable input. When OE = 0, DB0-DB7 are in high impedance state; OE = 1, DB0-DB7 are active outputs.
6	10	CLK	Clock. Clock input provides timing for A/D converter, S/H, and digital interface.
7	11	V_{CC}	Positive supply. 5 V ± 10%.
8	12	$+V_{REF}$	Positive reference voltage.
9	13	GND	Ground. 0 V, all analog and digital inputs or outputs are referenced to this point.
10	14	DB1	Data output 1.
11	15	DB2	Data output 2.
12	16	$-V_{REF}$	Negative reference voltage.
13	17	DB0	Data output 0.
14	18	DB4	Data output 4.
15	19	DB5	Data output 5.
16	20	DB6	Data output 6.
17	21	DB7	Data output 7.
18	22	ALE	Address latch enable. Input to latch in the digital address (ADDR2-0) on the rising edge of the multiplexer.
	23	ADDR2	Address input 2 to multiplexer. Digital input for selecting analog input.
	24	ADDR1	Address input 1 to multiplexer. Digital input for selecting analog input.
19	25	ADDR0	Address input 0 to multiplexer. Digital input for selecting analog input.
20	26	CH0	Analog input 0.
1	27	CH1	Analog input 1.
	28	CH2	Analog input 2.

ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage, V_{CC} ..... 6.5 V
Voltage
- Logic Inputs ..... −0.3 V to V_{CC} +0.3 V
- Analog Inputs ..... −0.3 V to V_{CC} +0.3 V

Input Current per Pin (Note 2) ..... ±25 mA
Storage Temperature ..... −65°C to +150°C
Package Dissipation
- at T_A = 25°C (Board Mount) ..... 875 mW

Lead Temperature (Soldering 10 sec.)
- Dual-In-Line Package (Plastic) ..... 260°C
- Dual-In-Line Package (Ceramic) ..... 300°C
- Molded Chip Carrier Package
  - Vapor Phase (60 sec.) ..... 215°C
  - Infrared (15 sec.) ..... 220°C

OPERATING CONDITIONS

Supply Voltage, V_{CC} ..... 4.5 V_{DC} to 6.3 V_{DC}
Temperature Range (Note 3) ..... $T_{MIN} \leq T_A \leq T_{MAX}$
- ML2252BMJ, ML2252CMJ ..... −55°C to +125°C
- ML2259BMJ, ML2259CMJ
- ML2252BIJ, ML2252CIJ ..... −40°C to +85°C
- ML2259BIJ, ML2259CIJ
- ML2252BCP, ML2259BCP ..... 0°C to +70°C
- ML2252BCQ, ML2259BCQ
- ML2252CCP, ML2259CCP
- ML2252CCQ, ML2259CCQ

ELECTRICAL CHARACTERISTICS

Unless otherwise specified $T_A = T_{MIN}$ to T_{MAX}, $V_{CC} = +V_{REF} = 5V \pm 10\%$, $-V_{REF} = GND$ and $f_{CLK} = 1.46MHz$.

PARAMETER	NOTES	CONDITIONS	ML2252B, ML2259B MIN	ML2252B, ML2259B TYP NOTE 4	ML2252B, ML2259B MAX	ML2252C, ML2259C MIN	ML2252C, ML2259C TYP NOTE 4	ML2252C, ML2259C MAX	UNITS
CONVERTER AND MULTIPLEXER CHARACTERISTICS									
Total Unadjusted Error	5, 7	$V_{REF} = V_{CC}$			$\pm 1/2$			± 1	LSB
$+V_{REF}$ Voltage Range	6		$-V_{REF}$		$V_{CC}+0.1$	$-V_{REF}$		$V_{CC}+0.1$	V
$-V_{REF}$ Voltage Range	6		GND − 0.1		$+V_{REF}$	GND − 0.1		$+V_{REF}$	V
Reference Input Resistance	5		14	20	28	14	20	28	kΩ
Analog Input Range	5, 8		GND − 0.1		$V_{CC}+0.1$	GND − 0.1		$V_{CC}+0.1$	V
Power Supply Sensitivity	6	DC $V_{CC} = 5V \pm 10\%$		$\pm 1/32$	$\pm 1/4$		$\pm 1/32$	$\pm 1/4$	LSB
		$100mV_{P-P}$ 100kHz Sine on V_{CC}, $V_{IN} = 0$		$\pm 1/16$			$\pm 1/16$		LSB
I_{Off}, Off Channel Leakage Current (Note 9)	5, 9	On Channel = V_{CC} Off Channel = 0V	−1			−1			μA
		On Channel = 0V Off Channel = V_{CC}			1			1	μA
I_{On}, On Channel Leakage Current (Note 9)	5, 9	On Channel = 0V Off Channel = V_{CC}	−1			−1			μA
		On Channel = V_{CC} Off Channel = 0V			1			1	μA

SYMBOL	PARAMETER	NOTES	CONDITIONS	MIN	TYP NOTE 4	MAX	UNITS
DIGITAL AND DC CHARACTERISTICS							
$V_{IN(1)}$	Logical "1" Input Voltage	5		2.0			V
$V_{IN(0)}$	Logical "0" Input Voltage	5				0.8	V
$I_{IN(1)}$	Logical "1" Input Current	5	$V_{IN} = V_{CC}$			1	μA
$I_{IN(0)}$	Logical "0" Input Current	5	$V_{IN} = 0V$	−1			μA
$V_{OUT(1)}$	Logical "1" Output Voltage	5	$I_{OUT} = -2mA$	4.0			V
$V_{OUT(0)}$	Logical "0" Output Voltage	5	$I_{OUT} = 2mA$			0.4	V
I_{OUT}	Three-State Output Current	5	$V_{OUT} = 0V$	−1			μA
			$V_{OUT} = V_{CC}$			1	μA
I_{CC}	Supply Current	5			1.5	3	mA
AC AND DYNAMIC PERFORMANCE CHARACTERISTICS (Note 10)							
t_{ACQ}	Sample & Hold Acquistion				1/2		$1/f_{CLK}$
f_{CLK}	Clock Frequency	5		10		1460	kHz
t_C	Conversion Time				8.5	8.5 + 250ns	$1/f_{CLK}$
SNR	Signal to Noise Ratio		$V_{IN} = 51kHz$, 5V Sine. $f_{CLK} = 1.46MHz$ ($f_{SAMPLING} \cong 150kHz$). Noise is Sum of All Nonfundamental Components up to 1/2 of $f_{SAMPLING}$		47		dB
THD	Total Harmonic Distortion		$V_{IN} = 51kHz$, 5V Sine. $f_{CLK} = 1.46MHz$ ($f_{SAMPLING} \cong 150kHz$). THD is Sum of 2, 3, 4, 5 Harmonics Relative to Fundamental		−60		dB

ELECTRICAL CHARACTERISTICS (Continued)

Unless otherwise specified $T_A = T_{MIN}$ to T_{MAX}, $V_{CC} = +V_{REF} = 5V \pm 10\%$, $-V_{REF} = GND$ and $f_{CLK} = 1.46MHz$.

SYMBOL	PARAMETER	NOTES	CONDITIONS	MIN	TYP NOTE 4	MAX	UNITS
AC AND DYNAMIC PERFORMANCE CHARACTERISTICS (Note 10) (Continued)							
IMD	Intermodulation Distortion		$V_{IN} = f_A + f_B$. $f_A = 49kHz$, 2.5V Sine. $f_B = 47.8kHz$, 2.5V Sine, $f_{CLK} = 1.46MHz$ ($f_{SAMPLING} \cong 150kHz$). IMD is $(f_A + f_B)$, $(f_A - f_B)$, $(2f_A + f_B)$, $(2f_A - f_B)$, $(f_A + 2f_B)$, $(f_A - 2f_B)$ Relative to Fundamental		-60		dB
FR	Frequency Response		$V_{IN} = 0$ to 50kHz. 5V Sine Relative to 1kHz		0.1		dB
t_{DC}	Clock Duty Cycle	6, 11		40		60	%
t_{EOC}	End of Conversion Delay	5			1/2	1/2 +250ns	$1/f_{CLK}$
t_{WS}	Start Pulse Width	5		50			ns
t_{SS}	Start Pulse Setup Time	6, 12	Synchronous Only	40			ns
t_{WALE}	Address Latch Enable Pulse Width	5		50			ns
t_S	Address Setup	5		0			ns
t_H	Address Hold	5		50			ns
t_{H1}, t_{H0}	Output Enable for DB0-DB7	6	Figure 1, $C_L = 50pF$			100	ns
		6	Figure 1, $C_L = 10pF$			50	ns
t_{1H}, t_{0H}	Output Disable for DB0-DB7	6	Figure 1, $C_L = 50pF$			100	ns
		6	Figure 1, $C_L = 10pF$			50	ns
C_{IN}	Capacitance of Logic Input				5		pF
C_{OUT}	Capacitance of Logic Outputs				10		pF

Note 1: Absolute maximum ratings are limits beyond which the life of the integrated circuit may be impaired. All voltages unless otherwise specified are measured with respect to ground.

Note 2: When the input voltage (V_{IN}) at any pin exceeds the power supply rails ($V_{IN} < GND - 0.1V$ or $V_{CC} + 0.1V$) the absolute value of current at that pin should be limited to 25mA or less.

Note 3: $-55°C$ to $+125°C$ operating temperature range devices are 100% tested at temperature extremes with worst-case test conditions. $-40°C$ to $+85°C$ operating temperature range devices are 100% tested with temperature limits guaranteed by 100% testing, sampling, or by correlation with worst-case test conditions.

Note 4: Typicals are parametric norm at 25°C.

Note 5: Parameter guaranteed and 100% production tested.

Note 6: Parameter guaranteed. Parameters not 100% tested are not in outgoing quality level calculation.

Note 7: Total unadjusted error includes offset, full-scale, linearity, multiplexer and sample and hold errors.

Note 8: For $-V_{REF} \geq V_{IN}(+)$ the digital output code will be 0000 0000. Two on-chip diodes are tied to each analog input which will forward conduct for analog input voltages one diode drop below ground or one diode drop greater than the V_{CC} supply. Be careful, during testing at low V_{CC} levels (4.5V), as high level analog inputs (5V) can cause this input diode to conduct–especially at elevated temperatures, and cause errors for analog inputs near full-scale. The spec allows 100mV forward bias of either diode. This means that as long as the analog V_{IN} or V_{REF} does not exceed the supply voltage by more than 100mV, the output code will be correct. To achieve an absolute $0V_{DC}$ to $5V_{DC}$ input voltage range will therefore require a minimum supply voltage of $4.900V_{DC}$ over temperature variations, initial tolerance and loading.

Note 9: Leakage current is measured with the clock not switching.

Note 10: $C_L = 50pF$, timing measured at 50% point.

Note 11: A 40% to 60% clock duty cycle range insures proper operation at all clock frequencies. In the case that an available clock has a duty cycle outside of these limits, the minimum time the clock is high or the minimum time the clock is low must be at least 40ns. The maximum time the clock can be high or low is 60μs.

Note 12: The conversion start setup time requirement only needs to be satisfied if a conversion must be synchronized to a given clock rising edge. If the setup time is not met, start conversion will have an uncertainty of one clock pulse.

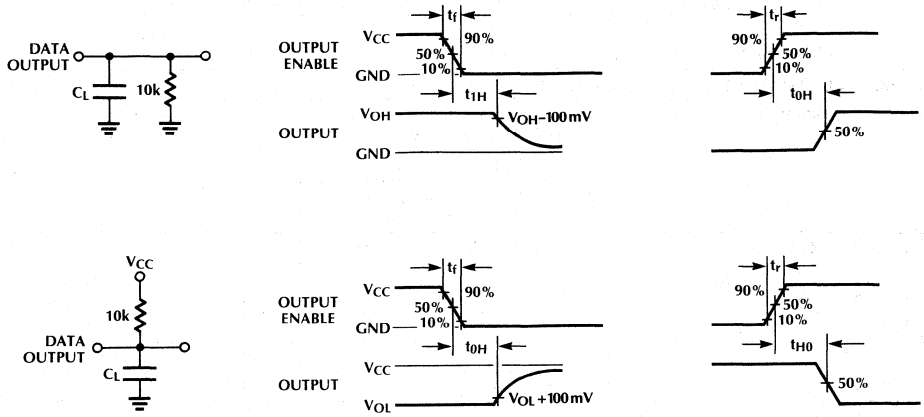


Figure 1. High Impedance Test Circuits and Waveforms

TYPICAL PERFORMANCE CURVES

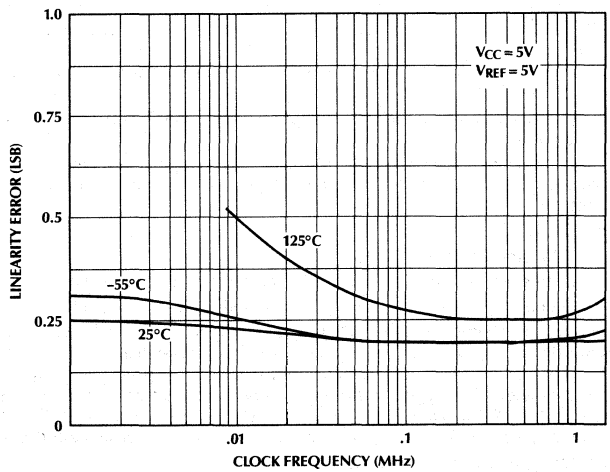


Figure 2. Linearity Error vs f_{CLK}

TYPICAL PERFORMANCE CURVES (Continued)

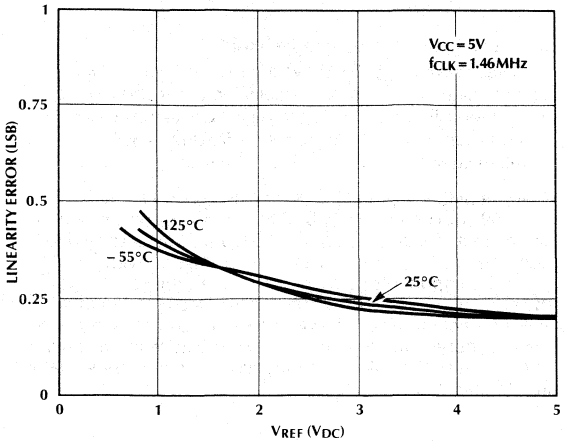


Figure 3. Linearity Error vs V_{REF} Voltage

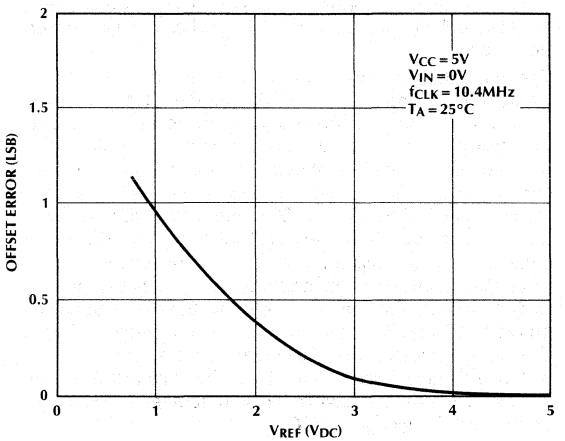


Figure 4. Unadjusted Offset Error vs V_{REF} Voltage

2

1.0 FUNCTIONAL DESCRIPTION

1.1 Multiplexer Addressing

The ML2252 and ML2259 contain a single ended analog multiplexer. A particular input channel is selected by using the address decoder. The relationship between the address inputs, ADDR0-ADDR2, and the analog input selected is shown in Table 1. The address inputs are latched into the decoder on the rising edge of the address latch signal ALE.

Table 1. Multiplexer Address Decoding

ML2252

Selected Analog Channel	Address Input
CH0	0
CH1	1

ML2259

Selected Analog Channel	Address Input ADDR2	ADDR1	ADDR0
CH0	0	0	0
CH1	0	0	1
CH2	0	1	0
CH3	0	1	1
CH4	1	0	0
CH5	1	0	1
CH6	1	1	0
CH7	1	1	1

1.2 A/D Converter

The A/D converter uses successive approximation to perform the conversion. The converter is composed of the successive approximation register, the DAC and the comparator.

The DAC generates the precise levels that determine the linearity and accuracy of the conversion. The DAC is composed of a capacitor upper array and a resistor lower array. The capacitor upper array generates the 4 MSB decision levels while the series resistor lower array generates the 4 LSB decision levels. A switch decoder tree is used to decode the proper level from both arrays.

The capacitor/resistor array offers fast conversion, superior linearity and accuracy since matching is only required between $2^4 = 16$ elements (as opposed to $2^8 = 256$ elements in conventional designs). And since the levels are based on the ratio of capacitors to capacitors and resistors to resistors, the accuracy and long term stability of the converter is improved. This also guarantees monotonicity and no missing codes, as well as eliminating any linearity temperature or power supply dependence.

The successive approximation register is a digital block used to store the bit decisions from the conversion.

The comparator design is unique in that it is fully differential and auto zeroed. The fully differential architecture provides excellent noise immunity, excellent power supply rejection, and wide common mode range. The comparator is auto zeroed at the start of each conversion in order to remove any DC offset and full-scale gain error, thus improving accuracy and linearity.

Another advantage of the capacitor array approach used in the ML2252 and ML2259 is the inherent sample-and-hold function. This true S/H allows an accurate conversion to be done on the input even if the analog signal is not stable.

1.0 FUNCTIONAL DESCRIPTION (Continued)

Linearity and accuracy are maintained for analog signals up to 1/2 the sampling frequency. As a result, input signals up to 50 kHz can be converted without degradation in linearity or accuracy.

The sequence of events during a conversion is shown in Figure 5. The rising edge of a START pulse resets the internal registers and initiates a conversion on the next rising edge of CLK providing that (tss) start pulse setup time is satisfied. If this setup time is not met, start conversion will have an uncertainty of one clock pulse. The input is then sampled for the next half CLK period until EOC goes low. EOC goes low on the falling edge of the next CLK pulse indicating that the conversion is now beginning. The actual conversion now takes place for the next eight CLK pulses, one bit for each CLK pulse. After the conversion is done, the data is updated on DB0-DB7 and EOC goes high on the rising edge of the 9th CLK pulse, indicating that the conversion has been completed and data is valid on DB0-DB7. The data will stay valid on DB0-DB7 until the next conversion updates the data word on the next rising edge of EOC.

A conversion can be interrupted and restarted at any time by a new START pulse.

1.3 Analog Inputs and Sample/Hold

The ML2252 and ML2259 have a true sample-and-hold circuit which samples both the selected input and ground simultaneously. These analog to digital converters can reject AC common mode signals from DC–50 kHz as well as maintain linearity for signals from DC–50 kHz.

The plot below (Figure 6) shows a 2048 point FFT of the ML2259 converting a 50 kHz, 0 to 5 V, low distortion sine wave input. The ML2252 and ML2259 sample and digitize at their specified accuracy, dynamic input signals with frequency components up to the Nyquist frequency (one-half the sampling rate). The output spectra yields precise measurements of input signal level, harmonic components, and signal to noise ratio up to the 8-bit level. The near ideal signal to noise ratio is maintained independent of increasing analog input frequencies to 50 kHz.

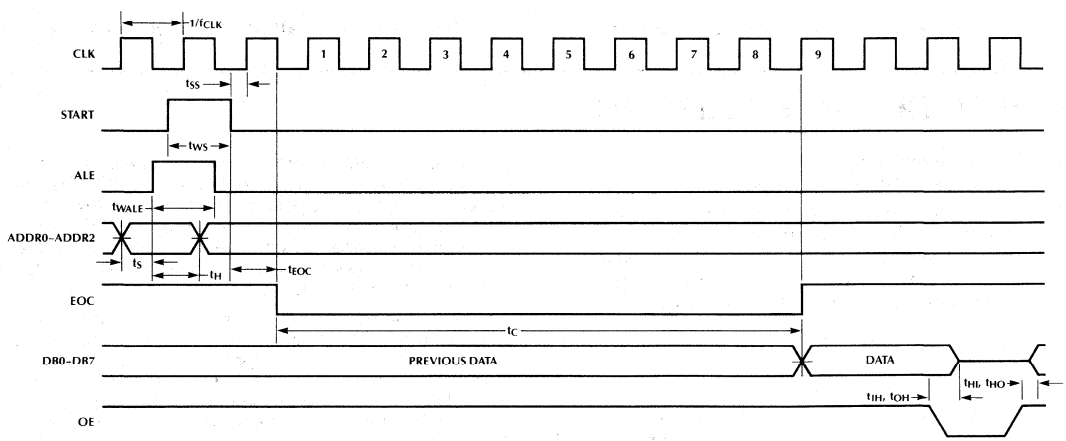


Figure 5. Timing Diagram

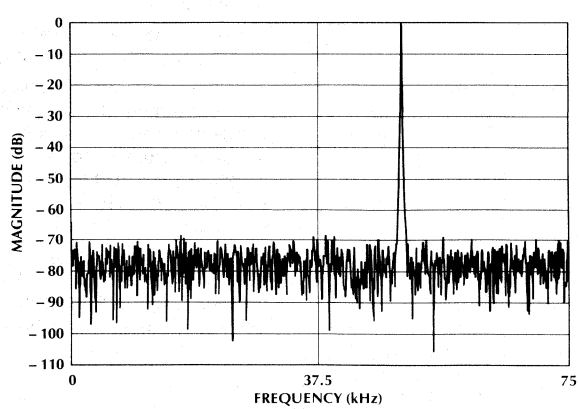


Figure 6. Output Spectrum

1.0 FUNCTIONAL DESCRIPTION (Continued)

The signal at the analog input is sampled during the interval when the sampling switch is open prior to conversion start. The sampling window (S/H acquisition time) is one half CLK period long and occurs one half CLK period after START goes low. When the sampling switch closes at the start of the S/H acquisition time, 8pF of capacitance is thrown onto the analog input. One half CLK period later, the sampling switch opens, the signal present at analog input is stored and conversion starts. Since any error on the analog input at the end of the S/H acquisition time will cause additional conversion error, care should be taken to insure adequate settling and charging time from the source. If more charging or settling time is needed to reduce these analog input errors, a longer CLK period can be used.

Each analog input has dual diodes to the supply rails, and a minimum of ±25mA (±100mA typically) can be injected into each analog input without causing latchup.

1.4 Reference

The voltage applied to the $+V_{REF}$ and $-V_{REF}$ inputs defines the voltage span of the analog input (the difference between V_{INMAX} and V_{INMIN}) over which the 256 possible output codes apply. The devices can be used in either ratiometric applications or in systems requiring absolute accuracy. The reference pins must be connected to a voltage source capable of driving the reference input resistance, typically 20k.

In a ratiometric system, the analog input voltage is proportional to the voltage used for the A/D reference. This voltage is typically the system power supply, so the $+V_{REF}$ pin can be tied to V_{CC} and $-V_{REF}$ tied to GND. This technique relaxes the stability requirements of the system reference as the analog input and A/D reference move together maintaining the same output code for a given input condition.

For absolute accuracy, where the analog input varies between specific voltage limits, the reference pins can be biased with a time and temperature stable voltage source.

$+V_{REF}$ and $-V_{REF}$ can be at any voltage between V_{CC} and GND. In addition, the difference between $+V_{REF}$ and $-V_{REF}$ can be set to small values for conversions over smaller voltage ranges. Particular care must be taken with regard to noise pickup, circuit layout and system error voltage sources when operating with a reduced span due to the increased sensitivity of the converter.

1.5 Power Supply and Reference Decoupling

A 10μF electrolytic capacitor is recommended to bypass V_{CC} to GND, using as short a lead length as possible. In addition, with clock frequencies above 1MHz, a 0.1μF ceramic disc capacitor should be used to bypass V_{CC} to GND.

If REF+ and REF− inputs are driven by long lines, they should be bypassed by 0.1μF ceramic disc capacitors at the reference input pins (pins 12, 16).

1.6 Dynamic Performance

Signal-to-Noise Ratio

Signal-to-noise ratio (SNR) is the measured signal to noise at the output of the converter. The signal is the rms magnitude of the fundamental. Noise is the rms sum of all the nonfundamental signals up to half the sampling frequency. SNR is dependent on the number of quantization levels used in the digitization process; the more the levels, the smaller the quantization noise. The theoretical SNR for a sine wave is given by

$$SNR = (6.02N + 1.76)dB$$

where N is the number of bits. Thus for ideal 8-bit converter, SNR = 49.92dB.

Harmonic Distortion

Harmonic distortion is the ratio of the rms sum of harmonics to the fundamental. Total harmonic distortion (THD) of the ML2252 or ML2259 are defined as

$$20 \log = \frac{(V_2^2 + V_3^2 + V_4^2 + V_5^2)^{1/2}}{V_1}$$

where V_1 is the rms amplitude of the fundamental and V_2, V_3, V_4, V_5 are the rms amplitudes of the individual harmonics.

Intermodulation Distortion

With inputs consisting of sine waves at two frequencies, f_A and f_B, any active device with nonlinearities will create distortion products, of order (m + n), at sum and difference frequencies of $mf_A + nf_B$, where m, n=0, 1, 2, 3 ... Intermodulation terms are those for which m or n is not equal to zero. The (IMD) intermodulation distortion specification includes the second order terms ($f_A + f_B$) and ($f_A - f_B$) and the third order terms ($2f_A + f_B$), ($2f_A - f_B$), ($f_A + 2f_B$), and ($f_A - 2f_B$) only.

1.7 Digital Interface

The analog inputs are selected by the digital addresses, ADDR0-ADDR2, and latched on the rising edge of ALE. This is described in the Multiplexer Addressing section.

A conversion is initiated by the rising edge of a START pulse. As long as this pulse is high, the internal logic is reset.

The sampling interval starts with the following CLK rising edge after a START falling edge and ends on the falling edge of CLK. The conversion starts and EOC goes low. The sampling clock is at least one half CLK period wide. Each bit conversion in the successive approximation process takes 1 CLK period. On the rising edge of the ninth CLK pulse, the digital output of the conversion is updated on the outputs DB0-DB7 and EOC goes high indicating the conversion is done and data on DB0-DB7 is valid.

One feature of the ML2252 and ML2259 is that the data is double buffered. This means that the outputs DB0-DB7 will stay valid until updated at the end of the next conversion and will not become invalid when the next conversion starts. This facilitates interfacing with external logic of μP.

The signal OE drives the data bus, DB0–DB7, into the high impedance state when held low. This allows the ML2252 and ML2259 to be tied directly to a μP system bus without any latches or buffers.

2

1.0 FUNCTIONAL DESCRIPTION (Continued)

1.7.1 Restart During Conversion

If the A/D is restarted (start goes low and returns high) during a conversion, the converter is reset and a new conversion is started. The output data latch is not updated if the conversion in process is not allowed to be completed. EOC will remain low and the output data latch is not updated.

1.7.2 Continuous Conversions

In the free-running, continuous conversion mode, the start input is tied to the (Figure 7) EOC output. An initialization pulse, following power-up, of momentarily forcing a logic high level is required to guarantee operation.

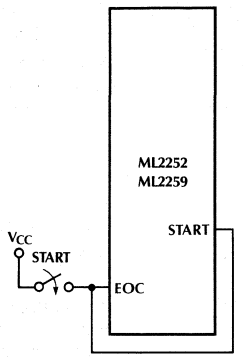


Figure 7. Continuous Conversion Mode

2.0 TYPICAL APPLICATIONS

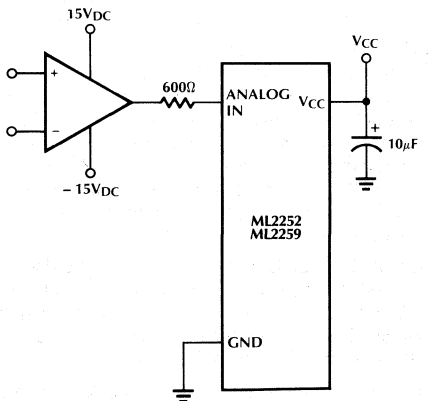


Figure 8. Protecting the Input

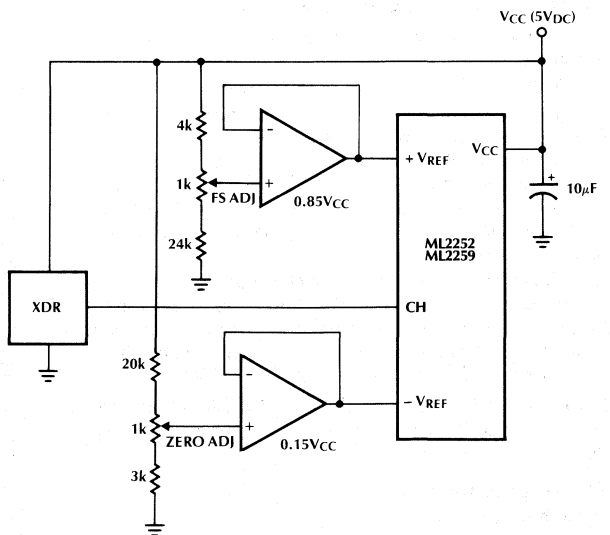


Figure 9. Operating with Ratiometric Transducers 15% of $V_{CC} \leq V_{XDR} \leq 85\%$ of V_{CC}

ORDERING INFORMATION

PART NUMBER	TOTAL UNADJUSTED ERROR	TEMPERATURE RANGE	PACKAGE
TWO ANALOG INPUTS, 20-PIN PACKAGE			
ML2252BMJ	±½LSB	−55°C to +125°C	HERMETIC DIP
ML2252BIJ		−40°C to +85°C	HERMETIC DIP
ML2252BCP		0°C to +70°C	MOLDED DIP
ML2252BCQ		0°C to +70°C	MOLDED PCC
ML2252CIJ	±1LSB	−40°C to +85°C	HERMETIC DIP
ML2252CCP		0°C to +70°C	MOLDED DIP
ML2252CCQ		0°C to +70°C	MOLDED PCC
EIGHT ANALOG INPUTS, 28-PIN PACKAGE			
ML2259BMJ	±½LSB	−55°C to +125°C	HERMETIC DIP
ML2259BIJ		−40°C to +85°C	HERMETIC DIP
ML2259BCP		0°C to +70°C	MOLDED DIP
ML2259BCQ		0°C to +70°C	MOLDED PCC
ML2259CIJ	±1LSB	−40°C to +85°C	HERMETIC DIP
ML2259CCP		0°C to +70°C	MOLDED DIP
ML2259CCQ		0°C to +70°C	MOLDED PCC

ML2258

μP Compatible 8-Bit A/D Converter with 8-Channel Multiplexer

GENERAL DESCRIPTION

The ML2258 combines an 8-bit A/D converter, 8-channel analog multiplexer, and a microprocessor compatible 8-bit parallel interface and control logic in a single monolithic CMOS device.

Easy interface to microprocessors is provided by the latched and decoded multiplexer address inputs and latched three-state outputs.

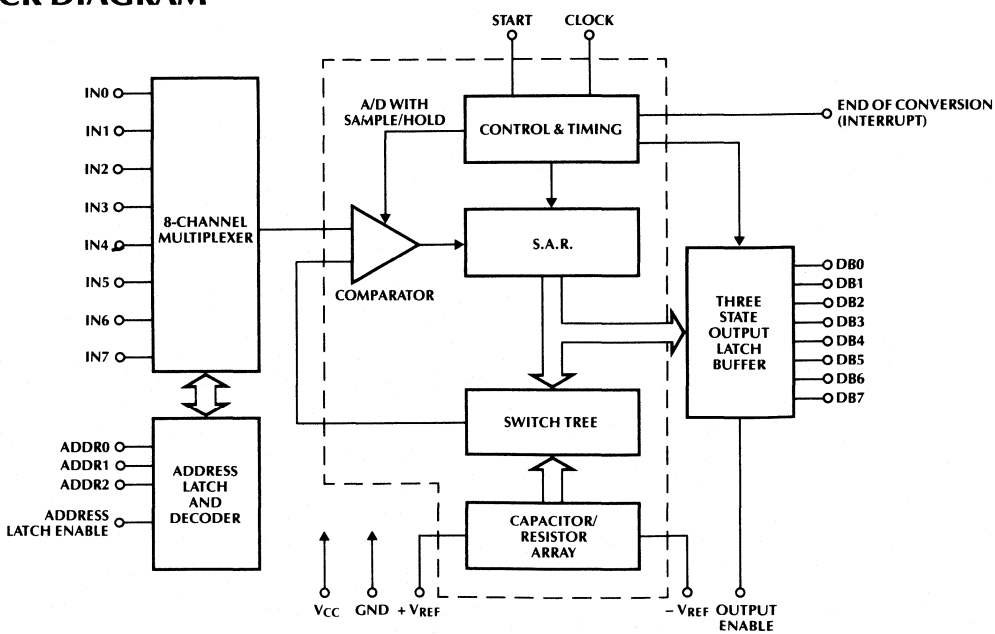
The device is suitable for a wide range of applications from process and machine control to consumer, automotive , and telecommunication applications.

The ML2258 is an enhanced pin compatible second source for the industry standard ADC0808/ADC0809. The ML2258 enhancements are faster conversion time, true sample and hold function, superior power supply rejection, wider reference range, and a double buffered data bus as well as faster digital timing. All parameters are guaranteed over temperature with a power supply voltage of 5V ± 10%.

FEATURES

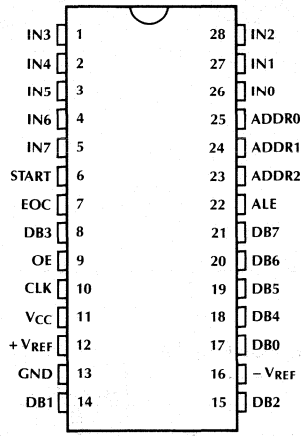
- Conversion time 6.6μs
- Total unadjusted error ± 1/2LSB or ± 1LSB
- No missing codes
- Sample and hold 390ns acquisition
- Capable of digitizing a 5V, 50kHz sine wave
- 8-input multiplexer
- 0V to 5V analog input range with single 5V power supply
- Operates ratiometrically or with up to 5V voltage reference
- No zero or full scale adjust required
- Analog input protection 25mA per input min
- Low power dissipation 3mA max
- TTL and CMOS compatible digital inputs and outputs
- Standard 28-pin DIP or surface mount PCC
- Superior pin compatible replacement for ADC0808 and ADC0809

BLOCK DIAGRAM



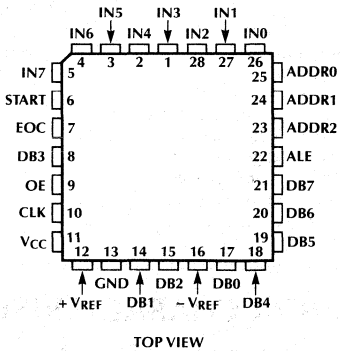
PIN CONNECTIONS

ML2258
28-PIN DIP



TOP VIEW

ML2258
28-PIN PCC



TOP VIEW

2

PIN DESCRIPTION

PIN NO.	NAME	FUNCTION
1	IN3	Analog input 3.
2	IN4	Analog input 4.
3	IN5	Analog input 5.
4	IN6	Analog input 6.
5	IN7	Analog input 7.
6	START	Start of conversion. Active high digital input pulse initiates conversion.
7	EOC	End of conversion. This output goes low after a START pulse occurs, stays low for the entire A/D conversion, and goes high after conversion is completed. Data on DB0–DB7 is valid on rising edge of EOC and stays valid until next EOC rising edge.
8	DB3	Data output 3.
9	OE	Output enable input. When OE = 0, DB0–DB7 are in high impedance state; OE = 1, DB0–DB7 are active outputs.
10	CLK	Clock. Clock input provides timing for A/D converter, S/H, and digital interface.
11	V_{CC}	Positive supply. 5V ± 10%.
12	$+V_{REF}$	Positive reference voltage.
13	GND	Ground. 0V, all analog and digital inputs or outputs are reference to this point.
14	DB1	Data output 1.
15	DB2	Data output 2.
16	$-V_{REF}$	Negative reference voltage.
17	DB0	Data output 0.
18	DB4	Data output 4.
19	DB5	Data output 5.
20	DB6	Data output 6.
21	DB7	Data output 7.
22	ALE	Address latch enable. Input to latch in the digital address (ADDR2–0) on the rising edge of the multiplexer.
23	ADDR0	Address input 0 to multiplexer. Digital input for selecting analog input.
24	ADDR1	Address input 1 to multiplexer. Digital input for selecting analog input.
25	ADDR2	Address input 2 to multiplexer. Digital input for selecting analog input.
26	IN0	Analog input 0.
27	IN1	Analog input 1.
28	IN2	Analog input 2.

ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage, V_{CC} 6.5V
Voltage
- Logic Inputs ..... −0.3V to V_{CC}+0.3V
- Analog Inputs ..... −0.3V to V_{CC}+0.3V

Input Current per Pin (Note 2) ..... ±25mA
Storage Temperature ..... −65°C to +150°C
Package Dissipation
- at T_A=25°C (Board Mount) 875mW

Lead Temperature (Soldering 10 sec.)
- Dual-In-Line Package (Plastic) ..... 260°C
- Dual-In-Line Package (Ceramic) ..... 300°C
- Molded Chip Carrier Package
  - Vapor Phase (60 sec.) ..... 215°C
  - Infrared (15 sec.) ..... 220°C

OPERATING CONDITIONS

Supply Voltage, V_{CC} ..... 4.5V_{DC} to 6.3V_{DC}
Temperature Range (Note 3) ..... $T_{MIN} \le T_A \le T_{MAX}$
- ML2258BMJ, ML2258CMJ ..... −55°C to +125°C
- ML2258BIJ, ML2258BIP
- ML2258BIQ, ML2258CIJ
- ML2258CIP, ML2258CIQ ..... −40°C to +85°C

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, $T_A = T_{MIN}$ to T_{MAX}, $V_{CC} = +V_{REF} = 5V \pm 10\%$, $-V_{REF}$ = GND and f_{CLK} = 10.24MHz

			ML2258B			ML2258C			
PARAMETER	**NOTES**	**CONDITIONS**	**MIN**	**TYP (NOTE 4)**	**MAX**	**MIN**	**TYP (NOTE 4)**	**MAX**	**UNITS**
Converter and Multiplexer									
Total Unadjusted Error	5,7	$V_{REF}=V_{CC}$			±1/2			±1	LSB
$+V_{REF}$ Voltage Range	6		$-V_{REF}$		V_{CC}+0.1	$-V_{REF}$		V_{CC}+0.1	V
$-V_{REF}$ Voltage Range	6		GND−0.1		$+V_{REF}$	GND−0.1		$+V_{REF}$	V
Reference Input Resistance	5		14	20	28	14	20	28	kΩ
Analog Input Range	5,8		GND−0.1		V_{CC}+0.1	GND−0.1		V_{CC}+0.1	V
Power Supply Sensitivity	6	DC $V_{CC}=5V\pm10\%$		±1/32	±1/4		±1/32	±1/4	LSB
		100mVp-p 100kHz Sine on V_{CC}, V_{IN}=0		±1/16			±1/16		LSB
I_{OFF}, Off Channel Leakage Current (Note 9)	5,9	On Channel=V_{CC} Off Channel=0V	−1			−1			µA
		On Channel=0V Off Channel=V_{CC}			1			1	µA
I_{ON}, On Channel Leakage Current (Note 9)	5,9	On Channel=0V Off Channel=V_{CC}	−1			−1			µA
		On Channel=V_{CC} Off Channel=0V			1			1	µA
Digital and DC									
$V_{IN(1)}$, Logical "1" Input Voltage	5		2.0			2.0			V
$V_{IN(0)}$, Logical "0" Input Voltage	5				0.8			0.8	V
$I_{IN(1)}$, Logical "1" Input Current	5	$V_{IN}=V_{CC}$			1			1	µA
$I_{IN(0)}$, Logical "0" Input Current	5	V_{IN}=0V	−1			−1			µA
$V_{OUT(1)}$, Logical "1" Output Voltage	5	$I_{OUT}=-2mA$	4.0			4.0			V
$V_{OUT(0)}$, Logical "0" Output Voltage	5	I_{OUT}=2mA			0.4			0.4	V
I_{OUT}, Three-State Output Current	5	V_{OUT}=0V	−1			−1			µA
		$V_{OUT}=V_{CC}$			1			1	µA
I_{CC}, Supply Current	5			1.5	3		1.5	3	mA

ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	NOTES	CONDITIONS	MIN	TYP (NOTE 4)	MAX	UNITS
AC and Dynamic Performance Characteristics (Note 10)							
t_{ACQ}	Sample and Hold Acquisition				4		$1/f_{CLK}$
f_{CLK}	Clock Frequency	5		100		10240	kHz
t_C	Conversion Time	5			67	67+250ns	$1/f_{CLK}$
SNR	Signal to Noise Ratio		V_{IN}=51kHz, 5V Sine. f_{CLK}=10.24MHz ($f_{SAMPLING} \cong$ 150kHz). Noise is Sum of All Nonfundamental Components up to 1/2 of $f_{SAMPLING}$		47		dB
THD	Total Harmonic Distortion		V_{IN}=51kHz, 5V Sine. f_{CLK}=10.24MHz ($f_{SAMPLING} \cong$ 150kHz). THD is Sum of 2, 3, 4, 5 Harmonics Relative to Fundamental		−60		dB
IMD	Intermodulation Distortion		$V_{IN}=f_A+f_B$. f_A=49kHz, 2.5V Sine. f_B=47.8kHz, 2.5V Sine, f_{CLK}=10.24MHz ($f_{SAMPLING} \cong$ 150kHz). IMD is (f_A+f_B), (f_A-f_B), $(2f_A+f_B)$, $(2f_A-f_B)$, (f_A+2f_B), (f_A-2f_B) Relative to Fundamental		−60		dB
FR	Frequency Response		V_{IN}=0 to 50kHz. 5V Sine Relative to 1kHz		0.1		dB
t_{DC}	Clock Duty Cycle	6,11		40		60	%
t_{EOC}	End of Conversion Delay	5			8	8+250ns	$1/f_{CLK}$
t_{WS}	Start Pulse Width	5		50			ns
t_{SS}	Start Pulse Setup Time	6, 12	Synchronous Only	40			ns
t_{WALE}	Address Latch Enable Pulse Width	5		50			ns
t_S	Address Setup	5		0			ns
t_H	Address Hold	5		50			ns
$t_{H1, H0}$	Output Enable for DB0–DB7	6	Figure 1, C_L=50pF			100	ns
		6	Figure 1, C_L=10pF			50	ns
$t_{1H, 0H}$	Output Disable for DB0–DB7	6	Figure 1, C_L=50pF			200	ns
		6	Figure 1, C_L=10pF			100	ns
C_{IN}	Capacitance of Logic Input				5		pF
C_{OUT}	Capacitance of Logic Outputs				10		pF

Note 1: Absolute maximum ratings are limits beyond which the life of the integrated circuit may be impaired. All voltages unless otherwise specified are measured with respect to ground.
Note 2: When the input voltage (V_{IN}) at any pin exceeds the power supply rails ($V_{IN} < V^-$ or $V_{IN} > V^+$) the absolute value of current at that pin should be limited to 25mA or less.
Note 3: −55°C to +125°C operating temperature range devices are 100% tested at temperature extremes with worst-case test conditions. −40°C to +85°C operating temperature range devices are 100% tested with temperature limits guaranteed by 100% testing, sampling, or by correlation with worst-case test conditions.
Note 4: Typicals are parametric norm at 25°C.
Note 5: Parameter guaranteed and 100% production tested.
Note 6: Parameter guaranteed. Parameters not 100% tested are not in outgoing quality level calculation.
Note 7: Total unadjusted error includes offset, full scale, linearity, multiplexer and sample and hold errors.
Note 8: For $-V_{REF} \geq V_{IN}(+)$ the digital output code will be 0000 0000. Two on-chip diodes are tied to each analog input which will forward conduct for analog input voltages one diode drop below ground or one diode drop greater than the V_{CC} supply. Be careful, during testing at low V_{CC} levels (4.5V), as high level analog inputs (5V) can cause this input diode to conduct—especially at elevated temperatures, and cause errors for analog inputs near full scale. The spec allows 100mV forward bias of either diode. This means that as long as the analog V_{IN} or V_{REF} does not exceed the supply voltage by more than 100mV, the output code will be correct. To achieve an absolute $0V_{DC}$ to $5V_{DC}$ input voltage range will therefore require a minimum supply voltage of $4.900V_{DC}$ over temperature variations, initial tolerance and loading.
Note 9: Leakage current is measured with the clock not switching.
Note 10: C_L=50pF, timing measured at 50% point.
Note 11: A 40% to 60% clock duty cycle range insures proper operation at all clock frequencies. In the case that an available clock has a duty cycle outside of these limits, the minimum time the clock is high or the minimum time the clock is low must be at least 40ns. The maximum time the clock can be high or low is 60μs.
Note 12: The conversion start setup time requirement only needs to be satisfied if a conversion must be synchronized to a given clock rising edge. If the setup time is not met, start conversion will have an uncertainty of one clock pulse.

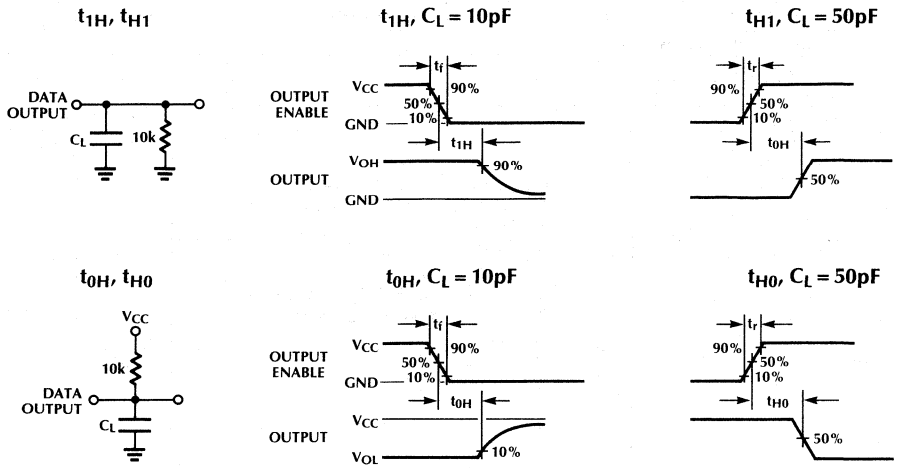


Figure 1. High Impedance Test Circuits and Waveforms

TYPICAL PERFORMANCE CURVES

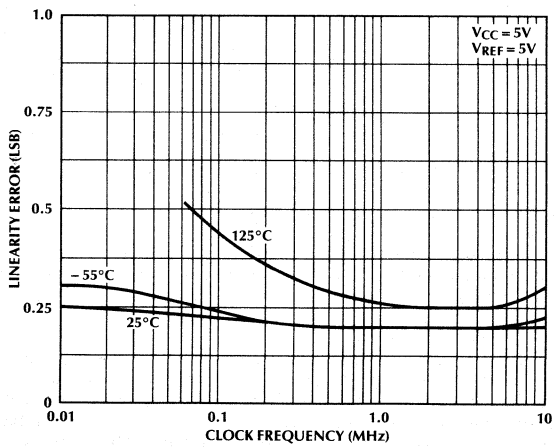


Figure 2. Linearity Error vs f_{CLK}

TYPICAL PERFORMANCE CURVES (Continued)

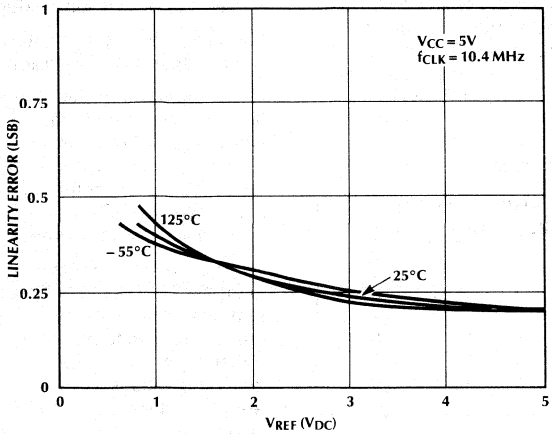


Figure 3. Linearity Error vs V_{REF} Voltage

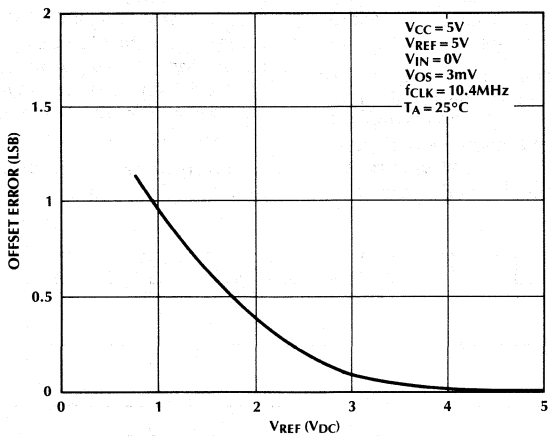


Figure 4. Unadjusted Offset Error vs V_{REF} Voltage

1.0 FUNCTIONAL DESCRIPTION

1.1 MULTIPLEXER ADDRESSING

The ML2258 contains an 8-channel single ended analog multiplexer. A particular input channel is selected by using the address decoder. The relationship between the address inputs, ADDR0–ADDR2, and the analog input selected is shown in Table 1. The address inputs are latched into the decoder on the rising edge of the address latch signal ALE.

Table 1. Multiplexer Address Decoding

SELECTED ANALOG CHANNEL	ADDRESS INPUT ADDR2	ADDR1	ADDR0
IN0	0	0	0
IN1	0	0	1
IN2	0	1	0
IN3	0	1	1
IN4	1	0	0
IN5	1	0	1
IN6	1	1	0
IN7	1	1	1

1.2 A/D CONVERTER

The A/D converter uses successive approximation to perform the conversion. The converter is composed of the successive approximation register, the DAC and the comparator.

The DAC generates the precise levels that determine the linearity and accuracy of the conversion. The DAC is composed of a capacitor upper array and a resistor lower array. The capacitor upper array generates the 4 MSB decision levels while the series resistor lower array generates the 4 LSB decision levels. A switch decoder tree is used to decode the proper level from both arrays.

The capacitor/resistor array offers fast conversion, superior linearity and accuracy since matching is only required between $2^4 = 16$ elements (as opposed to $2^8 = 256$ elements in conventional designs). And since the levels are based on the ratio of capacitors to capacitors and resistors to resistors, the accuracy and long term stability of the converter is improved. This also guarantees monotonicity and no missing codes, as well as eliminating any linearity temperature or power supply dependence.

The successive approximation register is a digital block used to store the bit decisions from the conversion.

The comparator design is unique in that it is fully differential and auto zeroed. The fully differential architecture provides excellent noise immunity, excellent power supply rejection, and wide common mode range. The comparator is auto zeroed at the start of each conversion in order to remove any DC offset and full scale gain error, thus improving accuracy and linearity.

Another advantage of the capacitor array approach used in the ML2258 over conventional designs is the inherent sample and hold function. This true S/H allows an accurate conversion to be done on the input even if the analog signal is not stable. Linearity and accuracy are maintained for analog signals up to 1/2 the sampling frequency. As a result, input signals up to 75kHz can be converted without degradation in linearity or accuracy.

The sequence of events during a conversion is shown in Figure 5. The rising edge of a START pulse resets the internal registers and the falling edge initiates a conversion on the next rising edge of CLK. Four CLK pulses later, sampling of the analog input begins. The input is then sampled for the next four CLK periods until EOC goes low. EOC goes low on the rising edge of the 8th CLK pulse indicating that the conversion is now beginning. The actual conversion now takes place for the next 56 CLK pulses, one bit for each 7 CLK pulses. After the conversion is done, the data is updated on DB0–DB7 and EOC goes high on the rising edge of the 67th CLK pulse, indicating that the conversion has been completed and data is valid on DB0–DB7. The data will stay valid on DB0–DB7 until the next conversion updates the data word on the next rising edge of EOC.

A conversion can be interrupted and restarted at any time by a new START pulse.

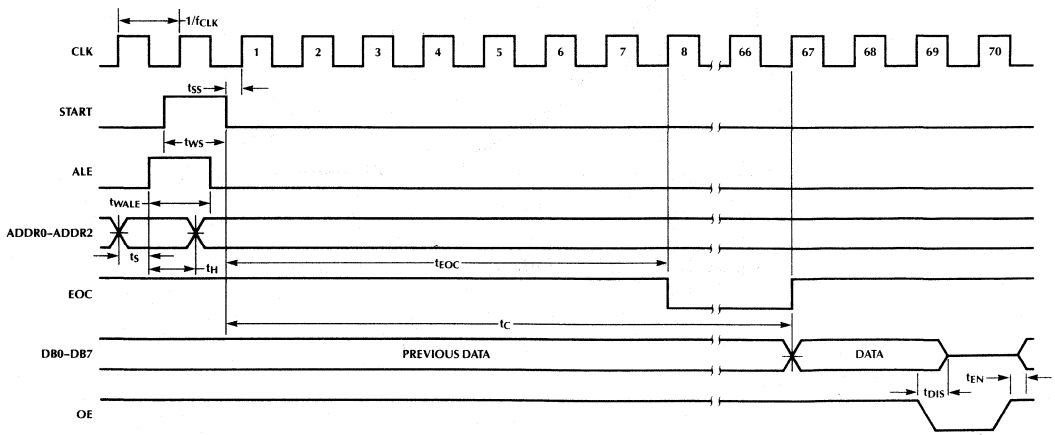


Figure 5. Timing Diagram

1.0 FUNCTIONAL DESCRIPTION (Continued)

1.3 ANALOG INPUTS AND SAMPLE/HOLD

The ML2258 has a true sample and hold circuit which samples both the selected input and ground simultaneously. This simultaneous sampling with a true S/H will give common mode rejection and AC linearity performance that is superior to devices where the two input terminals are not sampled at the same instant and where true sample and hold capability does not exist. Thus, the ML2258 can reject AC common mode signals from DC–50kHz as well as maintain linearity for signals from DC–50kHz.

The plot below (Figure 6) shows a 2048 point FFT of the ML2258 converting a 50kHz, 0 to 5V, low distortion sine wave input. The ML2258 samples and digitizes, at its specified accuracy, dynamic input signals with frequency components up to the Nyquist frequency (one-half the sampling rate). The output spectra yields precise measurements of input signal level, harmonic components, and signal to noise ratio up to the 8-bit level. The near ideal signal to noise ratio is maintained independent of increasing analog input frequencies to 50kHz.

The signal at the analog input is sampled during the interval when the sampling switch is open prior to conversion start. The sampling window (S/H acquisition time) is 4 CLK periods long and occurs 4 CLK periods after START goes low. When the sampling switch closes at the start of the S/H acquisition time, 8pF of capacitance is thrown onto the analog input. 4 CLK periods later, the sampling switch opens, the signal present at analog input is stored and conversion starts. Since any error on the analog input at the end of the S/H acquisition time will cause additional conversion error, care should be taken to insure adequate settling and charging time from the source. If more charging or settling time is needed to reduce these analog input errors, a longer CLK period can be used.

The ML2258 has improved latchup immunity. Each analog input has dual diodes to the supply rails, and a minimum of ±25mA (±100mA typically) can be injected into each analog input without causing latchup.

1.4 REFERENCE

The voltage applied to the $+V_{REF}$ and $-V_{REF}$ inputs defines the voltage span of the analog input (the difference between V_{INMAX} and V_{INMIN}) over which the 256 possible output codes apply. The devices can be used in either ratiometric applications or in systems requiring absolute accuracy. The reference pins must be connected to a voltage source capable of driving the reference input resistance, typically 20k.

In a ratiometric system, the analog input voltage is proportional to the voltage used for the A/D reference. This voltage is typically the system power supply, so the $+V_{REF}$ pin can be tied to V_{CC} and $-V_{REF}$ tied to GND. This technique relaxes the stability requirements of the system reference as the analog input and A/D reference move together maintaining the same output code for a given input condition.

For absolute accuracy, where the analog input varies between specific voltage limits, the reference pins can be biased with a time and temperature stable voltage source.

In contrast to the ADC0808 and ADC0809, the ML2258 $-V_{REF}$ and $+V_{REF}$ reference values do not have to be symmetric around one half of the supply. $+V_{REF}$ and $-V_{REF}$ can be at any voltage between V_{CC} and GND. In addition, the difference between $+V_{REF}$ and $-V_{REF}$ can be set to small values for conversions over smaller voltage ranges. Particular care must be taken with regard to noise pickup, circuit layout and system error voltage sources when operating with a reduced span due to the increased sensitivity of the converter.

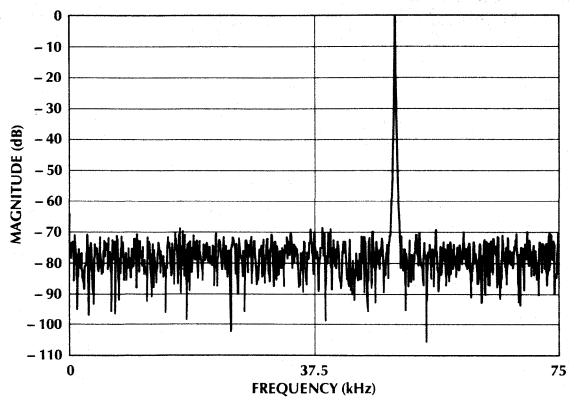


Figure 6. Output Spectrum

1.0 FUNCTIONAL DESCRIPTION (Continued)

1.5 POWER SUPPLY AND REFERENCE DECOUPLING

A 10μF electrolytic capacitor is recommended to bypass V_{CC} to GND, using as short a lead length as possible. In addition, with clock frequencies above 1MHz, a 0.1μF ceramic disc capacitor should be used to bypass V_{CC} to GND.

If REF+ and REF− inputs are driven by long lines, they should be bypassed by 0.1μF ceramic disc capacitors at the reference input pins (pins 12, 16).

1.6 DYNAMIC PERFORMANCE

Signal-to-Noise Ratio

Signal-to-noise ratio (SNR) is the measured signal to noise at the output of the converter. The signal is the rms magnitude of the fundamental. Noise is the rms sum of all the nonfundamental signals up to half the sampling frequency. SNR is dependent on the number of quantization levels used in the digitization process; the more levels, the smaller the quantization noise. The theoretical SNR for a sine wave is given by

$$SNR = (6.02N + 1.76)dB$$

where N is the number of bits. Thus for ideal 8-bit converter, SNR = 49.92dB.

Harmonic Distortion

Harmonic distortion is the ratio of the rms sum of harmonics to the fundamental. Total harmonic distortion (THD) of the ML2258 is defined as

$$20 \log \frac{(V_2^2 + V_3^2 + V_4^2 + V_5^2)^{1/2}}{V_1}$$

where V_1 is the rms amplitude of the fundamental and V_2, V_3, V_4, V_5 are the rms amplitudes of the individual harmonics.

Intermodulation Distortion

With inputs consisting of sine waves at two frequencies, f_A and f_B, any active device with nonlinearities will create distortion products, of order (m + n), at sum and difference frequencies of $mf_A + nf_B$, where m,n = 0, 1, 2, 3,... . Intermodulation terms are those for which m or n is not equal to zero. The ML2258 (IMD) intermodulation distortion specification includes the second order terms ($f_A + f_B$) and ($f_A - f_B$) and the third order terms ($2f_A + f_B$), ($2f_A - f_B$), ($f_A + 2f_B$) and ($f_A - 2f_B$) only.

1.7 DIGITAL INTERFACE

The analog inputs are selected by the digital addresses, ADDR0–ADDR2, and latched on the rising edge of ALE. This is described in the Multiplexer Addressing section.

A conversion is initiated by the rising edge of a START pulse. As long as this pulse is high, the internal logic is reset.

The sampling interval starts with the 4th CLK rising edge after a START falling edge and ends on the 8th rising edge of CLK, 4 CLK periods later. On the rising edge of the 8th CLK pulse, the conversion starts and EOC goes low.

Each bit conversion in the successive approximation process takes 7 CLK periods. On the rising edge of the 64 CLK pulse, the digital output of the conversion is updated on the outputs DB0–DB7. On the rising edge of the 65th CLK pulse, EOC goes high indicating the conversion is done and data on DB0–DB7 is valid.

One feature of the ML2258 over conventional devices is that the data is double buffered. This means that the outputs DB0–DB7 will stay valid until updated at the end of the next conversion and will not become invalid when the next conversion starts. This facilitates interfacing with external logic of μP.

The signal OE drives the data bus, DB0–DB7, into the high impedance state when held low. This allows the ML2258 to be tied directly to a μP system bus without any latches or buffers.

2.0 TYPICAL APPLICATIONS

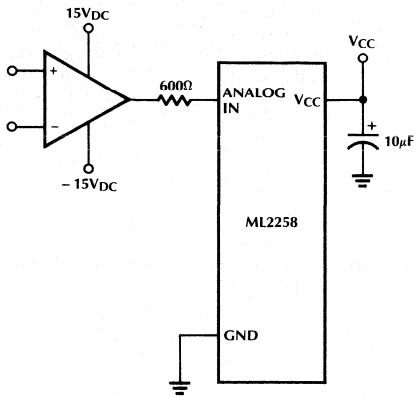


Figure 7. Protecting the Input

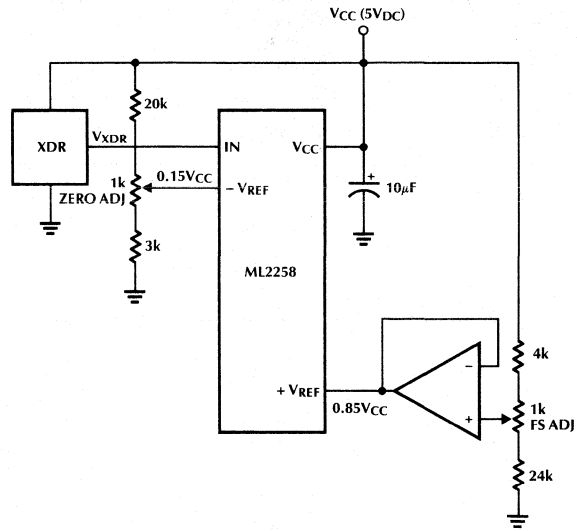


Figure 8. Operating with Ratiometric Transducers 15% of $V_{CC} \leq V_{XDR} \leq 85\%$ of V_{CC}

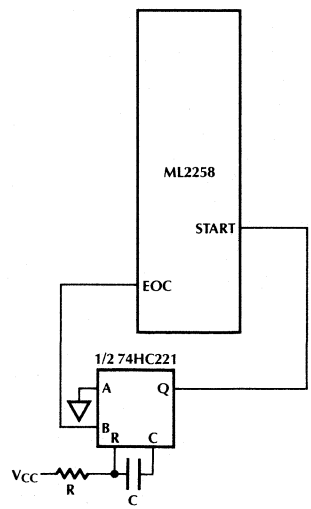


Figure 9. Continuous Conversion Mode

ORDERING INFORMATION

PART NUMBER	ALTERNATE PART NUMBER	TOTAL UNADJUSTED ERROR	TEMPERATURE RANGE	PACKAGE
ML2258BMJ	ADC0808CJ	±1/2LSB	−55°C to +125°C	Hermetic DIP
ML2258BIJ	ADC0808CCJ		−40°C to +85°C	Hermetic DIP
ML2258BIP	ADC0808CCN		−40°C to +85°C	Molded DIP
ML2258BIQ	ADC0808CCV		−40°C to +85°C	Molded (PCC)
ML2258CIJ		±1LSB	−40°C to +85°C	Hermetic DIP
ML2258CIP	ADC0809CCN		−40°C to +85°C	Molded DIP
ML2258CIQ	ADC0809CCV		−40°C to +85°C	Molded (PCC)

Micro Linear

ML2261

μP Compatible High-Speed 8-Bit A/D Converter with T/H (S/H)

GENERAL DESCRIPTION

The ML2261 is a high-speed, μP compatible 8-bit A/D converter with a conversion time of 670ns over the operating temperature range and supply voltage tolerance. The ML2261 operates from a single 5V supply and has an analog input range from GND to V_{CC}.

The ML2261 has two different pin selectable modes. The T/H mode has an internal track and hold. The S/H mode has a true internal sample and hold and can digitize 0 to 5V sinusoidal signals as high as 500kHz. Timing is compatible with the AD7821.

The ML2261 digital interface has been designed so that the device appears as a memory location or I/O port to a μP.

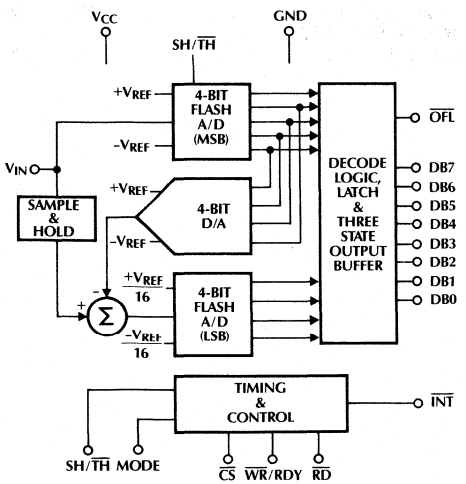
The ML2261 is an enhanced, pin compatible second source for the industry standard ADC0820 and AD7820. The ML2261 enhancements are faster conversion time, parameters guaranteed over the supply tolerance and temperature range, improved digital interface timing, superior power supply rejection, and better latchup immunity on analog inputs.

FEATURES

- Conversion time, WR-RD mode over temperature and supply voltage tolerance
  - Track & Hold Mode ..... 800ns max
  - Sample & Hold Mode ..... 670ns max
- Total unadjusted error ..... ±1/2 LSB or ±1 LSB
- Digitizes a 5V, 250kHz sine wave to 8-bit accuracy
- No missing codes
- 0V to 5V analog input range with single 5V power supply
- No zero or full scale adjust required
- Analog input protection ..... 25mA min
- Operates ratiometrically or with up to 5V voltage reference
- No external clock required
- Easy interface to μP, or operates stand alone
- Power-on reset circuitry
- Low power 75mW
- Standard 20-pin DIP or surface mount PCC
- Superior pin compatible replacement for ADC0820 and AD7820

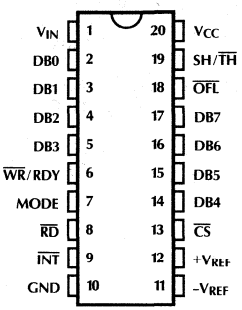
2

BLOCK DIAGRAM



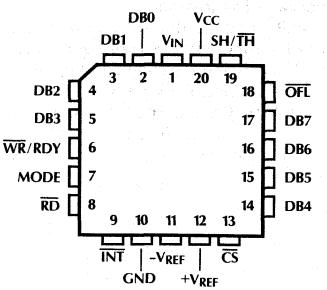
PIN CONNECTIONS

20-Pin DIP



TOP VIEW

20-Pin PCC



TOP VIEW

PIN DESCRIPTION

PIN NO.	NAME	FUNCTION
1	V_{IN}	Analog input.
2	DB0	Data output — bit 0 (LSB).
3	DB1	Data output — bit 1.
4	DB2	Data output — bit 2.
5	DB3	Data output — bit 3.
6	$\overline{WR}$/RDY	Write input or ready output. In WR-RD mode, this pin is $\overline{WR}$ input. In RD mode, this pin is RDY open drain output. See Digital Interface section.
7	MODE	Mode select input. MODE = GND: RD mode MODE = V_{CC}: WR-RD mode Pin has internal current source pulldown to GND.
8	$\overline{RD}$	Read input. In RD mode, this pin initiates a conversion. In WR-RD mode, this pin latches data into output latches. See Digital Interface section.
9	$\overline{INT}$	Interrupt output. This output signals the end of a conversion and indicates that data is valid on the data outputs. See Digital Interface section.
10	GND	Ground.
11	$-V_{REF}$	Negative reference voltage for A/D converter.
12	$+V_{REF}$	Positive reference voltage for A/D converter.
13	$\overline{CS}$	Chip select input. This pin must be held low for the device to perform a conversion.
14	DB4	Data output — bit 4.
15	DB5	Data output — bit 5.
16	DB6	Data output — bit 6.
17	DB7	Data output — bit 7 (MSB).
18	$\overline{OFL}$	Overflow output. This output goes low at end of conversion if V_{IN} is greater than $+V_{REF}$ – ½LSB.
19	SH/$\overline{TH}$	S/H, T/H mode select. When SH/$\overline{TH}$ = V_{CC}, the device is in sample and hold mode. When SH/$\overline{TH}$ = GND, the device is in track and hold mode. Pin has internal pulldown current source to GND.
20	V_{CC}	Positive supply. +5 volts ± 5%.

ABSOLUTE MAXIMUM RATINGS
(Note 1)

Supply Voltage, V_{CC} 6.5V
Voltage
- Logic Inputs ..... –0.3V to V_{CC} + 0.3V
- Analog Inputs ..... –0.3V to V_{CC} + 0.3V

Input Current per Pin (Note 2) ..... ±25mA
Storage Temperature ..... –65°C to +150°C
Package Dissipation
- at T_A = 25°C (Board Mount) 875mW

Lead Temperature (Soldering 10 sec.)
- Dual-In-Line Package (Plastic) ..... 260°C
- Dual-In-Line Package (Ceramic) ..... 300°C
- Molded Chip Carrier Package
  - Vapor Phase (60 sec.) ..... 215°C
  - Infrared (15 sec.) ..... 220°C

OPERATING CONDITIONS

Supply Voltage, V_{CC} ..... $4.5V_{DC}$ to $6.0V_{DC}$
Temperature Range (Note 3) ..... $T_{MIN} \leq T_A \leq T_{MAX}$
- ML2261BMJ, ML2261CMJ ..... –55°C to +125°C
- ML2261BIJ, ML2261CIJ ..... –40°C to +85°C
- ML2261BCQ, ML2261CCQ
- ML2261BCP, ML2261CCP ..... 0°C to +70°C

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, $T_A = T_{MIN}$ to T_{MAX}, $V_{CC} = +V_{REF} = 5V \pm 5\%$, and $-V_{REF} = GND$

PARAMETER	NOTES	CONDITIONS	ML2261XCX MIN	ML2261XCX TYP (Note 4)	ML2261XCX MAX	ML2261XIX, ML2261XMX MIN	ML2261XIX, ML2261XMX TYP (Note 4)	ML2261XIX, ML2261XMX MAX	UNITS
Converter									
Total Unadjusted Error ML2261BXX ML2261CXX	5, 7	$V_{REF} = V_{CC}$			 ±1/2 ±1			 ±1/2 ±1	 LSB LSB
$+V_{REF}$ Voltage Range	6		$-V_{REF}$		$V_{CC}+0.1$	$-V_{REF}$		$V_{CC}+0.1$	V
$-V_{REF}$ Voltage Range	6		GND–0.1		$+V_{REF}$	GND–0.1		$+V_{REF}$	V
Reference Input Resistance	5		1	2	3	1	2	3	kΩ
Analog Input Range	5, 8		GND–0.1		$V_{CC}+0.1$	GND–0.1		$V_{CC}+0.1$	V
Power Supply Sensitivity	5	DC V_{CC} = 5V ± 5%, V_{REF} = 4.75V		±1/32	±1/4		±1/32	±1/4	LSB
		100mVp-p 100kHz sine on V_{CC} V_{IN} = 0		±1/16			±1/16		LSB
Analog Input Leakage Current	5, 9	Converter Idle	–1		+1	–1		+1	μA
Analog Input Capacitance		During Acquisition Period		45			45		pF
Digital and DC									
$V_{IN(1)}$, Logical "1" Input Voltage	5	$\overline{WR}$, $\overline{RD}$, $\overline{CS}$	2.0			2.0			V
		MODE, SH/$\overline{TH}$	V_{CC}–0.5			V_{CC}–0.5			V
$V_{IN(0)}$, Logical "0" Input Voltage	5	$\overline{WR}$, $\overline{RD}$, $\overline{CS}$			0.8			0.8	V
		MODE, SH/$\overline{TH}$			0.5			0.5	V
$I_{IN(1)}$, Logical "1" Input Current	5	$V_{IH} = V_{CC}$; $\overline{WR}$, $\overline{RD}$, $\overline{CS}$			1			1	μA
		$V_{IH} = V_{CC}$; MODE, SH/$\overline{TH}$	15	50	150	15	50	150	μA
$I_{IN(0)}$, Logical "0" Input Current	5	V_{IL} = GND; $\overline{WR}$, $\overline{RD}$, $\overline{CS}$	–1			–1			μA
		V_{IL} = GND; MODE, SH/$\overline{TH}$	–20			–20			μA
$V_{OUT(1)}$, Logical "1" Output Voltage	5	I_{OUT} = –2mA	4.0			4.0			V
$V_{OUT(0)}$, Logical "0" Output Voltage	5	I_{OUT} = 2mA			0.4			0.4	V
I_{OUT}, Three-State Output Current	5	V_{OUT} = 0V	–1			–1			μA
		$V_{OUT} = V_{CC}$			1			1	μA
C_{OUT}, Logic Output Capacitance				5			5		pF
C_{IN}, Logic Input Capacitance				5			5		pF
I_{CC}, Supply Current	5	$\overline{CS} = \overline{WR} = \overline{RD}$ = "1" No Output Load		10	16		10	17.5	mA

2

ELECTRICAL CHARACTERISTICS (Continued)

Unless otherwise specified, $T_A = T_{MIN}$ to T_{MAX}, $V_{CC} = +V_{REF} = 5V \pm 5\%$, $-V_{REF}$ = GND, and timing measured at 1.4V, C_L = 100pF.

PARAMETER	NOTES	CONDITIONS	ML2261XCX MIN	ML2261XCX TYP (Note 4)	ML2261XCX MAX	ML2261XIX, ML2261XMX MIN	ML2261XIX, ML2261XMX TYP (Note 4)	ML2261XIX, ML2261XMX MAX	UNITS
AC and Dynamic Performance (Note 9)									
t_{CRD}, Conversion Time, Read Mode	5	$\overline{RD}$ to $\overline{INT}$, MODE = 0V			1020			1100	ns
t_{CWR-RD}, Conversion Time, Write-Read Mode	5, 9	$\overline{WR}$ Falling Edge to $\overline{INT}$, $t_{RD} < t_{INT}$, MODE = V_{CC}; SH/$\overline{TH}$=V_{CC}			670			725	ns
		$\overline{WR}$ Falling Edge to $\overline{INT}$, $t_{RD} < t_{INT}$, MODE = V_{CC}; SH/$\overline{TH}$=GND			800			880	ns
SNR, Signal to Noise Ratio		V_{IN} = 5V, 250kHz Noise is sum of all nonfundamental components from 0–500kHz. SH/$\overline{TH}$ = V_{CC}, MODE = V_{CC} $f_{SAMPLING}$ = 1 MHz		48			48		dB
HD, Harmonic Distortion		V_{IN} = 5V, 250kHz THD is sum of 2–5th harmonics relative to fundamental. SH/$\overline{TH}$ = V_{CC}, MODE = V_{CC} $f_{SAMPLING}$ = 1 MHz		–63			–63		dB
IMD, Intermodulation Distortion		fa = 2.5V, 250kHz fb = 2.5V, 248kHz IMB is (fa + fb), (fa – fb), (2fa + fb), (2fa – fb), (fa + 2fb), or (fa – 2fb) relative to fundamental. SH/$\overline{TH}$ = V_{CC}, MODE = V_{CC} $f_{SAMPLING}$ = 1 MHz		–60			–60		dB
FR, Frequency Response		V_{IN} = 5V, 0–250kHz Relative to 1kHz SH/$\overline{TH}$ = V_{CC}, MODE = V_{CC} $f_{SAMPLING}$ = 1 MHz		±0.1			±0.1		dB
SR, Slew Rate Tracking	6	SH/$\overline{TH}$ = V_{CC}			4.0			4.0	V/μs
		SH/$\overline{TH}$ = GND			.25			.25	V/μs
AC Performance Read Mode (Pin 7 = 0V), Figure 2									
t_{RDY}, $\overline{CS}$ to RDY Delay	5		0		50	0		55	ns
t_{RDD}, $\overline{RD}$ Low to RDY Delay	5, 10	Figure 1			1020			1100	ns
t_{CSS}, $\overline{CS}$ to $\overline{RD}$, $\overline{WR}$ Setup Time	5		0			0			ns
t_{CSH}, $\overline{CS}$ to $\overline{RD}$, $\overline{WR}$ Hold Time	5		0			0			ns
t_{CRD}, Conversion Time — $\overline{RD}$ Low to $\overline{INT}$ Low	5, 10				1020			1100	ns

ELECTRICAL CHARACTERISTICS (Continued)

Unless otherwise specified, $T_A = T_{MIN}$ to T_{MAX}, $V_{CC} = +V_{REF} = 5V \pm 5\%$, $-V_{REF}$ = GND, and timing measured at 1.4V, C_L = 100pF

PARAMETER	NOTES	CONDITIONS	ML2261XCX			ML2261XIX, ML2261XMX			UNITS
			MIN	TYP (Note 4)	MAX	MIN	TYP (Note 4)	MAX	
AC Performance Read Mode (Pin 7 = 0V), Figure 2 (Continued)									
t_{ACC0}, Data Access Time RD to Data Valid	5		t_{CRD}		t_{CRD}+30	t_{CRD}		t_{CRD}+30	ns
t_{RDPW}, $\overline{RD}$ Pulse Width	5		t_{CRD}+30			t_{CRD}+30			ns
t_{INTH}, $\overline{RD}$ to $\overline{INT}$ Delay	5, 10		0		60	0		70	ns
t_{DH}, Data Hold Time — $\overline{RD}$ Rising Edge to Data High Impedance State	6, 10	Figure 1	0		50	0		60	ns
t_P, Delay Time Between Conversions — $\overline{INT}$ Low to $\overline{RD}$ Low	5, 10	Sample & Hold Mode, SH/$\overline{TH}$ = V_{CC}	300			325			ns
		Track & Hold Mode, SH/$\overline{TH}$ = GND	240			260			ns
AC Performance Write-Read Mode (Pin 7 = 5V), Figures 3 and 4									
t_{CSS}, $\overline{CS}$ to $\overline{RD}$, $\overline{WR}$ Setup Time	5		0			0			ns
t_{CSH}, $\overline{CS}$ to $\overline{RD}$, $\overline{WR}$ Hold Time	5		0			0			ns
t_{WR}, $\overline{WR}$ Pulse Width	5	SH/$\overline{TH}$ = V_{CC}	180		50K	195		50K	ns
	6	SH/$\overline{TH}$ = GND	320		50K	360		50K	ns
t_{RD}, Read Time — $\overline{WR}$ High to $\overline{RD}$ Low Delay	5	$t_{RD} < t_{INTL}$	275			300			ns
t_{RI}, $\overline{RD}$ to $\overline{INT}$ Delay	5, 10	$t_{RD} < t_{INTL}$	0		215	0		230	ns
t_{ACC1}, Data Access Time — $\overline{RD}$ Low to Data Valid	5	$t_{RD} < t_{INTL}$	0		220	0		240	ns
t_{CWR-RD}, Conversion Time — $\overline{WR}$ Falling Edge to $\overline{INT}$ Low	5,9,10	$t_{RD} < t_{INTL}$, SH/$\overline{TH}$ = V_{CC}			670			725	ns
	6,9,10	$t_{RD} < t_{INTL}$, SH/$\overline{TH}$ = GND			800			880	ns
t_{INTL}, Internal Comparison Time — $\overline{WR}$ Rising Edge to $\overline{INT}$ Low	5, 10	$t_{RD} > t_{INTL}$			620			670	ns
t_{ACC2}, Data Access Time — $\overline{RD}$ to Data Valid	5	$t_{RD} > t_{INTL}$	0		50	0		60	ns
t_{DH}, Data Hold Time — $\overline{RD}$ Rising Edge to Data High Impedance State	6, 10	Figure 1	0		50	0		60	ns
t_{INTH}, $\overline{RD}$↑ to $\overline{INT}$↑ Delay	5, 10		0		60	0		70	ns
t_P, Delay Time Between Conversions — $\overline{INT}$ Low to $\overline{WR}$ Low	5, 10	Sample & Hold Mode, SH/$\overline{TH}$ = V_{CC}	300			325			ns
		Track & Hold Mode, SH/$\overline{TH}$ = GND	240			260			ns
t_{IHWR}, $\overline{WR}$↑ to $\overline{INT}$↑ Delay	5, 10	Standalone Mode	0		90	0		100	ns
t_{ID}, $\overline{INT}$↓ to Data Valid Delay	5, 10	Standalone Mode	0		20	0		30	ns

2

Note 1: Absolute maximum ratings are limits beyond which the life of the integrated circuit may be impaired. All voltages unless otherwise specified are measured with respect to ground.

Note 2: When the voltage at any pin exceeds the power supply rails (V_{IN} < GND or V_{IN} > V_{CC}) the absolute value of current at that pin should be limited to 25mA or less.

Note 3: –55°C to +125°C operating temperature range devices are 100% tested at temperature extremes with worst-case test conditions. 0°C to +70°C and –40°C to +85°C operating temperature range devices are 100% tested with temperature limits guaranteed by 100% testing, sampling, or by correlation with worst-case test conditions.

Note 4: Typicals are parametric norm at 25°C.

Note 5: Parameter guaranteed and 100% production tested.

Note 6: Parameter guaranteed. Parameters not 100% tested are not in outgoing quality level calculation.

Note 7: Total unadjusted error includes offset, full scale, linearity, and sample and hold errors. Total unadjusted error is tested at the minimum specified times for $\overline{WR}$, $\overline{RD}$, t_{RI}, and t_P. For example, for the ML2261XCX in the sample and hold mode, $\overline{WR/RD}$ mode: t_{WR} = 180ns, t_{RD} = 275ns with a frequency of 1.031MHz (cycle time of 970ns).

Note 8: For $-V_{REF} \geq V_{IN}$ the digital output code will be 0000 0000. Two on-chip diodes are tied to the analog input which will forward conduct for analog input voltages one diode drop below ground or one diode drop greater than the V_{CC} supply. Be careful, during testing at low V_{CC} levels (4.5V), as high level analog inputs (5V) can cause this input diode to conduct — especially at elevated temperatures, and cause errors for analog inputs near full scale. The spec allows 100mV forward bias of either diode. This means that as long as the analog V_{IN} or V_{REF} does not exceed the supply voltage by more than 100mV, the output code will be correct. To achieve an absolute $0V_{DC}$ to $5V_{DC}$ input voltage range will therefore require a minimum supply voltage of $4.900V_{DC}$ over temperature variations, initial tolerance and loading.

Note 9: Conversion time, write-read mode = t_{WR} + t_{RD} + t_{RI}.

Note 10: Defined from the time an output crosses 0.8V or 2.4V.

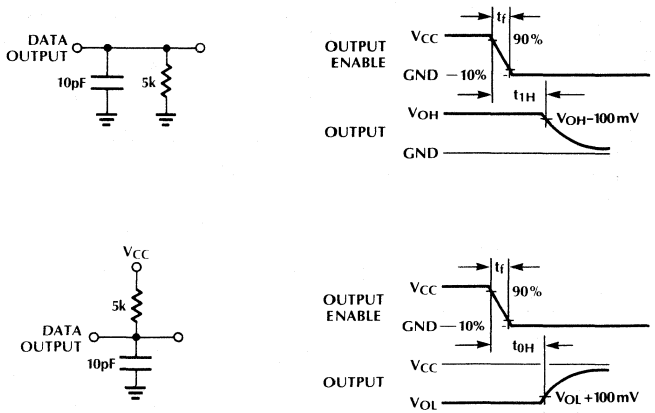
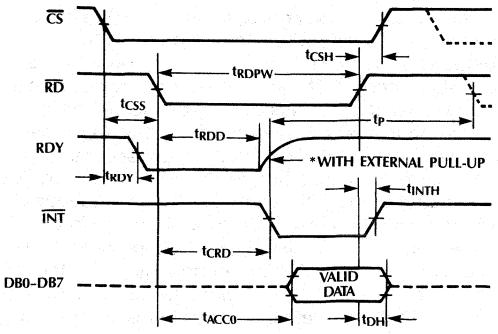


Figure 1. High Impedance Test Circuits and Waveforms



* IN SAMPLE & HOLD MODE A PULL UP RESISTOR ON RDY SHOULD NOT BE USED UNLESS CS↓ IS ≥ 20ns BEFORE RD↓.

Figure 2. RD Mode Timing

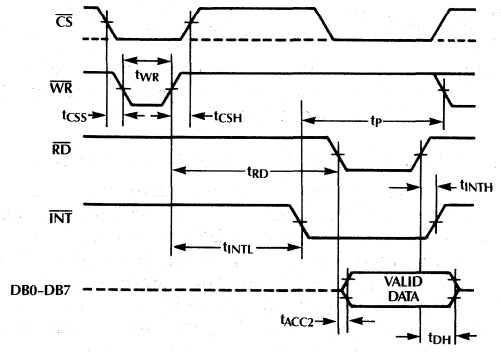


Figure 3. WR-RD Mode Timing ($t_{RD} > t_{INTL}$)

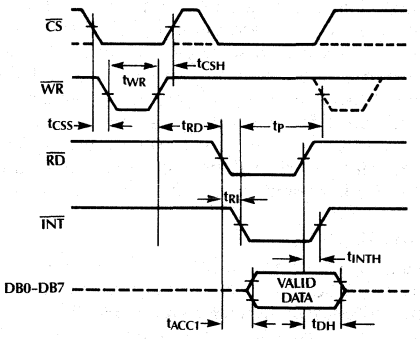


Figure 4. WR-RD Mode Timing ($t_{RD} < t_{INTL}$)

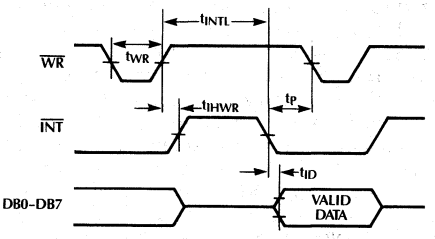


Figure 5. WR-RD Mode Stand-Alone Timing $\overline{CS}$ = $\overline{RD}$ = 0

1.0 FUNCTIONAL DESCRIPTION

The ML2261 uses a two stage flash technique for A/D conversion. This technique first performs a 4 bit flash conversion on V_{IN} to determine the 4 MSB's. These 4 MSB's are then cycled through an internal DAC to recreate the analog input. This reconstructed analog input signal from the DAC is then subtracted from the input, and the difference voltage is converted by a second 4 bit flash conversion, providing the 4 LSB's of the output data word. An additional overrange function detects if V_{IN} is greater than $+V_{REF}$ – ½LSB.

1.1 ANALOG INPUT

The analog input on the ML2261 behaves differently than inputs on conventional converters. The analog input current requirements change while the conversion is in progress, and the amount of input current depends on what cycle the converter is in.

The equivalent input circuit for the converter is shown in Figure 6. When the conversion starts in the T/H mode ($\overline{WR}$↓ in the WR-RD mode or $\overline{RD}$↓ in the RD mode) S1, S4 and S6 close and S3 opens. This period is known as the acquisition period where the MSB flash converter tracks the input signal and the LSB flash converter samples it. During this period, V_{IN} is connected to the 16 MSB and 15 LSB comparators. Thus 38 pF of input capacitance must be charged up through the combined R_{ON} resistance of the internal analog switches plus any external source resistance, R_S. In addition, there is a stray capacitance of approximately 11 pF that needs to be charged through the external source resistance R_S. This period ends in the WR-RD mode when $\overline{WR}$↑ or by an internal timer in the RD mode. At this point S1 and S4 open and the analog input at V_{IN} is no longer being sampled; thus during this time the analog voltage on V_{IN} does not affect converter performance.

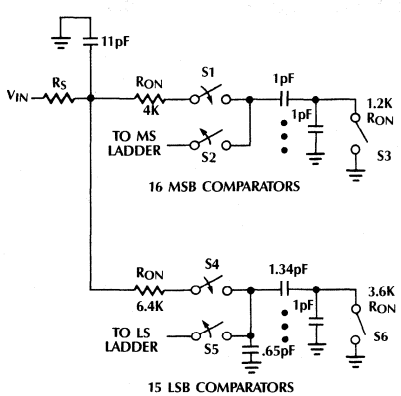


Figure 6. Converter Equivalent Input Circuit

As shown above, the critical period for charging up the analog input occurs when the MSB and LSB comparators are sampling the input, known as the acquisition period. The source of the external signal on V_{IN} must adequately charge up the analog voltage during the acquisition period. To do this, the input must settle within the required analog accuracy tolerance at least 50ns before the end of the acquisition period so that the MSB comparators have adequate time to make the correct decision. If more time is needed due to finite charging or settling time of the external source, the $\overline{WR}$ low period can be extended in WR-RD mode. In RD mode, since the acquisition time is fixed by internal delays, the burden is on the external source to charge up and settle the input adequately.

When the ML2261 operates in the S/H mode (pin 19 = V_{CC}) both the MSB and the LSB flash converter perform a true sample and hold operation during the acquisition or sampling period. This period starts after the falling edge of $\overline{INT}$ and ends with the falling edge of $\overline{WR}$ in the WR-RD mode or the falling edge of $\overline{RD}$ in the RD mode. The duration of this period is user controlled and must satisfy a minimum of t_P.

During this period S1, S3, S4 and S6 close, therefore 46 pF of input capacitance must be charged up in addition to the 11 pF of stray capacitance.

1.2 TRACK AND HOLD vs. SAMPLE AND HOLD

The MSB Flash Converter of the ML2261 in T/H mode has a track and hold mechanism for sampling the input. The input is attached to the MSB comparators directly in the MSB compare cycle, or acquisition period. When the MSB compare cycle ends, the state of the MSB comparators is latched. The LSB Flash Converter always performs a S/H operation. Thus, the analog input signal can be changing during the MSB compare cycle, or acquisition period, and the MSB comparators will be tracking it as long as the slew rate of the analog input is slow enough so that the MSB comparators can respond. The ML2261 can track and hold signals with slew rates as high as .25V/μs (16kHz @ 5 volts) without sacrificing conversion accuracy.

The ML2261 in S/H mode does not have the slew rate limitation of the T/H mode since an internal sample and hold acquires the analog signal, holds it internally, and then performs a conversion. Since this is a true sample and hold function, the S/H mode can theoretically digitize signals of frequencies much higher than the T/H mode. The ML2261 in S/H mode can digitize signals of frequencies as high as 250kHz @ 5V (slew rates as high as 4V/μs) without sacrificing conversion accuracy. In most applications, the S/H mode is more desirable than T/H mode because of the better dynamic performance.

1.2.1 CONVERTER — T/H MODE

The operating sequence for the WR-RD mode is illustrated in Figure 7a. Initially, the internal comparators are auto-zeroed while $\overline{WR}$ is high. A conversion is initiated by the falling edge of $\overline{WR}$. While $\overline{WR}$ is low, the MSB comparators are tracking the analog input and comparing this voltage against voltages from the internal resistor ladder. At the same time, the input is being acquired or sampled by LSB comparators. On the rising edge of $\overline{WR}$, the MSB comparator results are latched, and the LSB acquisition time is ended by closing the sampling switch to the LSB comparators. While $\overline{WR}$ is high, the LSB comparators then compare the residual input voltage against internal voltages from the resistor ladder to determine the 4 LSB's. When the LSB comparison or conversion is complete, $\overline{INT}$ goes low and latches the conversion result into the output latches. Then, the comparators are auto-zeroed while $\overline{WR}$ is high before another conversion can start.

The operating sequence for RD mode, is similar to that described above for the WR-RD mode, except the conversion is initiated by the falling edge of $\overline{RD}$, and the MSB and LSB conversions are generated by internal clock edges that are generated while $\overline{RD}$ is low.

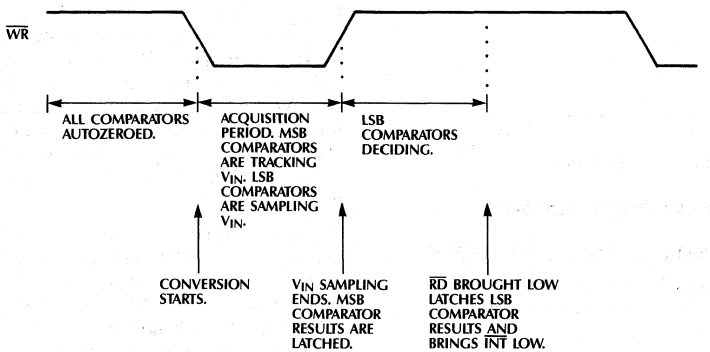
1.2.2 CONVERTER — S/H MODE

The operating sequence for S/H mode is illustrated in Figure 7b. Notice that it is similar to T/H mode described above except this mode has a true sample and hold function. The falling edge of $\overline{INT}$ closes the sampling switch and starts the acquisition period where the analog input is sampled at the same time all comparators are auto-zeroed. The falling edge of $\overline{WR}$ opens the internal sampling switch, ends the acquisition period, and starts the conversion on the internally sample and held signal. The MSB comparators make their decisions while $\overline{WR}$ is low. On the rising edge of $\overline{WR}$, the MSB comparator results are latched. The LSB comparators make their decision when $\overline{WR}$ is high. When the LSB comparison or conversion is complete, $\overline{INT}$ goes low and latches the conversion result into the output buffers. Then, the acquisition period begins again and the converter is ready for the next conversion.

The operating sequence for the RD mode is the same as the WR-RD mode, except the conversion is initiated by the falling edge of $\overline{RD}$, and the MSB and LSB conversions are generated by internal clock edges that are generated while $\overline{RD}$ is low.

2

a). T/H Mode



b). S/H Mode

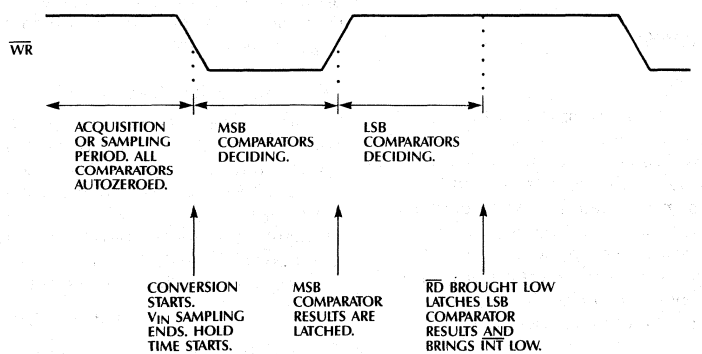


Figure 7. Operating Sequence (WR-RD Mode)

1.3 REFERENCE

The $+V_{REF}$ and $-V_{REF}$ inputs are the reference voltages that determine the full scale and zero input voltages, respectively, for the A/D converter. Thus, $+V_{REF}$ defines the analog input which produces a full scale output and $-V_{REF}$ defines the analog input which produces an output code of all zeroes. The transfer function for the A/D converter is shown in Figure 8.

$+V_{REF}$ and $-V_{REF}$ can be set to any voltage between GND and V_{CC}. This means that the reference voltages can be offset from GND and the difference between $+V_{REF}+$ and $-V_{REF}-$ can be made small to increase the resolution of the conversion. Note that the total unadjusted error increases when $[+V_{REF} - (-V_{REF})]$ decreases.

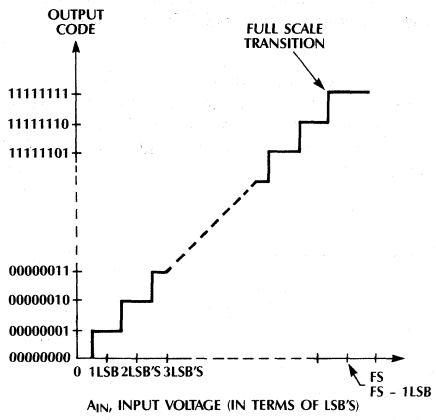


Figure 8. A/D Transfer Characteristic

1.4 POWER SUPPLY AND REFERENCE DECOUPLING

A 0.1μF ceramic disc capacitor is recommended to bypass V_{CC} to GND, using as short a lead length as possible.

If REF+ and REF– inputs are driven by long lines, they should be bypassed by 0.1μF ceramic disc capacitors at the reference input pins.

1.5 DYNAMIC PERFORMANCE

1.5.1 SINUSOIDAL INPUTS

Since the ML2261 has an internal sample and hold, the device can digitize high frequency sinusoids with little or no signal degradations. Using the Nyquist criteria, the highest frequency input to the converter could theoretically be 1/2 the sampling rate (f_s). Any frequency components above $f_s/2$ will be aliased below $f_s/2$. In most applications, these aliased components cause unacceptable distortion and must be filtered out of the input. If the input frequency is too close to $f_s/2$, then the requirements on the anti-alias filter become difficult to impossible to realize with standard component and tolerances. In most practical applications, the highest input frequency has to be limited to 1/3 to 1/4 of f_{max} in order to relax the filtering requirements enough to make a realizable anti-alias filter.

The maximum sampling rate (f_{max}) for the ML2261 in the WR-RD mode, ($t_{RD} < t_{INTL}$) can be calculated as follows:

$$f_{max} = \frac{1}{t_{WR} + t_{RD} + t_{RI} + t_P}$$

$$f_{max} = \frac{1}{180ns + 275ns + 215ns + 300ns}$$

f_{max} = 1.031 MHz

t_{WR} = Write Pulse Width

t_{RD} = Delay Time between $\overline{WR}$ and $\overline{RD}$ Pulses

t_{RI} = $\overline{RD}$ to $\overline{INT}$ Delay

t_P = Delay Time between Conversions

This permits a maximum sampling rate of 1MHz for the ML2261. The dynamic performance specifications (SNR, HD, IMD, and FR) for the ML2261 are all specified at 250kHz, which is approximately 1/4 of the sampling rate, f_s.

In applications where aliased frequency components are acceptable and filtering of the input signal is not needed or where a filter with a steep amplitude response is available, the user can apply an input sinusoid higher than 250kHz to the device. Note, however, that as the input frequency increases above 500kHz, dynamic performance degradation will occur due to the finite bandwidth of the internal sample and hold.

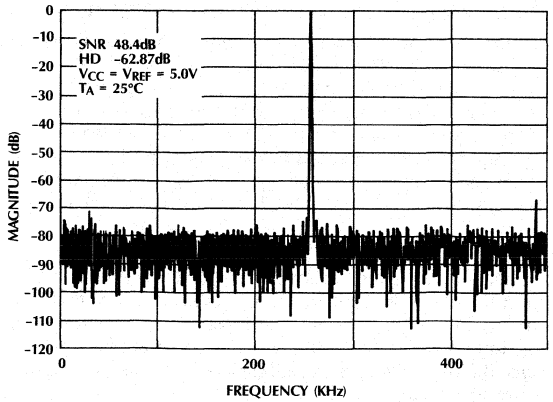
The Figure 9 plots are 4096 point FFT's of the ML2261 converting a 257kHz and a 491kHz, 0 to 4.5V, low distortion sine wave input. The ML2261 samples and digitizes at its specified accuracy, dynamic input signals with frequency components up to the Nyquist frequency (one-half the sampling rate). The output spectra yields precise measurements of the input signal level, harmonic components, and signal to noise ratio up to the 8-bit level. The near ideal signal to noise ratio is maintained independent of increasing analog input frequencies to 500kHz.

1.5.2 SIGNAL-TO-NOISE RATIO

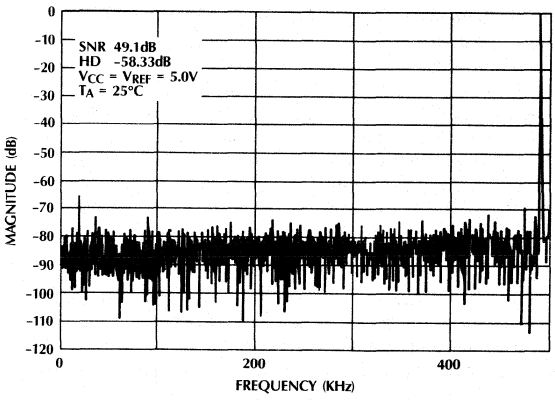
Signal-to-noise ratio (SNR) is the measured signal to noise at the output of the converter. The signal is the rms magnitude of the fundamental. Noise is the rms sum of all the nonfundamental signals up to half the sampling frequency. SNR is dependent on the number of quantization levels used in the digitization process; the more the levels, the smaller the quantization noise. The theoretical SNR for a sine wave is given by

$$SNR = (6.02N + 1.76)\ dB$$

where N is the number of bits. Thus for ideal 8-bit converter, SNR = 49.92 dB.



a) Ouput Spectrum with f_{IN} = 257kHz, f_S = 1MHz



b) Output Spectrum with f_{IN} = 491kHz, f_S = 1MHz

Figure 9. Dynamic Performance, Sample and Hold Mode

1.5.3 HARMONIC DISTORTION

Harmonic distortion is the ratio of the rms sum of harmonics to the fundamental. Total harmonic distortion (THD) of the ML2261 is defined as

$$20 \log = \frac{(V_2^2 + V_3^2 + V_4^2 + V_5^2)^{1/2}}{V_1}$$

where V_1 is the rms amplitude of the fundamental and V_2, V_3, V_4, V_5 are the rms amplitudes of the individual harmonics.

1.5.4 INTERMODULATION DISTORTION

With inputs consisting of sine waves at two frequencies, f_A and f_B, any active device with nonlinearities will create distortion products, of order (m + n), at sum and difference frequencies of $mf_A + nf_B$, where m, n = 0, 1, 2, 3 . . . Intermodulation terms are those for which m or n is not equal to zero. The (IMD) intermodulation distortion specification includes the second order terms ($f_A + f_B$) and ($f_A - f_B$) and the third order terms ($2f_A + f_B$), ($2f_A - f_B$), ($f_A + 2f_B$), and ($f_A - 2f_B$) only.

1.6 DIGITAL INTERFACE

The ML2261 has two basic interface modes, RD and WR-RD, which are selected by the MODE input pin.

1.6.1 RD MODE

In the RD mode, the $\overline{WR}$/RDY pin is configured as the RDY output. The read mode performs a conversion with a single $\overline{RD}$ pulse. This allows the μP to start a conversion, wait, and then read data with a single read instruction.

The timing for the RD mode is shown in Figure 2. To do a conversion, $\overline{CS}$ must be low to select the device. After $\overline{CS}$ goes low, the RDY output goes low indicating that the device is ready to do a conversion. The conversion starts on the falling edge of $\overline{RD}$. While $\overline{RD}$ is low, the MSB and LSB decisions are made with internally generated clock edges. When the conversion is complete, RDY goes high and $\overline{INT}$ goes low signaling the end of the conversion. After $\overline{INT}$ goes low, the data outputs go from high impedance to active state with valid output data. Data stays valid until either $\overline{RD}$ or $\overline{CS}$ goes high. When either signal goes high, the output data lines return to the high impedance state and $\overline{INT}$ returns high. A pull up resistor on RDY in the sample and hold mode will cause clock injection, degrading the total unadjusted error, unless $\overline{CS}\downarrow$ is $\geq$ 20ns before $\overline{RD}\downarrow$.

1.6.2 WR-RD MODE

In the WR-RD mode, the $\overline{WR}$/RDY pin is configured as the $\overline{WR}$ input. In this mode, $\overline{WR}$ initiates the conversion and $\overline{RD}$ controls reading the output data. This can be done in several ways, described below.

1.6.3 WR-RD MODE — USING INTERNAL DELAY ($t_{RD} > t_{INTL}$)

The timing is shown in Figure 3. To do a conversion, $\overline{CS}$ must be low to select the device. Then, $\overline{WR}$ falling edge triggers the conversion. While $\overline{WR}$ is low, the MSB comparison is made. When $\overline{WR}$ returns high the LSB decision is made. After some internal delay, $\overline{INT}$ goes low indicating end of conversion. Valid data will appear on DB0–7 when $\overline{RD}$ is pulled low. $\overline{INT}$ is then reset by the rising edge of either $\overline{CS}$ or $\overline{RD}$.

1.6.4 WR-RD MODE — READING BEFORE DELAY ($t_{RD} < t_{INTL}$)

The internally generated delay for the LSB decision when $t_{RD} > t_{INTL}$ is longer than necessary due to circuit design tolerances of t_{INTL} delay. If desired, a faster conversion will result without loss of accuracy by bringing $\overline{RD}$ low within the minimum time specified for t_{RD}. The timing diagram for this mode is shown in Figure 4. $\overline{WR}$ is the same as when $t_{RD} > t_{INTL}$. But in this case, $\overline{RD}$ is brought low t_{RD} ns after $\overline{WR}$ rising edge and before $\overline{INT}$. $\overline{INT}$ goes low indicating an end of conversion after the falling edge of $\overline{RD}$ and is reset on the rising edge of $\overline{RD}$ or $\overline{CS}$. When $\overline{RD}$ is brought low before $\overline{INT}$ goes low the data bus always remains in the high-impedance state until $\overline{INT}\downarrow$.

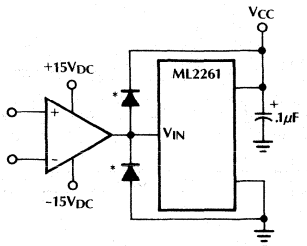
1.6.5 WR-RD MODE — STAND ALONE OPERATION

Stand alone operation can be implemented by tying $\overline{CS}$ and $\overline{RD}$ low as shown in Figure 5. $\overline{WR}$ initiates a conversion as before. When $\overline{WR}$ is low, the MSB comparison is made. When $\overline{WR}$ goes high, the LSB comparison is made. Since $\overline{RD}$ is already low, the output data will appear automatically at end of conversion. Since $\overline{RD}$ is always low, $\overline{INT}$ is reset on rising edge of $\overline{WR}$ and goes low at end of conversion.

1.6.6 POWER-ON RESET

When power is first applied, an internal power-on reset and timer circuit inhibits the $\overline{CS}$ input and resets the internal circuitry to prevent the ML2261 from starting in an unknown state. During this period of approximately 3μs, $\overline{INT}$ remains high and the data bus is in the high-impedance state.

2.0 TYPICAL APPLICATIONS



* NO PROTECTION IS REQUIRED IF INPUT CURRENT > 25mA

Figure 10. Protecting the Input

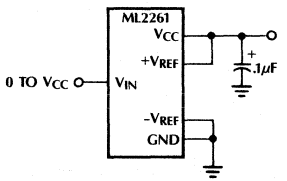


Figure 11. Using V_{CC} as Reference for Ratiometric Operation

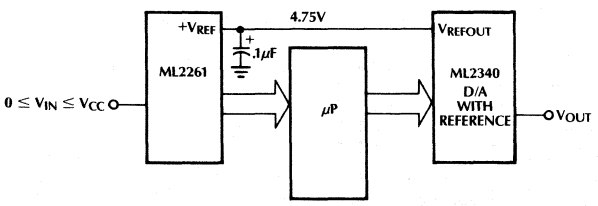


Figure 12. Using External Reference of D/A

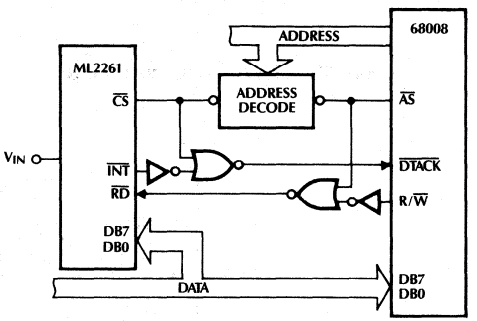


Figure 13. 68000 Type Interface to ML2261

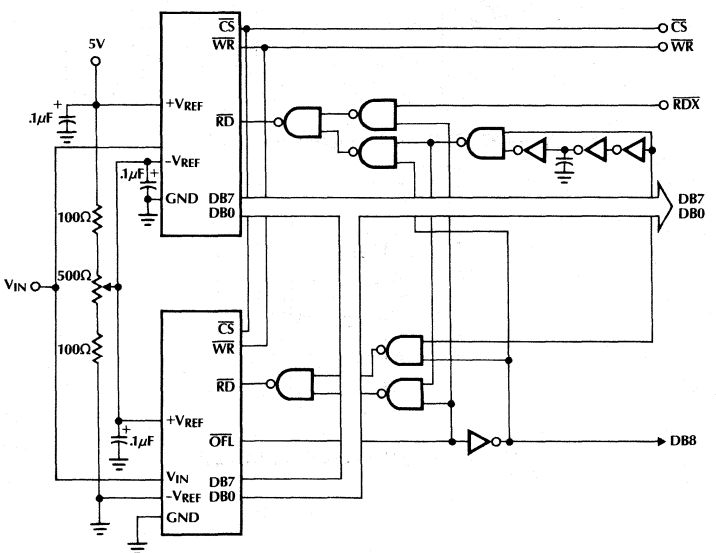


Figure 14. 9-Bit Resolution

2.0 TYPICAL APPLICATIONS (Continued)

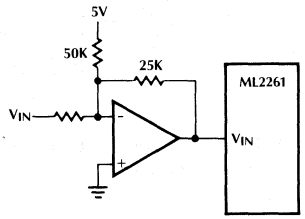


Figure 15. ±2.5V Analog Input Range

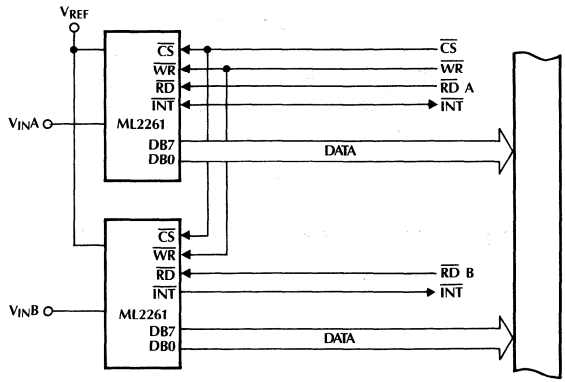


Figure 16. Simultaneous Sampling of Two Variables

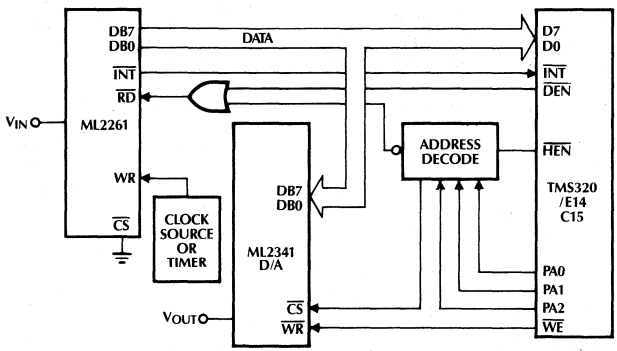


Figure 17. TMS320 Interface with D/A Output

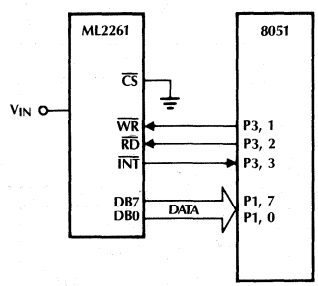


Figure 18. 8051 Interface to ML2261

TYPICAL APPLICATIONS (Continued)

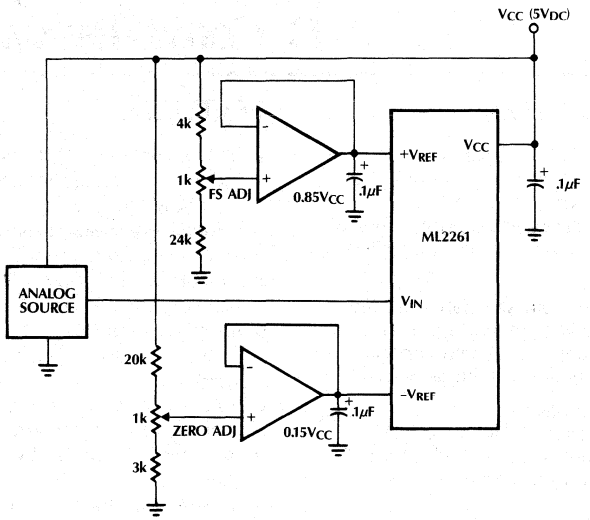


Figure 19. Operating with a Ratiometric Analog Signal of 15% of V_{CC} to 85% of V_{CC}

ORDERING INFORMATION

PART NUMBER	TOTAL UNADJUSTED ERROR	TEMPERATURE RANGE	PACKAGE
ML2261BMJ	±½ LSB	-55°C to +125°C	HERMETIC DIP
ML2261BIJ		-40°C to +85°C	HERMETIC DIP
ML2261BCP		0°C to +70°C	MOLDED DIP
ML2261BCQ		0°C to +70°C	MOLDED PCC
ML2261CMJ	±1 LSB	-55°C to +125°C	HERMETIC DIP
ML2261CIJ		-40°C to +85°C	HERMETIC DIP
ML2261CCP		0°C to +70°C	MOLDED DIP
ML2261CCQ		0°C to +70°C	MOLDED PCC

4-Channel High-Speed 8-Bit A/D Converter with T/H (S/H)

GENERAL DESCRIPTION

The ML2264 is a high-speed, μP compatible, 4-channel 8-bit A/D converter with a conversion time of 680ns over the operating temperature range and supply voltage tolerance. The ML2264 operates from a single 5V supply and has an analog input range from GND to V_{CC}.

The ML2264 has two different pin selectable modes. The T/H mode has an internal track and hold. The S/H mode has a true internal sample and hold and can digitize 0 to 5V sinusoidal signals as high as 500kHz.

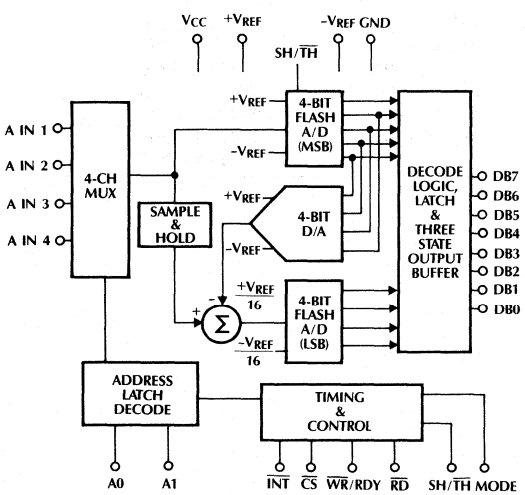
The ML2264 digital interface has been designed so that the device appears as a memory location or I/O port to a μP. Analog input channels are selected by the latched and decoded multiplexer address inputs.

The ML2264 is an enhanced, pin compatible second source for the industry standard AD7824. The ML2264 enhancements are faster conversion time, parameters guaranteed over the supply tolerance and temperature range, improved digital interface timing, superior power supply rejection, and better latchup immunity on analog inputs.

FEATURES

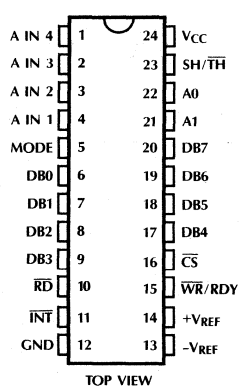
- Conversion time, WR-RD mode over temperature and supply voltage tolerance
  - Track & Hold Mode ..... 800ns max
  - Sample & Hold Mode ..... 680ns max
- Total unadjusted error ..... ±1/2 LSB or ±1 LSB
- Capable of digitizing a 5V, 250kHz sine wave
- 4-analog input channels
- No missing codes
- 0V to 5V analog input range with single 5V power supply
- No zero or full scale adjust required
- Analog input protection ..... 25mA min
- Operates ratiometrically or with up to 5V voltage reference
- No external clock required
- Power-on reset circuitry
- Low power 100mW
- Narrow 24-pin DIP or surface mount SOIC
- Superior pin compatible replacement for AD7824

BLOCK DIAGRAM



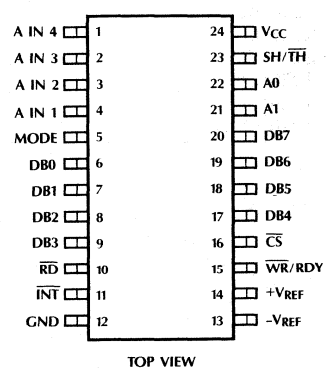
PIN CONNECTIONS

24-Pin DIP



TOP VIEW

24-Pin SOIC



TOP VIEW

PIN DESCRIPTION

PIN NO.	NAME	FUNCTION
1	A IN 4	Analog input 4.
2	A IN 3	Analog input 3.
3	A IN 2	Analog input 2.
4	A IN 1	Analog input 1.
5	MODE	Mode select input. MODE = GND: RD mode MODE = V_{CC}: WR-RD mode Pin has internal current source pulldown to GND.
6	DB0	Data output — bit 0 (LSB).
7	DB1	Data output — bit 1.
8	DB2	Data output — bit 2.
9	DB3	Data output — bit 3.
10	$\overline{RD}$	Read input. In RD mode, this pin initiates a conversion. In WR-RD mode, this pin latches data into output latches. See Digital Interface section.
11	$\overline{INT}$	Interrupt output. This output signals the end of a conversion and indicates that data is valid on the data outputs. See Digital Interface section.
12	GND	Ground.
13	$-V_{REF}$	Negative reference voltage for A/D converter.
14	$+V_{REF}$	Positive reference voltage for A/D converter.
15	$\overline{WR}$/RDY	Write input or ready output. In WR-RD mode, this pin is $\overline{WR}$ input. In RD mode, this pin is RDY open drain output. See Digital Interface section.
16	$\overline{CS}$	Chip select input. This pin must be held low for the device to perform a conversion.
17	DB4	Data output — bit 4.
18	DB5	Data output — bit 5.
19	DB6	Data output — bit 6.
20	DB7	Data output — bit 7 (MSB).
21	A1	Digital address input 1 that selects analog input channel. See multiplexer addressing section.
22	A0	Digital address input 0 that selects analog input channel. See multiplexer addressing section.
23	SH/$\overline{TH}$	S/H, T/H mode select. When SH/$\overline{TH}$ = V_{CC}, the device is in sample and hold mode. When SH/$\overline{TH}$ = GND, the device is in track and hold mode. Pin has internal pulldown current source to GND.
24	V_{CC}	Positive supply. +5 volts ± 5%.

ABSOLUTE MAXIMUM RATINGS
(Note 1)

Supply Voltage, V_{CC} 6.5V
Voltage
  Logic Inputs ..... –0.3V to V_{CC} + 0.3V
  Analog Inputs ..... –0.3V to V_{CC} + 0.3V
Input Current per Pin (Note 2) ..... ±25mA
Storage Temperature ..... –65°C to +150°C
Package Dissipation
  at T_A = 25°C (Board Mount) 875mW
Lead Temperature (Soldering 10 sec.)
  Dual-In-Line Package (Plastic) ..... 260°C
  Dual-In-Line Package (Ceramic) ..... 300°C
  SOIC
    Vapor Phase (60 sec.) ..... 215°C
    Infrared (15 sec.) ..... 220°C

OPERATING CONDITIONS

Supply Voltage, V_{CC} ..... $4.5V_{DC}$ to $6.0V_{DC}$
Temperature Range (Note 3) ..... $T_{MIN} \leq T_A \leq T_{MAX}$
  ML2264BMJ, ML2264CMJ ..... –55°C to +125°C
  ML2264BIJ, ML2264CIJ ..... –40°C to +85°C
  ML2264BCS, ML2264CCS
  ML2264BCP, ML2264CCP ..... 0°C to +70°C

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, $T_A = T_{MIN}$ to T_{MAX}, $V_{CC} = +V_{REF} = 5V \pm 5\%$, and $-V_{REF} = GND$

PARAMETER	NOTES	CONDITIONS	ML2264XCX			ML2264XIX, ML2264XMX			UNITS
			MIN	TYP (Note 4)	MAX	MIN	TYP (Note 4)	MAX	
Converter									
Total Unadjusted Error ML2264BXX ML2264CXX	5, 7	$V_{REF} = V_{CC}$			 ±1/2 ±1			 ±1/2 ±1	 LSB LSB
Integral Linearity Error ML2264BXX ML2264CXX	5, 7	$V_{REF} = V_{CC}$			 ±1/2 ±1			 ±1/2 ±1	 LSB LSB
Differential Linearity Error ML2264BXX ML2264CXX	5	$V_{REF} = V_{CC}$			 ±1/2 ±1			 ±1/2 ±1	 LSB LSB
Full Scale Error ML2264BXX ML2264CXX	5				 ±1/2 ±1			 ±1/2 ±1	 LSB LSB
Zero Scale Error ML2264BXX ML2264CXX	5				 ±1/2 ±1			 ±1/2 ±1	 LSB LSB
Channel to Channel Mismatch	5				±1/4			±1/4	LSB
$+V_{REF}$ Voltage Range	6		$-V_{REF}$		$V_{CC}+0.1$	$-V_{REF}$		$V_{CC}+0.1$	V
$-V_{REF}$ Voltage Range	6		GND–0.1		$+V_{REF}$	GND–0.1		$+V_{REF}$	V
Reference Input Resistance	5		1	2	3	1	2	3	kΩ
Analog Input Range	5, 8		GND–0.1		$V_{CC}+0.1$	GND–0.1		$V_{CC}+0.1$	V
Power Supply Sensitivity	5	DC $V_{CC}=5V\pm5\%$, $V_{REF}=4.50V$		±1/32	±1/4		±1/32	±1/4	LSB
		100mVp-p 100kHz sine on V_{CC}, $V_{IN} = 0$		±1/16			±1/16		LSB
Analog Input Leakage Current, OFF Channel	5	ON Channel = V_{CC} OFF Channel = 0V	–1			–1			µA
		ON Channel = 0V OFF Channel = V_{CC}			1			1	µA
Analog Input Leakage Current, ON Channel	5	ON Channel = 0V OFF Channel = V_{CC}	–1			–1			µA
		ON Channel = V_{CC} OFF Channel = 0V			1			1	µA
Analog Input Capacitance		During Acquisition Period		45			45		pF
Digital and DC									
$V_{IN(1)}$, Logical "1" Input Voltage	5	$\overline{WR}$, $\overline{RD}$, $\overline{CS}$, A0, A1	2.0			2.0			V
		MODE, SH/$\overline{TH}$	$V_{CC}-0.5$			$V_{CC}-0.5$			V
$V_{IN(0)}$, Logical "0" Input Voltage	5	$\overline{WR}$, $\overline{RD}$, $\overline{CS}$, A0, A1			0.8			0.8	V
		MODE, SH/$\overline{TH}$			0.5			0.5	V

ELECTRICAL CHARACTERISTICS (Continued)

Unless otherwise specified, $T_A = T_{MIN}$ to T_{MAX}, $V_{CC} = +V_{REF} = 5V \pm 5\%$, $-V_{REF}$ = GND, and timing measured at 1.4V, C_L = 100pF.

PARAMETER	NOTES	CONDITIONS	ML2264XCX MIN	ML2264XCX TYP (Note 4)	ML2264XCX MAX	ML2264XIX, ML2264XMX MIN	ML2264XIX, ML2264XMX TYP (Note 4)	ML2264XIX, ML2264XMX MAX	UNITS
Digital and DC (Continued)									
$I_{IN(1)}$, Logical "1" Input Current	5	$V_{IH}=V_{CC}$; $\overline{WR}$, $\overline{RD}$, $\overline{CS}$, A0, A1			1			1	µA
		$V_{IH}=V_{CC}$; MODE, SH/$\overline{TH}$	15	50	150	15	50	150	µA
$I_{IN(0)}$, Logical "0" Input Current	5	V_{IL}=GND; $\overline{WR}$, $\overline{RD}$, $\overline{CS}$	-1			-1			µA
		V_{IL}=GND; MODE, SH/$\overline{TH}$	-20			-20			µA
$V_{OUT(1)}$, Logical "1" Output Voltage	5	I_{OUT} = -2mA	4.0			4.0			V
$V_{OUT(0)}$, Logical "0" Output Voltage	5	I_{OUT} = 2mA			0.4			0.4	V
I_{OUT}, Three-State Output Current	5	V_{OUT} = 0V	-1			-1			µA
		V_{OUT} = V_{CC}			1			1	µA
C_{OUT}, Logic Output Capacitance				5			5		pF
C_{IN}, Logic Input Capacitance				5			5		pF
I_{CC}, Supply Current	5	$\overline{CS}$ = $\overline{WR}$ = $\overline{RD}$ = "1" No Output Load			25			27	mA
AC and Dynamic Performance (Note 9)									
t_{CRD}, Conversion Time, Read Mode	5	$\overline{RD}$ to $\overline{INT}$, MODE = 0V			1020			1100	ns
t_{CWR-RD}, Conversion Time, Write-Read Mode	5, 9	$\overline{WR}$ Falling Edge to $\overline{INT}$, $t_{RD} < t_{INT}$, MODE = V_{CC}; SH/$\overline{TH}$=V_{CC}			680			735	ns
		$\overline{WR}$ Falling Edge to $\overline{INT}$, $t_{RD} < t_{INT}$, MODE = V_{CC}; SH/$\overline{TH}$=GND			800			880	ns
SNR, Signal to Noise Ratio		V_{IN} = 5V, 250kHz Noise is sum of all nonfundamental components from 0-500kHz. SH/$\overline{TH}$ = V_{CC}, MODE = V_{CC} $f_{SAMPLING}$ = 1.0 MHz		48			48		dB
HD, Harmonic Distortion		V_{IN} = 5V, 250kHz THD is sum of 2-5th harmonics relative to fundamental. SH/$\overline{TH}$ = V_{CC}, MODE = V_{CC} $f_{SAMPLING}$ = 1.0 MHz		-63			-63		dB
IMD, Intermodulation Distortion		fa = 2.5V, 250kHz fb = 2.5V, 248kHz IMB is (fa + fb), (fa - fb), (2fa + fb), (2fa - fb), (fa + 2fb), or (fa - 2fb) relative to fundamental. SH/$\overline{TH}$ = V_{CC}, MODE = V_{CC} $f_{SAMPLING}$ = 1.0 MHz		-60			-60		dB

2

ELECTRICAL CHARACTERISTICS (Continued)

Unless otherwise specified, $T_A = T_{MIN}$ to T_{MAX}, $V_{CC} = +V_{REF} = 5V \pm 5\%$, $-V_{REF}$ = GND, and timing measured at 1.4V, C_L = 100pF

PARAMETER	NOTES	CONDITIONS	ML2264XCX MIN	ML2264XCX TYP (Note 4)	ML2264XCX MAX	ML2264XIX, ML2264XMX MIN	ML2264XIX, ML2264XMX TYP (Note 4)	ML2264XIX, ML2264XMX MAX	UNITS
AC and Dynamic Performance (Note 9) (Continued)									
FR, Frequency Response		V_{IN} = 5V, 0–250kHz Relative to 1kHz SH/$\overline{TH}$ = V_{CC}, MODE = V_{CC} $f_{SAMPLING}$ = 1.0 MHz		±0.1			±0.1		dB
SR, Slew Rate Tracking	6	SH/$\overline{TH}$ = V_{CC}			4.0			4.0	V/μs
		SH/$\overline{TH}$ = GND			.25			.25	V/μs
t_{AS}, Multiplexer Address Setup Time	5	SH/$\overline{TH}$ = GND, Figure 1 (Track & Hold Operation)	0			0			ns
t_{AH}, Multiplexer Address Hold Time	5	SH/$\overline{TH}$ = GND, Figure 1 (Track & Hold Operation)	60			70			ns
t_{AS}, Multiplexer Address Setup Time	5	SH/$\overline{TH}$ = V_{CC}, Figure 2 (Sample & Hold Operation)	225			245			ns
t_{AH}, Multiplexer Address Hold Time	5	SH/$\overline{TH}$ = V_{CC}, Figure 2 (Sample & Hold Operation)	60			70			ns
AC Performance Read Mode (Pin 5 = 0V), Figure 4									
t_{RDY}, $\overline{CS}$ to RDY Delay	5		0		50	0		55	ns
t_{RDD}, $\overline{RD}$ Low to RDY Delay	5, 10	Figure 3			1020			1100	ns
t_{CSS}, $\overline{CS}$ to $\overline{RD}$, $\overline{WR}$ Setup Time	5		0			0			ns
t_{CSH}, $\overline{CS}$ to $\overline{RD}$, $\overline{WR}$ Hold Time	5		0			0			ns
t_{CRD}, Conversion Time — $\overline{RD}$ Low to $\overline{INT}$ Low	5, 10				1020			1100	ns
t_{ACC0}, Data Access Time $\overline{RD}$ to Data Valid	5		t_{CRD}		t_{CRD}+30	t_{CRD}		t_{CRD}+30	ns
t_{RDPW}, $\overline{RD}$ Pulse Width	5		t_{CRD}+30			t_{CRD}+30			ns
t_{INTH}, $\overline{RD}$ to $\overline{INT}$ Delay	5, 10		0		60	0		70	ns
t_{DH}, Data Hold Time — $\overline{RD}$ Rising Edge to Data High Impedance State	6, 10	Figure 3	0		50	0		60	ns
t_P, Delay Time Between Conversions — $\overline{INT}$ Low to $\overline{RD}$ Low	5, 10	Sample & Hold Mode, SH/$\overline{TH}$ = V_{CC}	300			325			ns
		Track & Hold Mode, SH/$\overline{TH}$ = GND	240			260			ns
AC Performance Write-Read Mode (Pin 5 = 5V), Figures 5 and 6									
t_{CSS}, $\overline{CS}$ to $\overline{RD}$, $\overline{WR}$ Setup Time	5		0			0			ns
t_{CSH}, $\overline{CS}$ to $\overline{RD}$, $\overline{WR}$ Hold Time	5		0			0			ns
t_{WR}, $\overline{WR}$ Pulse Width	5	SH/$\overline{TH}$ = V_{CC}	190		50K	205		50K	ns
	6	SH/$\overline{TH}$ = GND	320		50K	360		50K	ns

ELECTRICAL CHARACTERISTICS (Continued)

Unless otherwise specified, $T_A = T_{MIN}$ to T_{MAX}, $V_{CC} = +V_{REF} = 5V \pm 5\%$, $-V_{REF}$ = GND, and timing measured at 1.4V, C_L = 100pF

PARAMETER	NOTES	CONDITIONS	ML2264XCX			ML2264XIX, ML2264XMX			UNITS
			MIN	TYP (Note 4)	MAX	MIN	TYP (Note 4)	MAX	
AC Performance Write-Read Mode (Pin 5 = 5V), Figures 5 and 6 (Continued)									
t_{RD}, Read Time — $\overline{WR}$ High to $\overline{RD}$ Low Delay	5	$t_{RD} < t_{INTL}$	275			300			ns
t_{RI}, $\overline{RD}$ to $\overline{INT}$ Delay	5, 10	$t_{RD} < t_{INTL}$	0		215	0		230	ns
t_{ACC1}, Data Access Time — $\overline{RD}$ Low to Data Valid	5	$t_{RD} < t_{INTL}$	0		220	0		240	ns
t_{CWR-RD}, Conversion Time — $\overline{WR}$ Falling Edge to $\overline{INT}$ Low	5,9,10	$t_{RD} < t_{INTL}$, SH/$\overline{TH}$ = V_{CC}			680			735	ns
	6,9,10	$t_{RD} < t_{INTL}$, SH/$\overline{TH}$ = GND			810			890	ns
t_{INTL}, Internal Comparison Time — $\overline{WR}$ Rising Edge to $\overline{INT}$ Low	5, 10	$t_{RD} > t_{INTL}$			620			670	ns
t_{ACC2}, Data Access Time — $\overline{RD}$ to Data Valid	5	$t_{RD} > t_{INTL}$	0		50	0		60	ns
t_{DH}, Data Hold Time — $\overline{RD}$ Rising Edge to Data High Impedance State	6, 10	Figure 3	0		50	0		60	ns
t_{INTH}, $\overline{RD}$↑ to $\overline{INT}$↑ Delay	5, 10		0		60	0		70	ns
t_P, Delay Time Between Conversions — $\overline{INT}$ Low to $\overline{WR}$ Low	5, 10	Sample & Hold Mode, SH/$\overline{TH}$ = V_{CC}	300			325			ns
		Track & Hold Mode, SH/$\overline{TH}$ = GND	240			260			ns
t_{IHWR}, $\overline{WR}$↑ to $\overline{INT}$↑ Delay	5, 10	Standalone Mode	0		90	0		100	ns
t_{ID}, $\overline{INT}$↓ to Data Valid Delay	5, 10	Standalone Mode	0		20	0		30	ns

Note 1: Absolute maximum ratings are limits beyond which the life of the integrated circuit may be impaired. All voltages unless otherwise specified are measured with respect to ground.

Note 2: When the voltage at any pin exceeds the power supply rails ($V_{IN} <$ GND or $V_{IN} > V_{CC}$) the absolute value of current at that pin should be limited to 25mA or less.

Note 3: -55°C to +125°C operating temperature range devices are 100% tested at temperature extremes with worst-case test conditions. 0°C to +70°C and -40°C to +85°C operating temperature range devices are 100% tested with temperature limits guaranteed by 100% testing, sampling, or by correlation with worst-case test conditions.

Note 4: Typicals are parametric norm at 25°C.

Note 5: Parameter guaranteed and 100% production tested.

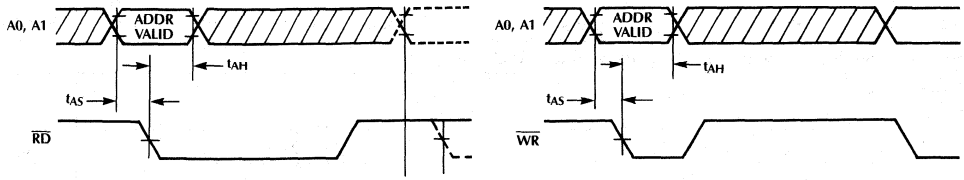
Note 6: Parameter guaranteed. Parameters not 100% tested are not in outgoing quality level calculation.

Note 7: Total unadjusted error includes offset, full scale, linearity, sample and hold, and multiplexer errors. Total unadjusted error is tested at the minimum specified times for $\overline{WR}$, $\overline{RD}$, t_{R1}, and t_P. For example, for the ML2264XCX in the sample and hold mode, $\overline{WR}$/$\overline{RD}$ mode: t_{WR} = 190ns, t_{RD} = 275ns with a frequency of 1.020MHz (cycle time of 980ns).

Note 8: For $-V_{REF} \geq V_{IN}$ the digital output code will be 0000 0000. Two on-chip diodes are tied to the analog input which will forward conduct for analog input voltages one diode drop below ground or one diode drop greater than the V_{CC} supply. Be careful, during testing at low V_{CC} levels (4.5V), as high level analog inputs (5V) can cause this input diode to conduct — especially at elevated temperatures, and cause errors for analog inputs near full scale. The spec allows 100mV forward bias of either diode. This means that as long as the analog V_{IN} or V_{REF} does not exceed the supply voltage by more than 100mV, the output code will be correct. To achieve an absolute $0V_{DC}$ to $5V_{DC}$ input voltage range will therefore require a minimum supply voltage of $4.900V_{DC}$ over temperature variations, initial tolerance and loading.

Note 9: Conversion time, write-read mode = $t_{WR} + t_{RD} + t_{RI}$.

Note 10: Defined from the time an output crosses 0.8V or 2.4V.



a) RD Mode (Pin 5 = GND) b) WR-RD Mode (Pin 5 = V_{CC})

Figure 1. Analog Multiplexer Address Timing for Track & Hold Mode (Pin 23 = GND)

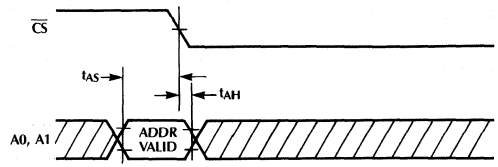


Figure 2. Analog Multiplexer Address Timing for Sample & Hold Mode (Pin 23 = V_{CC})

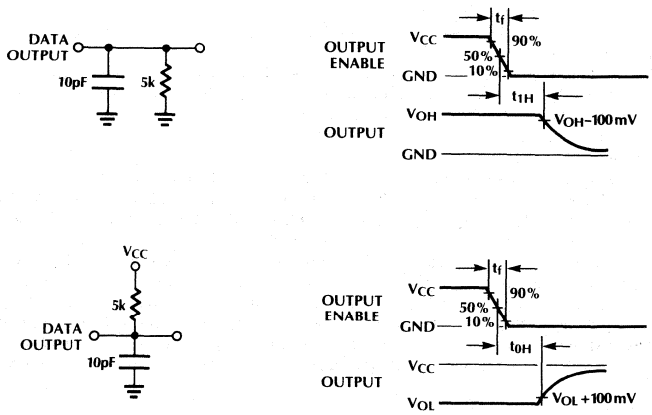
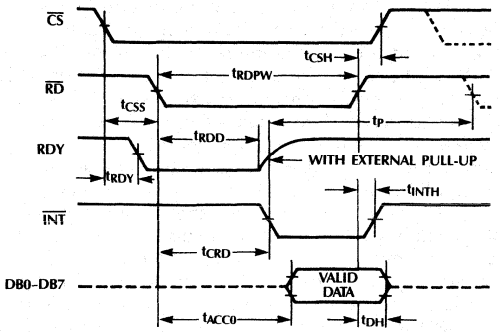


Figure 3. High Impedance Test Circuits and Waveforms



* In SAMPLE & HOLD mode a pull up resistor on RDY should not be used unless CS↓ is ≥ 20ns before RD↓.

Figure 4. RD Mode Timing

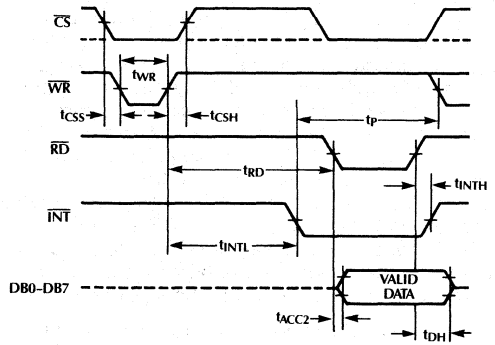


Figure 5. WR-RD Mode Timing ($t_{RD} > t_{INTL}$)

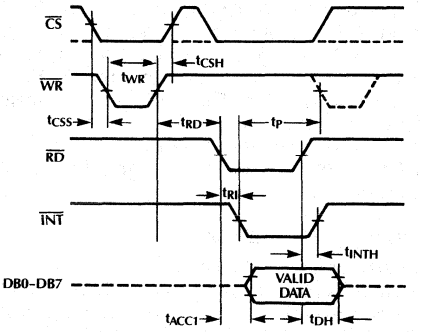


Figure 6. WR-RD Mode Timing ($t_{RD} < t_{INTL}$)

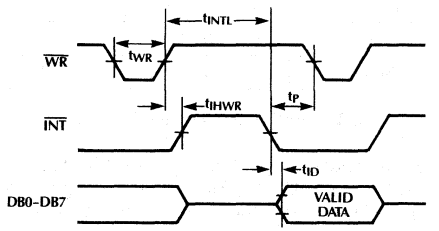


Figure 7. WR-RD Mode Stand-Alone Timing $\overline{CS}$ = $\overline{RD}$ = 0

2

1.0 FUNCTIONAL DESCRIPTION

The ML2264 uses a two stage flash technique for A/D conversion. This technique first performs a 4 bit flash conversion on V_{IN} to determine the 4 MSB's. These 4 MSB's are then cycled through an internal DAC to recreate the analog input. This reconstructed analog input signal from the DAC is then subtracted from the input, and the difference voltage is converted by a second 4 bit flash conversion, providing the 4 LSB's of the output data word.

1.1 MULTIPLEXER ADDRESSING

The ML2264 contains a 4-channel single ended analog multiplexer. A particular input channel is selected by using the address inputs A0 and A1. The relationship between the address inputs, A0 and A1, and the analog input selected is shown in Table 1.

Selected Analog Channel	Address Input	
	A0	A1
A IN 1	0	0
A IN 2	1	0
A IN 3	0	1
A IN 4	1	1

Table 1. Multiplexer Address Decoding

The address inputs are latched into the ML2264 on the falling edge of the $\overline{RD}$, $\overline{WR}$, or $\overline{CS}$ depending on the state of pins SH/TH and mode as shown in Table 2.

Address Latching Signal	Mode	Operation Mode
$\overline{RD}$↓	GND	GND
$\overline{WR}$↓	V_{CC}	GND
$\overline{CS}$↓	GND	V_{CC}
$\overline{CS}$↓	V_{CC}	V_{CC}

Table 2.

In the Sample & Hold mode of operation $\overline{CS}$ is used as the address latch enable, allowing for continuous conversions without addressing a given analog input for each conversion.

The Track & Hold mode of operation requires an analog input to be addressed and latched for each conversion that the ML2264 performs.

1.2 ANALOG INPUTS

The analog input on the ML2264 behaves differently than inputs on conventional converters. The analog input current requirements change while the conversion is in progress, and the amount of input current depends on what cycle the converter is in.

The equivalent input circuit for the converter is shown in Figure 8. When the conversion starts in the T/H mode ($\overline{WR}$↓ in the WR-RD mode or $\overline{RD}$↓ in the RD mode) S1, S4 and S6 close and S3 opens. This period is known as the acquisition period where the MSB flash converter tracks the input signal and the LSB flash converter samples it. During this period, V_{IN} is connected to the 16 MSB and 15 LSB comparators. Thus 38 pF of input capacitance must be charged up through the combined R_{ON} resistance of the internal analog switches plus any external source resistance, R_S. In addition, there is a stray capacitance of approximately 11 pF that needs to be charged through the external source resistance R_S. This period ends in the WR-RD mode when $\overline{WR}$↑ or by an internal timer in the RD mode. At this point S1 and S4 open and the analog input at V_{IN} is no longer being sampled; thus during this time the analog voltage on V_{IN} does not affect converter performance.

As shown above, the critical period for charging up the analog input occurs when the MSB and LSB comparators are sampling the input, known as the acquisition period. The source of the external signal on V_{IN} must adequately charge up the analog voltage during the acquisition period. To do this, the input must settle within the required analog accuracy tolerance at least 50ns before the end of the acquisition period so that the MSB comparators have adequate time to make the correct decision. If more time is needed due to finite charging or settling time of the external source, the $\overline{WR}$ low period can be extended in WR-RD mode. In RD mode, since the acquisition time is fixed by internal delays, the burden is on the external source to charge up and settle the input adequately.

When the ML2264 operates in the S/H mode (pin 23 = V_{CC}) both the MSB and the LSB flash converter perform a true sample and hold operation during the acquisition or sampling period. This period starts after the falling edge of $\overline{INT}$ and ends with the falling edge of $\overline{WR}$ in the WR-RD mode or the falling edge of $\overline{RD}$ in the RD mode. The duration of this period is user controlled and must satisfy a minimum of t_P.

During this period S1, S3, S4 and S6 close, therefore 46 pF of input capacitance must be charged up in addition to the 11 pF of stray capacitance.

1.3 TRACK AND HOLD vs. SAMPLE AND HOLD

The MSB Flash Converter of the ML2264 in T/H mode has a track and hold mechanism for sampling the input. The input is attached to the MSB comparators directly in the MSB compare cycle, or acquisition period. When the MSB compare cycle ends, the state of the MSB comparators is latched. The LSB Flash Converter always performs a S/H operation. Thus, the analog input signal can be changing during the MSB compare cycle, or acquisition period, and the MSB comparators will be

tracking it as long as the slew rate of the analog input is slow enough so that the MSB comparators can respond. The ML2264 can track and hold signals with slew rates as high as .25V/μs (16kHz @ 5 volts) without sacrificing conversion accuracy.

The ML2264 in S/H mode does not have the slew rate limitation of the T/H mode since an internal sample and hold acquires the analog signal, holds it internally, and then performs a conversion. Since this is a true sample and hold function, the S/H mode can theoretically digitize signals of frequencies much higher than the T/H mode. The ML2264 in S/H mode can digitize signals of frequencies as high as 250kHz @ 5V (slew rates as high as 4V/μs) without sacrificing conversion accuracy. In most applications, the S/H mode is more desirable than T/H mode because of the better dynamic performance.

1.3.1 CONVERTER — T/H MODE

The operating sequence for the WR-RD mode is illustrated in Figure 9a. Initially, the internal comparators are auto-zeroed while $\overline{WR}$ is high. A conversion is initiated by the falling edge of $\overline{WR}$. While $\overline{WR}$ is low, the MSB comparators are tracking the analog input and comparing this voltage against voltages from the internal resistor ladder. At the same time, the input is being acquired or sampled by LSB comparators. On the rising edge of $\overline{WR}$, the MSB comparator results are latched, and the LSB acquisition time is ended by closing the sampling switch to the LSB comparators. While $\overline{WR}$ is high, the LSB comparators then compare the residual input voltage against internal voltages from the resistor ladder to determine the 4 LSB's. When the LSB comparison or conversion is complete, $\overline{INT}$ goes low and latches the conversion result into the output latches. Then, the comparators are auto-zeroed while $\overline{WR}$ is high before another conversion can start.

The operating sequence for RD mode, is similar to that described above for the WR-RD mode, except the conversion is initiated by the falling edge of $\overline{RD}$, and the MSB and LSB conversions are generated by internal clock edges that are generated while $\overline{RD}$ is low.

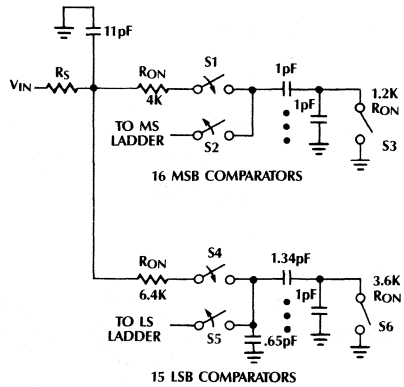


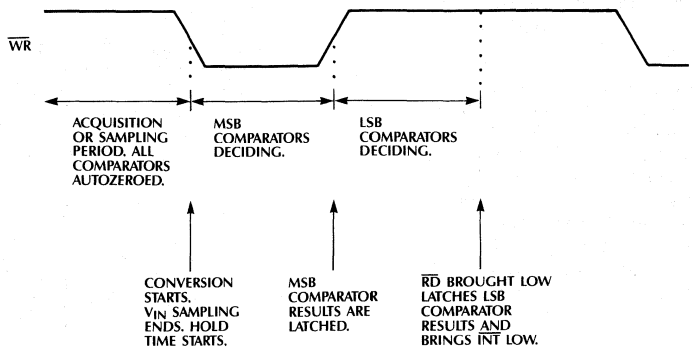
Figure 8. Converter Equivalent Input Circuit

1.3.2 CONVERTER — S/H MODE

The operating sequence for S/H mode is illustrated in Figure 9b. Notice that it is similar to T/H mode described above except this mode has a true sample and hold function. The falling edge of $\overline{INT}$ closes the sampling switch and starts the acquisition period where the analog input is sampled at the same time all comparators are auto-zeroed. The falling edge of $\overline{WR}$ opens the internal sampling switch, ends the acquisition period, and starts the conversion on the internally sample and held signal. The MSB comparators make their decisions while $\overline{WR}$ is low. On the rising edge of $\overline{WR}$, the MSB comparator results are latched. The LSB comparators make their decision when $\overline{WR}$ is high. When the LSB comparison or conversion is complete, $\overline{INT}$ goes low and latches the conversion result into the output buffers. Then, the acquisition period begins again and the converter is ready for the next conversion.

The operating sequence for the RD mode is the same as the WR-RD mode, except the conversion is initiated by the falling edge of $\overline{RD}$, and the MSB and LSB conversions are generated by internal clock edges that are generated while $\overline{RD}$ is low.

a). T/H Mode



b). S/H Mode

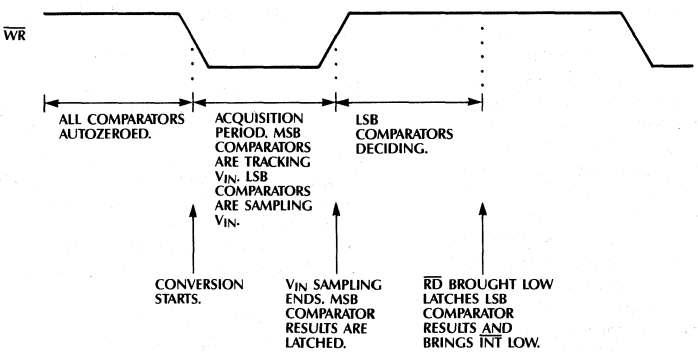


Figure 9. Operating Sequence (WR-RD Mode)

1.4 REFERENCE

The $+V_{REF}$ and $-V_{REF}$ inputs are the reference voltages that determine the full scale and zero input voltages, respectively, for the A/D converter. Thus, $+V_{REF}$ defines the analog input which produces a full scale output and $-V_{REF}$ defines the analog input which produces an output code of all zeroes. The transfer function for the A/D converter is shown in Figure 10.

$+V_{REF}$ and $-V_{REF}$ can be set to any voltage between GND and V_{CC}. This means that the reference voltages can be offset from GND and the difference between $+V_{REF}+$ and $-V_{REF}-$ can be made small to increase the resolution of the conversion. Note that the total unadjusted error increases when $[+V_{REF} - (-V_{REF})]$ decreases.

1.5 POWER SUPPLY AND REFERENCE DECOUPLING

A 0.1μF ceramic disc capacitor is recommended to bypass V_{CC} to GND, using as short a lead length as possible.

If REF+ and REF– inputs are driven by long lines, they should be bypassed by 0.1μF ceramic disc capacitors at the reference input pins.

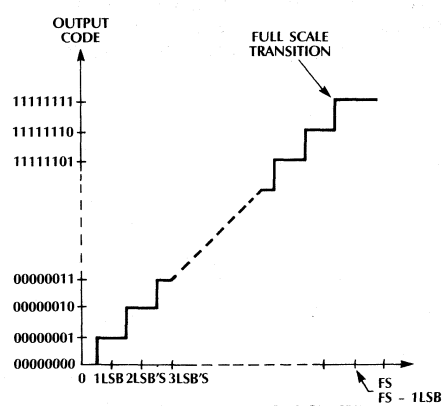


Figure 10. A/D Transfer Characteristic

1.6 DYNAMIC PERFORMANCE

1.6.1 SINUSOIDAL INPUTS

Since the ML2264 has an internal sample and hold, the device can digitize high frequency sinusoids with little or no signal degradations. Using the Nyquist criteria, the highest frequency input to the converter could theoretically be 1/2 the sampling rate (f_S). Any frequency components above $f_S/2$ will be aliased below $f_S/2$. In most applications, these aliased components cause unacceptable distortion and must be filtered out of the input. If the input frequency is too close to $f_S/2$, then the requirements on the anti-alias filter become difficult to impossible to realize with standard component and tolerances. In most practical applications, the highest input frequency has to be limited to 1/3 to 1/4 of f_{MAX} in order to relax the filtering requirements enough to make a realizable anti-alias filter.

The maximum sampling rate (f_{max}) for the ML2264 in the WR-RD mode, ($t_{RD} < t_{INTL}$) can be calculated as follows:

$$f_{max} = \frac{1}{t_{WR} + t_{RD} + t_{RI} + t_P}$$

$$f_{max} = \frac{1}{190ns + 275ns + 215ns + 300ns}$$

f_{max} = 1.020 MHz

t_{WR} = Write Pulse Width

t_{RD} = Delay Time between $\overline{WR}$ and $\overline{RD}$ Pulses

t_{RI} = $\overline{RD}$ to $\overline{INT}$ Delay

t_P = Delay Time between Conversions

This permits a maximum sampling rate of 1MHz for the ML2264. The dynamic performance specifications (SNR, HD, IMD, and FR) for the ML2264 are all specified at 250kHz, which is approximately 1/4 of the sampling rate, f_S.

In applications where aliased frequency components are acceptable and filtering of the input signal is not needed, or where a filter with a steep amplitude response is available, the user can apply an input sinusoid higher than 250kHz to the device. Note, however, that as the input frequency increases above 500kHz, dynamic performance degradation will occur due to the finite bandwidth of the internal sample and hold.

The Figure 11 plots are 4096 point FFT's of the ML2264 converting a 257kHz and a 491kHz, 0 to 4.5V, low distortion sine wave input. The ML2264 samples and digitizes at its specified accuracy, dynamic input signals with frequency components up to the Nyquist frequency (one-half the sampling rate). The output spectra yields precise measurements of the input signal level, harmonic components, and signal to noise ratio up to the 8-bit level. The near ideal signal to noise ratio is maintained independent of increasing analog input frequencies to 500kHz.

1.6.2 SIGNAL-TO-NOISE RATIO

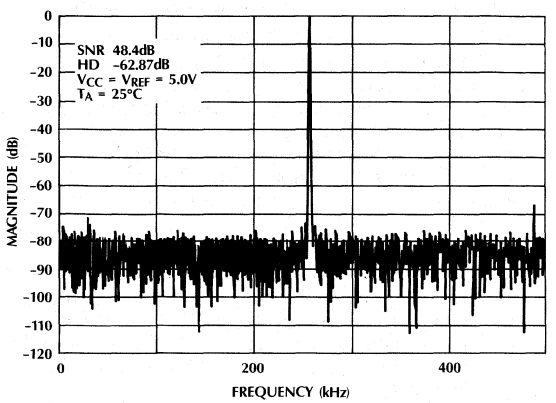
Signal-to-noise ratio (SNR) is the measured signal to noise at the output of the converter. The signal is the rms magnitude of the fundamental. Noise is the rms sum of all the nonfundamental signals up to half the sampling frequency. SNR is dependent on the number of quantization levels used in the digitization process; the more the levels, the smaller the quantization noise. The theoretical SNR for a sine wave is given by

$$SNR = (6.02N + 1.76)\ dB$$

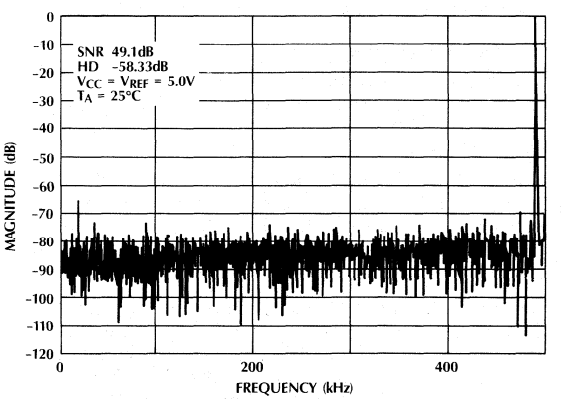
where N is the number of bits. Thus for ideal 8-bit converter, SNR = 49.92 dB.

1.6.3 HARMONIC DISTORTION

Harmonic distortion is the ratio of the rms sum of harmonics to the fundamental. Total harmonic distortion (THD) of the ML2264 is defined as



a) Output Spectrum with f_{IN} = 257kHz, f_S = 1MHz



b) Output Spectrum with f_{IN} = 491kHz, f_S = 1MHz

Figure 11. Dynamic Performance, Sample and Hold Mode

$$20 \log = \frac{(V_2^2 + V_3^2 + V_4^2 + V_5^2)^{1/2}}{V_1}$$

where V_1 is the rms amplitude of the fundamental and V_2, V_3, V_4, V_5 are the rms amplitudes of the individual harmonics.

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where V_1 is the rms amplitude of the fundamental and V_2, V_3, V_4, V_5 are the rms amplitudes of the individual harmonics.

1.6.4 INTERMODULATION DISTORTION

With inputs consisting of sine waves at two frequencies, f_A and f_B, any active device with nonlinearities will create distortion products, of order (m + n), at sum and difference frequencies of $mf_A + nf_B$, where m, n = 0, 1, 2, 3 . . . Intermodulation terms are those for which m or n is not equal to zero. The (IMD) intermodulation distortion specification includes the second order terms $(f_A + f_B)$ and $(f_A - f_B)$ and the third order terms $(2f_A + f_B)$, $(2f_A - f_B)$, $(f_A + 2f_B)$, and $(f_A - 2f_B)$ only.

1.7 DIGITAL INTERFACE

The ML2264 has two basic interface modes, RD and WR-RD, which are selected by the MODE input pin.

1.7.1 RD MODE

In the RD mode, the $\overline{WR}/RDY$ pin is configured as the RDY output. The read mode performs a conversion with a single $\overline{RD}$ pulse. This allows the μP to start a conversion, wait, and then read data with a single read instruction.

The timing for the $\overline{RD}$ mode is shown in Figure 4. To do a conversion, $\overline{CS}$ must be low to select the device. After $\overline{CS}$ goes low, the RDY output goes low indicating that the device is ready to do a conversion. The conversion starts on the falling edge of $\overline{RD}$. While $\overline{RD}$ is low, the MSB and LSB decisions are made with internally generated clock edges. When the conversion is complete, RDY goes high and $\overline{INT}$ goes low signaling the end of the conversion. After $\overline{INT}$ goes low, the data outputs go from high impedance to active state with valid output data. Data stays valid until either $\overline{RD}$ or $\overline{CS}$ goes high. When either signal goes high, the output data lines return to the high impedance state and $\overline{INT}$ returns high.

1.7.2 WR-RD MODE

In the WR-RD mode, the $\overline{WR}/RDY$ pin is configured as the $\overline{WR}$ input. In this mode, $\overline{WR}$ initiates the conversion and $\overline{RD}$ controls reading the output data. This can be done in several ways, described below.

1.7.3 WR-RD MODE — USING INTERNAL DELAY ($t_{RD} > t_{INTL}$)

The timing is shown in Figure 5. To do a conversion, $\overline{CS}$ must be low to select the device. Then, $\overline{WR}$ falling edge triggers the conversion. While $\overline{WR}$ is low, the MSB comparison is made. When $\overline{WR}$ returns high the LSB decision is made. After some internal delay, $\overline{INT}$ goes low indicating end of conversion. Valid data will appear on DB0–7 when RD is pulled low. $\overline{INT}$ is then reset by the rising edge of either $\overline{CS}$ or $\overline{RD}$.

1.7.4 WR-RD MODE — READING BEFORE DELAY ($t_{RD} < t_{INTL}$)

The internally generated delay for the LSB decision when $t_{RD} > t_{INTL}$ is longer than necessary due to circuit design tolerances of t_{INTL} delay. If desired, a faster conversion will result without loss of accuracy by bringing $\overline{RD}$ low within the minimum time specified for t_{RD}. The timing diagram for this mode is shown in Figure 6. $\overline{WR}$ is the same as when $t_{RD} > t_{INTL}$. But in this case, $\overline{RD}$ is brought low t_{RD} ns after $\overline{WR}$ rising edge and before $\overline{INT}$. $\overline{INT}$ goes low indicating an end of conversion after the falling edge of $\overline{RD}$ and is reset on the rising edge of $\overline{RD}$ or $\overline{CS}$. When $\overline{RD}$ is brought low before $\overline{INT}$ goes low the data bus always remains in the high-impedance state until $\overline{INT}\downarrow$.

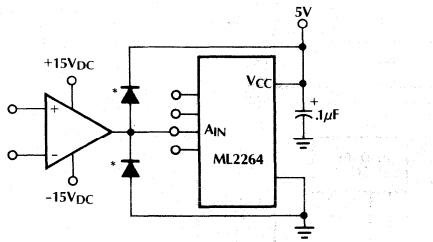
1.7.5 WR-RD MODE — STAND ALONE OPERATION

Stand alone operation can be implemented by tying $\overline{CS}$ and $\overline{RD}$ low as shown in Figure 7. $\overline{WR}$ initiates a conversion as before. When $\overline{WR}$ is low, the MSB comparison is made. When $\overline{WR}$ goes high, the LSB comparison is made. Since $\overline{RD}$ is already low, the output data will appear automatically at end of conversion. Since $\overline{RD}$ is always low, $\overline{INT}$ is reset on rising edge of $\overline{WR}$ and goes low at end of conversion.

1.7.6 POWER-ON RESET

When power is first applied, an internal power-on reset and timer circuit inhibits the $\overline{CS}$ input and resets the internal circuitry to prevent the ML2264 from starting in an unknown state. During this period of approximately 3μs, $\overline{INT}$ remains high and the data bus is in the high-impedance state.

2.0 TYPICAL APPLICATIONS



* NO PROTECTION IS REQUIRED IF INPUT CURRENT > 25mA

Figure 12. Protecting the Input

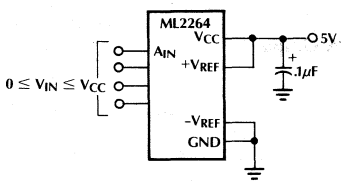


Figure 13. Using V_{CC} as Reference for Ratiometric Operation

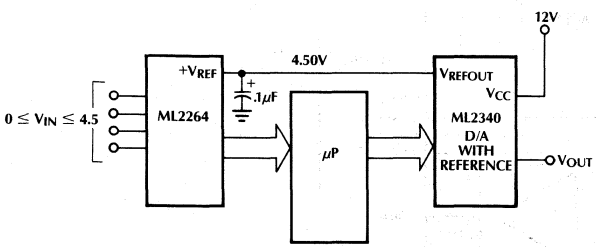


Figure 14. Using External Reference of D/A

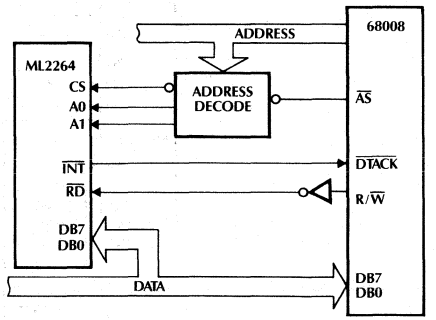


Figure 15. 68000 Type Interface to ML2264

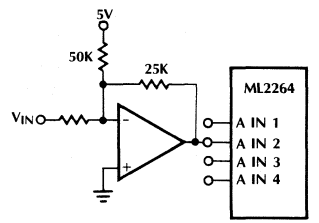


Figure 16. ±2.5V Analog Input Range

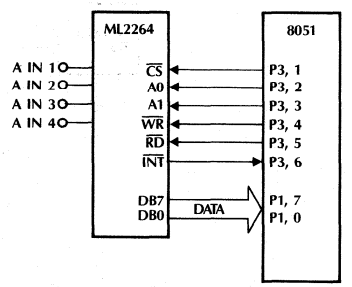


Figure 17. 8051 Interface to ML2264

2.0 TYPICAL APPLICATIONS (Continued)

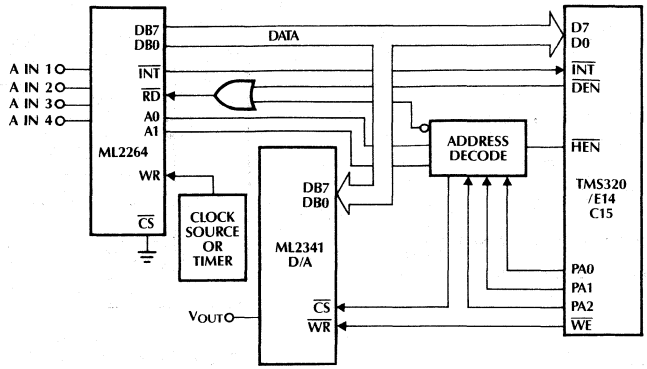


Figure 18. TMS320 Interface with D/A Output

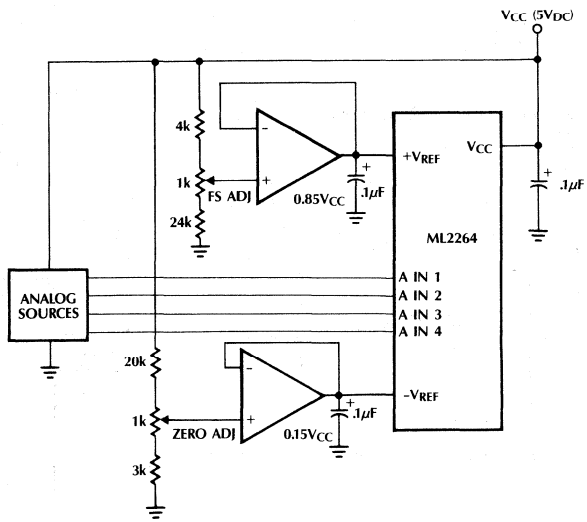


Figure 19. Operating with a Ratiometric Analog Signal of 15% of V_{CC} to 85% of V_{CC}

ORDERING INFORMATION

PART NUMBER	TOTAL UNADJUSTED ERROR	TEMPERATURE RANGE	PACKAGE
ML2264BMJ	±½ LSB	–55°C to +125°C	HERMETIC DIP
ML2264BIJ		–40°C to +85°C	HERMETIC DIP
ML2264BCP		0°C to +70°C	MOLDED DIP
ML2264BCS		0°C to +70°C	MOLDED SOIC
ML2264CMJ	±1 LSB	–55°C to +125°C	HERMETIC DIP
ML2264CIJ		–40°C to +85°C	HERMETIC DIP
ML2264CCP		0°C to +70°C	MOLDED DIP
ML2264CCS		0°C to +70°C	MOLDED SOIC

Micro Linear

ML2271

μP Compatible High-Speed 10-Bit A/D Converter with S/H

GENERAL DESCRIPTION

The ML2271 is a high speed, μP compatible 10-bit A/D converter. A three step flash technique is used to achieve a conversion time of 1.45μs. The ML2271 operates from a single 5V supply and has an analog input range from GND to V_{CC}.

The ML2271 has a true internal sample and hold and can digitize sinusoid signals as high as 150kHz without conversion errors.

The ML2271 digital interface has been designed so that the device appears as a memory location or I/O port to a μP, eliminating the need for external interfacing logic. The data outputs are latched and have three state control, allowing direct connection to a μP bus or I/O port. The addition of an internal timing generator also allows the device to easily operate in stand alone applications.

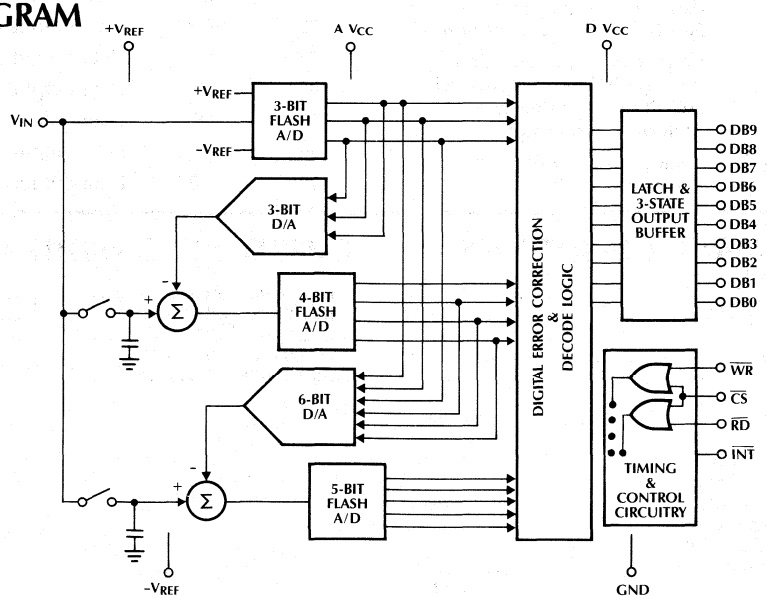
The ML2271 is pin and function compatible with the ADC1061.

FEATURES

- Conversion time over temperature and supply voltage tolerance 1.5μs
- Linearity error ±1/2 LSB or ±1 LSB
- Full scale error ±1/2 LSB or ±1 LSB
- Zero error ±1/2 LSB or ±1 LSB
- Capable of digitizing a 5V, 150kHz sine wave
- No missing codes
- 0V to 5V analog input range with single 5V power supply
- Analog input protection 25mA min
- Operates ratiometrically or with up to 5V voltage reference
- No external clock required
- Easy interface to μP, or operates standalone
- Latched, 3-state data outputs
- Power-on reset circuitry
- Low power 180mW max
- Standard 20-pin DIP or surface mount SOIC
- 0°C to 70°C, –40°C to +85°C, –55°C to +125°C operating temperature range

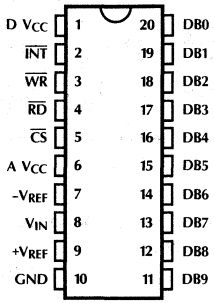
2

BLOCK DIAGRAM



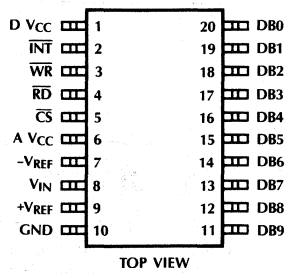
PIN CONNECTIONS

20-Pin DIP



TOP VIEW

20-Pin SOIC



TOP VIEW

PIN DESCRIPTION

PIN NO.	NAME	FUNCTION
1	D V_{CC}	Digital supply. +5V ± 5%. Connect to A V_{CC}.
2	$\overline{INT}$	Interrupt output. This output signals the end of a conversion and indicates that data is valid on the data outputs. See Digital Interface section.
3	$\overline{WR}$	Write input. Input which initiates a conversion. See Digital Interface section.
4	$\overline{RD}$	Read input. This input latches data into the output latches. See Digital Interface section.
5	$\overline{CS}$	Chip select input. This input must be held low during $\overline{WR}$ and $\overline{RD}$ for the device to perform a conversion.
6	A V_{CC}	Analog supply. +5V ± 5%. Connect to D V_{CC}.
7	$-V_{REF}$	Negative reference input voltage for A/D converter.
8	V_{IN}	Analog input.
9	$+V_{REF}$	Positive reference input voltage for A/D converter.
10	GND	Ground.
11	DB9	Data output — bit 9 (MSB).
12	DB8	Data output — bit 8.
13	DB7	Data output — bit 7.
14	DB6	Data output — bit 6.
15	DB5	Data output — bit 5.
16	DB4	Data output — bit 4.
17	DB3	Data output — bit 3.
18	DB2	Data output — bit 2.
19	DB1	Data output — bit 1.
20	DB0	Data output — bit 0 (LSB).

ABSOLUTE MAXIMUM RATINGS
(Note 1)

Supply Voltage, A V_{CC}, D V_{CC} 6.5V
Voltage
  Logic Inputs ..... -0.3V to V_{CC} + 0.3V
  Analog Inputs ..... -0.3V to V_{CC} + 0.3V
Input Current per Pin (Note 2) ..... ±25mA
Storage Temperature ..... -65°C to +150°C
Package Dissipation
  at T_A = 25°C (Board Mount) 875mW
Lead Temperature (Soldering 10 sec.)
  Dual-In-Line Package (Molded) ..... 260°C
  Dual-In-Line Package (Ceramic) ..... 300°C
  Molded Small Outline IC Package
    Vapor Phase (60 sec.) ..... 215°C
    Infrared (15 sec.) ..... 220°C

OPERATING CONDITIONS

Temperature Range (Note 3) ..... $T_{MIN} \leq T_A \leq T_{MAX}$
  ML2271BMJ, ML2271CMJ ..... -55°C to +125°C
  ML2271BIJ, ML2271CIJ ..... -40°C to +85°C
  ML2271BCS, ML2271CCS
  ML2271BCP, ML2271CCP ..... 0°C to +70°C

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, $T_A = T_{MIN}$ to T_{MAX}, D V_{CC} = A V_{CC} = $+V_{REF}$ = 5V ± 5%, and $-V_{REF}$ = GND

PARAMETER	NOTES	CONDITIONS	ML2271XCX			ML2271XIX, ML2271XMX			UNITS
			MIN	TYP (Note 4)	MAX	MIN	TYP (Note 4)	MAX	
Converter									
Intergral Linearity Error ML2271BXX ML2271CXX	5, 7	$V_{REF} = V_{CC}$			 ±1/2 ±1			 ±1/2 ±1	 LSB LSB
Differential Linearity Error ML2271BXX ML2271CXX	5	$V_{REF} = V_{CC}$			 ±1/2 ±1			 ±1/2 ±1	 LSB LSB
Full Scale Error ML2271BXX ML2271CXX	5				 ±1/2 ±1			 ±1/2 ±1	 LSB LSB
Zero Scale Error ML2271BXX ML2271CXX	5				 ±1/2 ±1			 ±1/2 ±1	 LSB LSB
Total Unadjusted Error ML2271BXX ML2271CXX	5				 ±3/4 ±1½			 ±3/4 ±1½	 LSB LSB
$+V_{REF}$ Voltage Range	6		$-V_{REF}$		V_{CC}+0.1	$-V_{REF}$		V_{CC}+0.1	V
$-V_{REF}$ Voltage Range	6		GND–0.1		$+V_{REF}$	GND–0.1		$+V_{REF}$	V
Reference Input Resistance	5		.9	1.3	1.7	.9	1.3	1.7	kΩ
Analog Input Range	5, 8		$-V_{REF}$		$+V_{REF}$	$-V_{REF}$		$+V_{REF}$	V
Power Supply Sensitivity	5	DC V_{CC} = 5V ± 5%, V_{REF} = 4.75V		±1/32	±1/4		±1/32	±1/4	LSB
		100mVp–p 100kHz sine on V_{CC}, V_{IN} = 0		±1/16			±1/16		LSB
Analog Input Leakage Current	5, 9	Converter Idle	–2		+2	–2		+2	µA
Analog Input Capacitance		During Acquisition Period		25			25		pF
Digital and DC									
$V_{IN(1)}$, Logical "1" Input Voltage	5		2.0			2.0			V
$V_{IN(0)}$, Logical "0" Input Voltage	5				0.8			0.8	V
$I_{IN(1)}$, Logical "1" Input Current	5	$V_{IN} = V_{CC}$			1			1	µA
$I_{IN(0)}$, Logical "0" Input Current	5	V_{IN} = 0V	–1			–1			µA
$V_{OUT(1)}$, Logical "1" Output Voltage	5	I_{OUT} = –2mA	4.0			4.0			V
$V_{OUT(0)}$, Logical "0" Output Voltage	5	I_{OUT} = 2mA			0.4			0.4	V
I_{OUT}, Three-State Output Current	5	V_{OUT} = 0V	–1			–1			µA
		$V_{OUT} = V_{CC}$			1			1	µA

2

ELECTRICAL CHARACTERISTICS (Continued)

Unless otherwise specified, $T_A = T_{MIN}$ to T_{MAX}, D V_{CC} = A V_{CC} = $+V_{REF}$ = 5V ± 5%, $-V_{REF}$ = GND, and timing measured at 1.4V, C_L = 100pF.

PARAMETER	NOTES	CONDITIONS	ML2271XCX			ML2271XIX, ML2271XMX			UNITS
			MIN	TYP (Note 4)	MAX	MIN	TYP (Note 4)	MAX	
Digital and DC (Continued)									
C_{OUT}, Logic Output Capacitance				5			5		pF
C_{IN}, Logic Input Capacitance				5			5		pF
I_{CC}, Supply Current, Analog Plus Digital	5	$\overline{CS}$ = $\overline{WR}$ = $\overline{RD}$ = 0 No Output Load			32			35	mA
AC and Dynamic Performance (Note 9)									
t_{CONV}, Conversion Time, Interrupt Mode	6	Figure 2			1450			1600	ns
t_{CONV}, Conversion Time, Write-Read Mode	5	Figure 3			1450			1600	ns
t_{CONV}, Conversion Time, Read Mode	6	Figure 4			1450			1600	ns
SNR, Signal to Noise Ratio		V_{IN} = 5V, 150kHz Noise is sum of all nonfundamental components from 0–300kHz. $f_{SAMPLING}$ = 600kHz		60			60		dB
HD, Harmonic Distortion		V_{IN} = 5V, 150kHz THD is sum of 2–5th harmonics or aliases relative to fundamental. $f_{SAMPLING}$ = 600kHz		–60			–60		dB
IMD, Intermodulation Distortion		fa = 2.5V, 150kHz fb = 2.5V, 148kHz IMB is (fa + fb), (fa – fb), (2fa + fb), (2fa – fb), (fa + 2fb), or (fa – 2fb) relative to fundamental. $f_{SAMPLING}$ = 600kHz		–60			–60		dB
FR, Freqency Response		V_{IN} = 5V, 0–150kHz Relative to 1kHz $f_{SAMPLING}$ = 600kHz		±0.1			±0.1		dB
SR, Slew Rate Tracking				2.36			2.36		V/μs
AC Performance, Figures 2, 3, 4, and 5									
t_{CSS}, $\overline{CS}$ to $\overline{RD}$, $\overline{WR}$ Setup Time	5		0			0			ns
t_{CSH}, $\overline{CS}$ to $\overline{RD}$, $\overline{WR}$ Hold Time	5		0			0			ns
t_{WR}, $\overline{WR}$ Pulse Width	5		250		50K	300		50K	ns

ELECTRICAL CHARACTERISTICS (Continued)

Unless otherwise specified, $T_A = T_{MIN}$ to T_{MAX}, D V_{CC} = A V_{CC} = $+V_{REF}$ = 5V ± 5%, and $-V_{REF}$ = GND, and timing measured at 1.4V, C_L = 100 pF.

PARAMETER	NOTES	CONDITIONS	ML2271XCX			ML2271XIX, ML2271XMX			UNITS
			MIN	TYP (Note 4)	MAX	MIN	TYP (Note 4)	MAX	
AC Performance, Figures 2, 3, 4, and 5 (Continued)									
t_{ACC2}, $\overline{WR}$ to Data Valid	5				1500			1600	ns
t_{RD}, Read Pulse Width	5		100			120			ns
t_{WRL}, $\overline{WR}$↑ to $\overline{RD}$↓	6		0			0			ns
t_{INTH}, $\overline{RD}$↑ to $\overline{INT}$↑	5		10		50	10		50	ns
t_{RIL}, $\overline{RD}$ to $\overline{INT}$↓	5		0		50	0		50	ns
t_{ACC1}, Data Access Time, $\overline{RD}$↓ to Data Valid	5		0		55	0		60	ns
t_{ID}, Data Access Time, $\overline{INT}$↓ to Data Valid	5		0		55	0		60	ns
t_{1H}, t_{0H}, $\overline{RD}$↑ to Data High Impedance State	5	Figure 1	10		50	10		60	ns
t_P, Delay Time Between Conversions	5		300			300			ns

Note 1: Absolute maximum ratings are limits beyond which the life of the integrated circuit may be impaired. All voltages unless otherwise specified are measured with respect to ground.

Note 2: When the voltage at any pin exceeds the power supply rails (V_{IN} < GND or V_{IN} > V_{CC}) the absolute value of current at that pin should be limited to 25mA or less.

Note 3: –55°C to +125°C operating temperature range devices are 100% tested at temperature extremes with worst-case test conditions. 0°C to +70°C and –40°C to +85°C operating temperature range devices are 100% tested with temperature limits guaranteed by 100% testing, sampling, or by correlation with worst-case test conditions.

Note 4: Typicals are parametric norm at 25°C.

Note 5: Parameter guaranteed and 100% production tested.

Note 6: Parameter guaranteed. Parameters not 100% tested are not in outgoing quality level calculation.

Note 7: Total unadjusted error includes offset, full scale, linearity, and sample and hold errors.

Note 8: For $-V_{REF} \geq V_{IN}$ the digital output code will be 0000 0000. Two on-chip diodes are tied to the analog input which will forward conduct for analog input voltages one diode drop below ground or one diode drop greater than the V_{CC} supply. Be careful, during testing at low V_{CC} levels (4.5V), as high level analog inputs (5V) can cause this input diode to conduct — especially at elevated temperatures, and cause errors for analog inputs near full scale. The spec allows 100mV forward bias of either diode. This means that as long as the analog V_{IN} or V_{REF} does not exceed the supply voltage by more than 100mV, the output code will be correct. To achieve an absolute $0V_{DC}$ to $5V_{DC}$ input voltage range will therefore require a minimum supply voltage of $4.900V_{DC}$ over temperature variations, initial tolerance and loading.

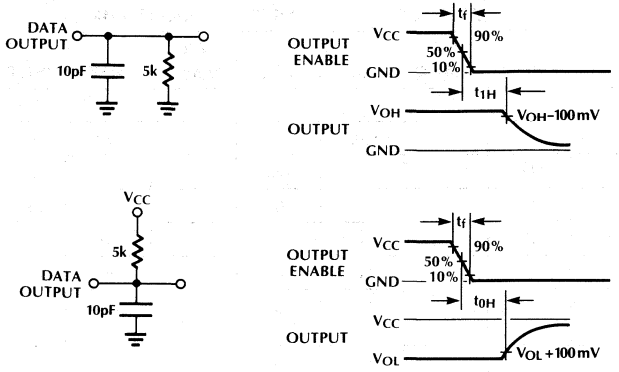


Figure 1. High Impedance Test Circuits and Waveforms

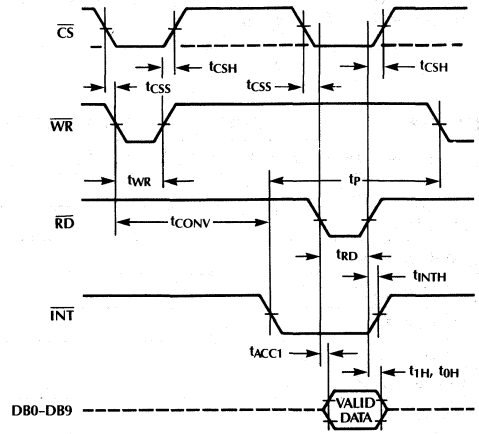


Figure 2. Interrupt Mode Timing

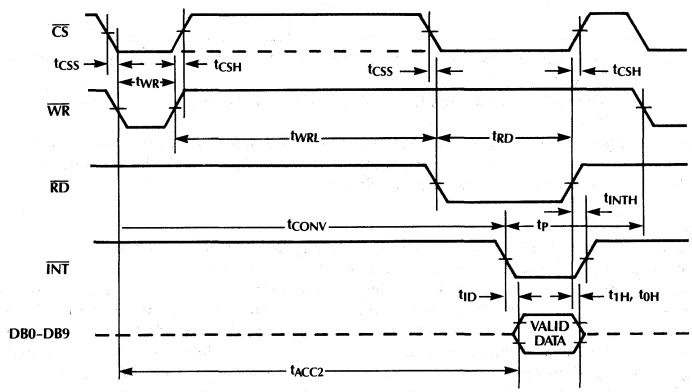
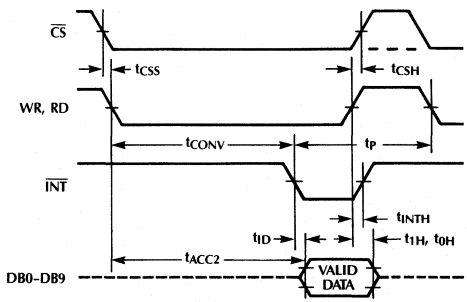


Figure 3. WR-RD Mode Timing



READ IS TIED TO WRITE

Figure 4. RD Mode Timing

1.0 FUNCTIONAL DESCRIPTION

The ML2271 uses a three step flash technique for A/D conversion. This technique first performs a 3 bit flash conversion on V_{IN} to determine the 3 most significant bits (MSB decision). These 3 MSB's are then cycled through an internal DAC to recreate the analog input. This reconstructed analog input signal from the DAC is then subtracted from the input, and the difference voltage is converted by a second 3 bit flash conversion providing the next 3 significant bits, called intermediate significant bits (ISB decision). This procedure is then performed again to provide the final 4 least significant bits (LSB decision).

The ML2271 has a true internal sample and hold. The internal operating sequence is shown in Figure 5. The falling edge of $\overline{WR}$ opens the S/H sampling switch, ends the acquisition time for the analog input, and starts the conversion on the internally sample and held signal. Then the MSB, ISB, and LSB decisions are made. $\overline{INT}$ goes low at end of conversion and RD controls the data outputs. This falling edge of $\overline{INT}$ also closes the sampling switch and starts the acquisition period for the next conversion.

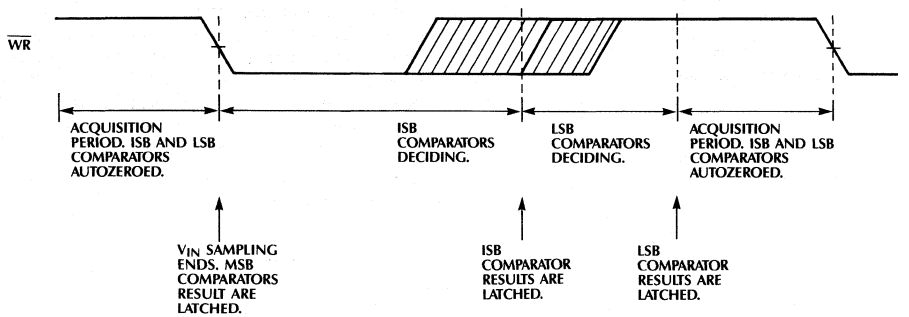


Figure 5. Operating Sequence

1.1 ANALOG INPUT

The analog input on the ML2271 behaves differently than inputs on conventional converters. The analog input current requirements change while the conversion is in progress, and the amount of input current depends on what cycle the converter is in.

The input circuit for the converter is shown in Figure 6A with the equivalent input circuit shown in Figure 6B. The acquisition period for the S/H starts on $\overline{INT}$ falling edge and ends on $\overline{WR}$ falling edge.

The critical period for charging up the analog input occurs during the acquisition period and the source of the external signal on V_{IN} must adequately charge up the analog voltage during this time. To do this, the input must settle within the required analog accuracy tolerance 100ns before the end of the acquisition period so that the sampling capacitors have adequate time to store the input signal. If more time is needed due to finite charging or settling time of the external source, the $\overline{WR}$ high period can be extended as long as is required.

1.2 SAMPLE AND HOLD

The ML2271 does not have the limitation of an equivalent circuit implemented with a track/hold. An internal sample and hold acquires the analog signal, holds it internally, and then a conversion is performed on the sample and held signal. Since this is a true sample and hold function, the ML2271 can sample and hold signals with frequencies as high as 150kHz @ 5V (slew rates as high as 2.36V/μs) without sacrificing conversion accuracy.

1.3 REFERENCE

The $+V_{REF}$ and $-V_{REF}$ inputs are the reference voltages that determine the full scale and zero input voltages, respectively, for the A/D converter. Thus, $+V_{REF}$ defines the analog input which produces a full scale output and $-V_{REF}$ defines the analog input which produces an output code of all zeroes. The transfer function for the A/D converter is shown in Figure 7.

$+V_{REF}$ and $-V_{REF}$ can be set to any voltage between GND and V_{CC}. This means that the reference voltages can be offset from GND and the difference between $+V_{REF}$ and $-V_{REF}$ can be made small to increase the resolution of the conversion. Note that the linearity error increases when $[+V_{REF} - (-V_{REF})]$ decreases.

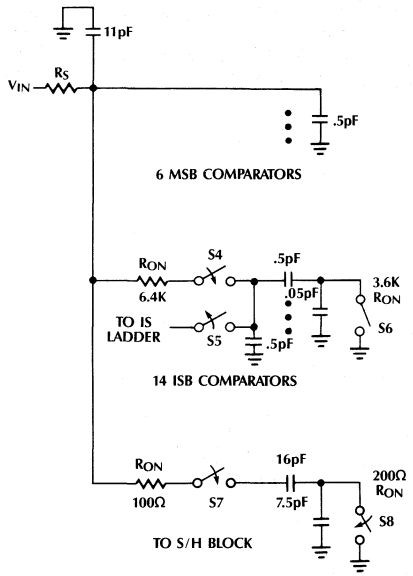


Figure 6A. Converter Input Circuit

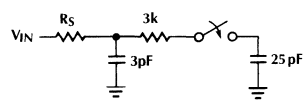


Figure 6B. Converter Equivalent Input Circuit

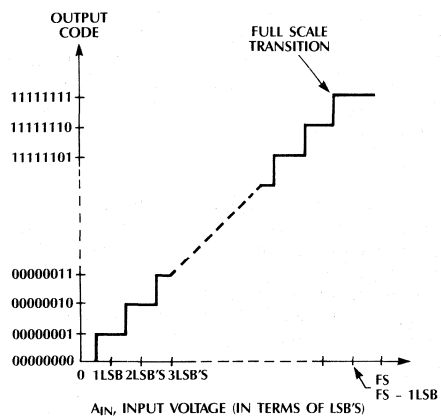


Figure 7. A/D Transfer Characteristic

1.4 POWER SUPPLY AND REFERENCE DECOUPLING

0.1μF in parallel with 0.01μF ceramic disc capacitors are recommended to bypass A V_{CC} to GND, as well as D V_{CC} to GND, using the shortest lead lengths possible.

If $+V_{REF}$ and $-V_{REF}$ inputs are driven by long lines, they should be bypassed by 0.1μF in parallel with 0.01μF ceramic disc capacitors at the reference input pins.

1.5 DYNAMIC PERFORMANCE

1.5.1 SINUSOIDAL INPUTS

Since the ML2271 has an internal sample and hold, the device can digitize high frequency sinusoids with little or no signal degradations. Using the Nyquist criteria, the highest frequency input to the converter could theoretically be 1/2 the sampling rate (f_S). Any frequency components above $f_S/2$ will be aliased below $f_S/2$. In most applications, these aliased components cause unacceptable distortion and must be filtered out of the input. If the input frequency is too close to $f_S/2$, then the requirements on the antialias filter become difficult or impossible to realize with standard component and tolerances. In most practical applications, the highest input frequency has to be limited to 1/3 to 1/4 of f_S in order to relax the filtering requirements enough to make a realizeable antialias filter.

The maximum sampling rate (f_{MAX}) for the ML2271 can be calculated as follows:

$$f_{max} = \frac{1}{t_{CONV} + t_P}$$

$$f_{max} = \frac{1}{1.45\mu s + 0.300\mu s}$$

f_{max} = 570kHz

t_{WR} = Write Pulse Width

t_{WRD} = Write to Data Delay

t_P = Delay Time between Conversions

Note that the dynamic performance specifications (SNR, HD, IMD, and FR) for the ML2271 are all specified at 150kHz, which is less than 1/3 of the sampling rate, f_S. This allows adequate margin between the input frequency and the aliased components to allow antialias filtering if needed.

In applications where aliased frequency components are acceptable and filtering of the input signal is not needed, the user can apply an input sinusoid higher than 150kHz to the device. Note, however, that as the input frequency increases above 150kHz, dynamic performance degradation will occur due to the finite bandwidth of the internal sample and hold.

1.5.2 SIGNAL-TO-NOISE RATIO

Signal-to-noise ratio (SNR) is the measured signal to noise at the output of the converter. The signal is the rms magnitude of the fundamental. Noise is the rms sum of all the nonfundamental signals up to half the sampling frequency. SNR is dependent on the number of quantization levels used in the digitization process; the more the levels, the smaller the quantization noise. The theoretical SNR for a sine wave is given by

$$SNR = (6.02N + 1.76)\ dB$$

where N is the number of bits. Thus for ideal 10-bit converter, SNR = 61.96 dB.

1.5.3 HARMONIC DISTORTION

Harmonic distortion is the ratio of the rms sum of harmonics to the fundamental. Total harmonic distortion (THD) of the ML2271 is defined as

$$20 \log = \frac{(V_2^2 + V_3^2 + V_4^2 + V_5^2)^{1/2}}{V_1}$$

where V_1 is the rms amplitude of the fundamental and V_2, V_3, V_4, V_5 are the rms amplitudes of the individual harmonics.

1.5.4 INTERMODULATION DISTORTION

With inputs consisting of sine waves at two frequencies, f_A and f_B, any active device with nonlinearities will create distortion products, of order (m + n), at sum and difference frequencies of $mf_A + nf_B$, where m, n = 0, 1, 2, 3 . . . Intermodulation terms are those for which m or n is not equal to zero. The (IMD) intermodulation distortion specification includes the second order terms ($f_A + f_B$) and ($f_A - f_B$) and the third order terms ($2f_A + f_B$), ($2f_A - f_B$), ($f_A + 2f_B$), and ($f_A - 2f_B$) only.

1.6 DIGITAL INTERFACE

Depending on the way the external signals are applied to the ML2271, the timing of the conversion and resultant digital interface can be configured in three different modes.

While the operation for each mode is described below, there are some general rules that dictate the general relationships between CS, WR, RD, INT, and DB0–DB9. The falling edge of WR terminates the acquisition period and initiates a conversion. INT is forced low when a conversion is internally completed. INT is reset high by the RD rising edge. DB0–DB9 is in the high impedance state except when both RD and INT are low. RD low period does not affect the internal conversion but only determines when the digital signals DB0–DB9 are active; thus, RD can occur anytime. CS is used to select the device and needs to be low only while WR is low or when RD is low.

1.6.1 INTERRUPT MODE

Timing for the Interrupt Mode is shown in Figure 2. To do a conversion, CS must be low to select the device. INT falling edge starts the acquisition period. The falling edge of WR ends the acquisition period and the MSB comparison is made. Then, the (Intermediate Significant Bits) ISB and LSB decisions are made with internal timing signals. After the conversion is complete, INT goes low indicating end of conversion. When RD goes low, DB0–DB9 goes from high impedance to the active state with the digital result of the conversion. INT is reset high and DB0–DB9 is reset to high impedance on the rising edge of RD.

Interrupt Operation is intended to be used in interrupt driven systems or applications where INT signals the transfer of data.

1.6.2 WRITE-READ MODE

Write-Read Operation is the same as Interrupt Operation except that RD is brought low before the internal conversion is completed (before INT goes low).

Timing for Write-Read Operation is shown in Figure 3. To perform a conversion, CS must be low to select the device. INT falling edge starts the acquisition period. The falling edge of WR ends the acquisition period and the MSB decision is made. Then, the ISB and LSB decisions are made by internal timing signals. In this mode, RD is brought low before the internal conversion is completed. When the internal conversion is completed, INT will be forced low and data will appear on DB0–DB9 as long as RD is still low. INT is reset high and DB0–DB9 is reset to high impedance on the rising edge of RD.

Write-Read Operation is intended for applications where RD controls the transfer of data to a microprocessor.

1.6.3 READ MODE

Read Mode Operation is implemented by tying RD to WR and keeping RD and WR low long enough so that the conversion time is totally determined by the internal timing signals.

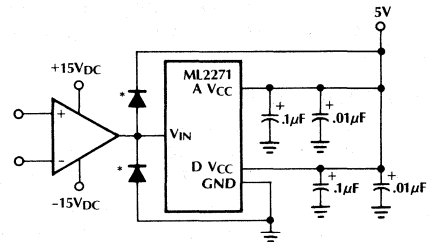
Timing for the Read Mode is shown in Figure 4. To do a conversion, CS must be low to select the device. The RD and WR falling edge starts the conversion. RD and WR is held low for the entire internal conversion. Thus, the MSB, ISB, and LSB comparisons along with the end of the acquisition period are made by internally generated timing signals. After the conversion is complete, INT goes low. Since RD is fixed low, DB0–DB9 will go from high impedance to active state as soon as INT goes low. INT is reset high and DB0–DB9 is reset to high impedance on rising edge of WR and RD.

Read Mode Operation allows a conversion to be done with the device's own internal timing and thus, no external timing is needed.

1.6.4 POWER-ON RESET

When power is first applied, an internal power-on reset and timer circuit inhibits the $\overline{CS}$ input and resets the internal circuitry to prevent the ML2271 from starting in an unknown state. During this period of approximately 50μs, $\overline{INT}$ remains high and the data bus is in the high-impedance state.

2.0 TYPICAL APPLICATIONS



PROTECTION IS REQUIRED IF INPUT CURRENT > 25mA

Figure 8. Protecting the Input

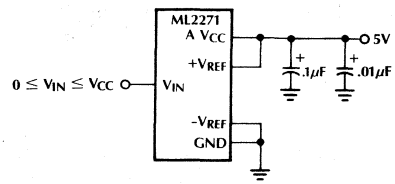


Figure 9. Using V_{CC} as Reference for Ratiometric Operation

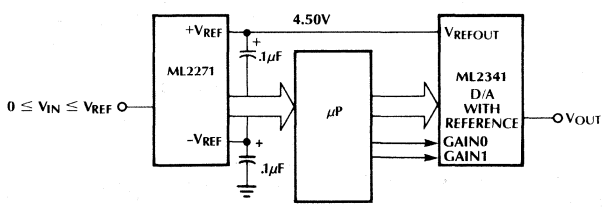


Figure 10. Using External Reference of D/A

2.0 TYPICAL APPLICATIONS (Continued)

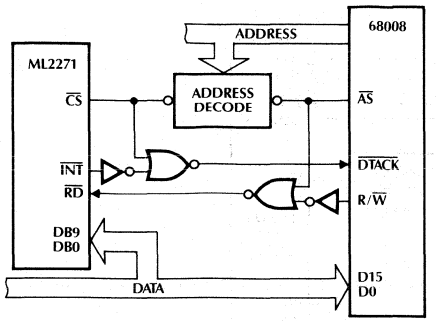


Figure 11. 68000 Type Interface to ML2271

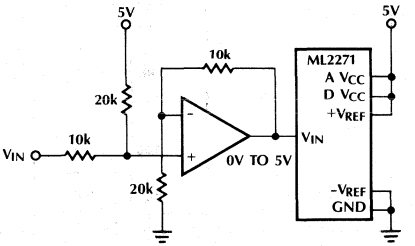


Figure 12. ±2.5V Analog Input Range

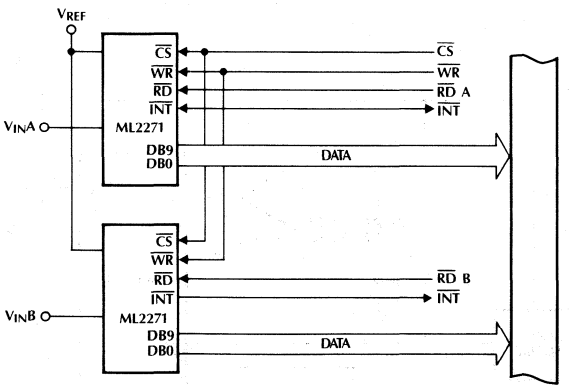


Figure 13. Simultaneous Sampling of Two Variables

2.0 TYPICAL APPLICATIONS (Continued)

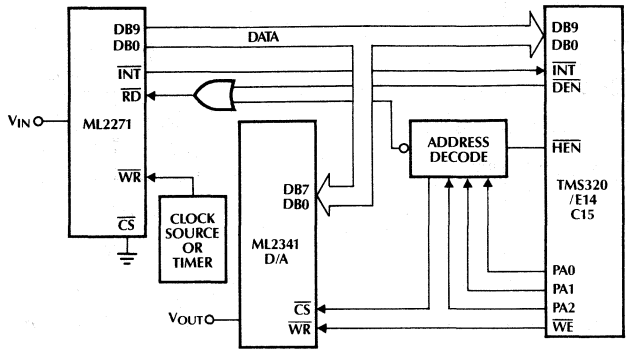


Figure 14. TMS320 Interface with D/A Output

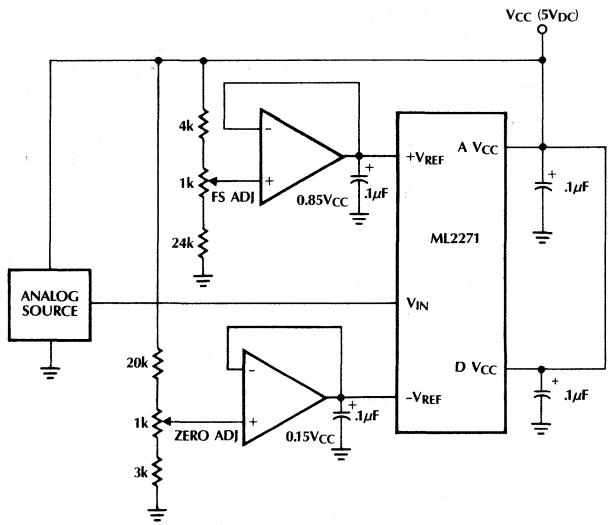


Figure 15. Operating with a Ratiometric Analog Signal of 15% of V_{CC} to 85% of V_{CC}

ORDERING INFORMATION

PART NUMBER	LINEARITY ERROR	TEMPERATURE RANGE	PACKAGE
ML2271BMJ	±½ LSB	–55°C to +125°C	HERMETIC DIP
ML2271BIJ		–40°C to +85°C	HERMETIC DIP
ML2271BCP		0°C to +70°C	MOLDED DIP
ML2271BCS		0°C to +70°C	MOLDED SOIC
ML2271CMJ	±1 LSB	–55°C to +125°C	HERMETIC DIP
ML2271CIJ		–40°C to +85°C	HERMETIC DIP
ML2271CCP		0°C to +70°C	MOLDED DIP
ML2271CCS		0°C to +70°C	MOLDED SOIC

ML2280, ML2283

Serial I/O 8-Bit A/D Converters

GENERAL DESCRIPTION

The ML2280 and ML2283 are 8-bit successive approximation A/D converters with serial I/O and configurable input multiplexers with up to 4 input channels.

All errors of the sample-and-hold incorporated on the ML2280 and ML2283, are accounted for in the analog-to-digital converters accuracy specification.

The voltage reference can be externally set to any value between GND and V_{CC}, thus allowing a full conversion over a relatively small voltage span if desired.

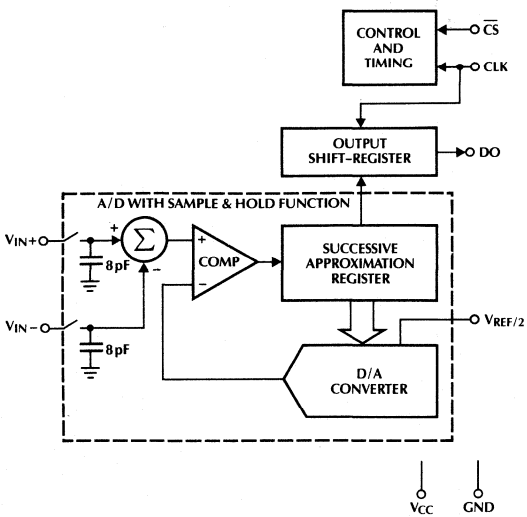
The ML2283 is an enhanced double polysilicon CMOS pin compatible second source for the ADC0833 A/D converter. All parameters are guaranteed over temperature with a power supply voltage of 5V ±10%.

FEATURES

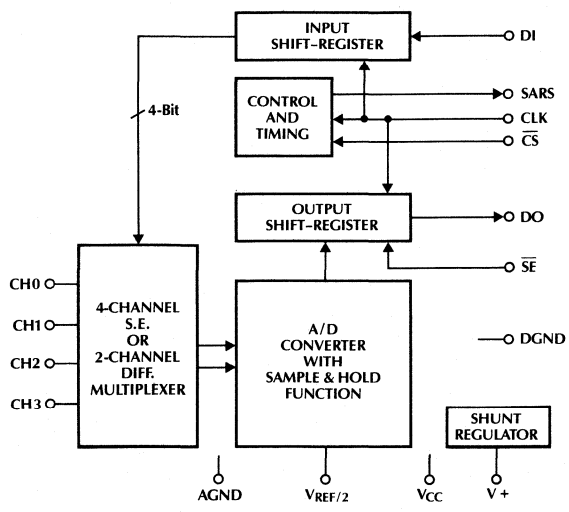
- Conversion time 6μs
- ML2280 capable of digitizing a 5V, 40kHz sine wave
- Total unadjusted error with external reference ±½LSB or ±1LSB
- Sample-and-hold 375ns acquisition
- 0 to 5V analog input range with single 5V power supply
- 2.5V reference provides 0 to 5V analog input range
- No zero or full-scale adjust required
- Low power 12.5mW MAX
- Analog input protection 25mA (min) per input
- Differential analog voltage inputs
- 0.3″ width 8- or 14-pin DIP
- 4-channel input MUX option
- Superior pin compatible replacement for ADC0833

BLOCK DIAGRAMS

ML2280



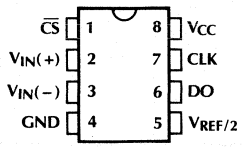
ML2283



PIN CONNECTIONS

ML2280 Single Differential Input

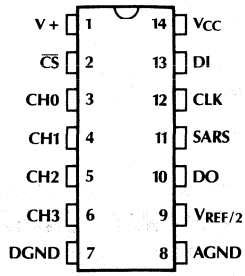
8-PIN DIP



TOP VIEW

ML2283 4-Channel MUX

14-PIN DIP



TOP VIEW

2

PIN DESCRIPTION

NAME	FUNCTION
V_{CC}	Positive supply. 5 volts ± 10%
DGND	Digital ground. 0 volts. All digital inputs and outputs are referenced to this point.
AGND	Analog ground. The negative reference voltage for A/D converter.
GND	Combined analog and digital ground.
CH0, $V_{IN}+$, $V_{IN}-$	Analog inputs. Digitally selected to be single ended (V_{IN}) or; $V_{IN}+$ or $V_{IN}-$ of a differential input. Analog range = GND ≤ V_{IN} ≤ V_{CC}
$V_{REF/2}$	Reference. The analog input range is twice the positive reference voltage value applied to this pin.
V+	Input to the Shunt Regulator.
DO	Data out. Digital output which contains result of A/D conversion. The serial data is clocked out on falling edges of CLK.

NAME	FUNCTION
SARS	Successive approximation register status. Digital output which indicates that a conversion is in progress. When SARS goes to 1, the sampling window is closed and conversion begins. When SARS goes to 0, conversion is completed. When $\overline{CS}$ = 1, SARS is in high impedance state.
CLK	Clock. Digital input which clocks data in on DI on rising edges and out on DO on falling edges. Also used to generate clocks for A/D conversion.
DI	Data input. Digital input which contains serial data to program the MUX and channel assignments.
$\overline{CS}$	Chip select. Selects the chip for multiplexer and channel assignment and A/D converison. When $\overline{CS}$ = 1, all digital outputs are in high impedance state. When $\overline{CS}$ = 0, normal A/D conversion takes place.

ABSOLUTE MAXIMUM RATINGS

(Note 1)

Current into V+ 15mA
Supply Voltage, V_{CC} 6.5V
Voltage
  Logic Inputs ..... $-7V$ to V_{CC} $+7V$
  Analog Inputs ..... $-0.3V$ to V_{CC} $+0.3V$
Input Current per Pin (Note 2) ..... $\pm 25mA$
Storage Temperature ..... $-65°C$ to $+150°C$
Package Dissipation
  at $T_A = 25°C$ (Board Mount) 800mW
Lead Temperature (Soldering 10 sec.)
  Dual-In-Line Package (Molded) ..... 260°C
  Dual-In-Line Package (Ceramic) ..... 300°C

OPERATING CONDITIONS

Supply Voltage, V_{CC} ..... $4.5V_{DC}$ to $6.3V_{DC}$
Temperature Range (Note 3) ..... $T_{MIN} \leq T_A \leq T_{MAX}$
  ML2280BMJ, ML2283BMJ ..... $-55°C$ to $+125°C$
  ML2280BIJ, ML2283BIJ ..... $-40°C$ to $+85°C$
  ML2280CIJ, ML2283CIJ
  ML2280BCP, ML2283BCP ..... 0°C to +70°C
  ML2280CCP, ML2283CCP

ELECTRICAL CHARACTERISTICS

Unless otherwise specified $T_A = T_{MIN}$ to T_{MAX}, $V_{CC} = 5V \pm 10\%$, $f_{CLK} = 1.333MHz$, and $V_{REF/2} = 2.5V$.

PARAMETER	NOTES	CONDITIONS	ML2280B, ML2283B			ML2280C, ML2283C			UNITS
			MIN	TYP NOTE 4	MAX	MIN	TYP NOTE 4	MAX	
CONVERTER AND MULTIPLEXER CHARACTERISTICS									
Total Unadjusted Error	5, 7	$V_{REF/2} = 2.5V$ $V_{REF/2}$ not Connected			$\pm 1/2$ ± 2			± 1 ± 2	LSB LSB
Reference Input Resistance, $V_{REF/2}$	5		3	5	7.5	3	5	7.5	kΩ
Common-Mode Input Range	5,8		GND -0.05		V_{CC} $+0.05$	GND -0.05		V_{CC} $+0.05$	V
DC Common-Mode Error	6	Common Mode Voltage GND to $V_{CC/2}$		$\pm 1/16$	$\pm 1/4$		$\pm 1/16$	$\pm 1/4$	LSB
AC Common-Mode Error	6	Comon Mode Voltage GND to V_{CC}, 0 to 50kHz			$\pm 1/4$			$\pm 1/4$	LSB
DC Power Supply Sensitivity	6	$V_{CC} = 5V \pm 10\%$ $V_{REF} \leq V_{CC} + 0.1V$		$\pm 1/32$	$\pm 1/4$		$\pm 1/32$	$\pm 1/4$	LSB
AC Power Supply Sensitivity	6	$100mV_{P-P}$, 25kHz Sine on V_{CC}			$\pm 1/4$			$\pm 1/4$	LSB
Change in Zero Error from $V_{CC} = 5V$ to Internal Zener Operation	6	15mA into V+ V_{CC} = N.C. $V_{REF/2} = 2.5V$		$\pm 1/2$			$\pm 1/2$		LSB
V_Z, Internal Diode Regulated Breakdown (at V+)		15mA into V+		6.9			6.9		V
V+ Input Resistance	5		20	35		20	35		kΩ
I_{Off}, Off Channel Leakage Current	5, 9	On Channel = V_{CC} Off Channel = 0V	-1			-1			μA
		On Channel = 0V Off Channel = V_{CC}			+1			+1	μA
I_{On}, On Channel Leakage Current	5, 9	On Channel = 0V Off Channel = V_{CC}	-1			-1			μA
		On Channel = V_{CC} Off Channel = 0V			+1			+1	μA

ELECTRICAL CHARACTERISTICS (Continued)

Unless otherwise specified $T_A = T_{MIN}$ to T_{MAX}, $V_{CC} = 5V \pm 10\%$, $f_{CLK} = 1.333MHz$, and $V_{REF/2} = 2.5V$.

PARAMETER	NOTES	CONDITIONS	MIN	TYP NOTE 4	MAX	LIMIT UNITS
DIGITAL AND DC CHARACTERISTICS						
$V_{IN(1)}$, Logical "1" Input Voltage	5		2.0			V
$V_{IN(0)}$, Logical "0" Input Voltage	5				0.8	V
$I_{IN(1)}$, Logical "1" Input Current	5	$V_{IN} = V_{CC}$			1	μA
$I_{IN(0)}$, Logical "0" Input Current	5	$V_{IN} = 0V$	−1			μA
$V_{OUT(1)}$, Logical "1" Output Voltage	5	$I_{OUT} = -2mA$	4.0			V
$V_{OUT(0)}$, Logical "0" Output Voltage	5	$I_{OUT} = 2mA$			0.4	V
I_{OUT}, Hi-Z Output Current	5	$V_{OUT} = 0V$ $V_{OUT} = V_{CC}$	−1		 1	μA μA
I_{SOURCE}, Output Source Current	5	$V_{OUT} = 0V$	−6.5			mA
I_{SINK}, Output Sink Current	5	$V_{OUT} = V_{CC}$			8.0	mA
I_{CC}, Supply Current	5			1.3	2.5	mA
AC ELECTRICAL CHARACTERISTICS						
f_{CLK}, Clock Frequency	5		10		1333	kHz
t_{ACQ}, Sample-and-Hold Acquistion				1/2		$1/f_{CLK}$
t_C, Conversion Time		Not including MUX Addressing Time		8		$1/f_{CLK}$
SNR, Signal to Noise Ratio ML2280	12	$V_{IN} = 40kHz$, 5V Sine. $f_{CLK} = 1.333MHz$ ($f_{SAMPLING} \cong 120kHz$). Noise is Sum of All Nonfundamental Components up to 1/2 of $f_{SAMPLING}$		47		dB
THD, Total Harmonic Distortion ML2280	12	$V_{IN} = 40kHz$, 5V Sine. $f_{CLK} = 1.333MHz$ ($f_{SAMPLING} \cong 120kHz$). THD is Sum of 2, 3, 4, 5 Harmonics Relative to Fundamental		−60		dB
IMD, Intermodulation Distortion ML2280	12	$V_{IN} = f_A + f_B$. $f_A = 40kHz$, 2.5V Sine. $f_B = 39.8kHz$, 2.5V Sine, $f_{CLK} = 1.333MHz$ ($f_{SAMPLING} \cong 120kHz$). IMD is $(f_A + f_B)$, $(f_A - f_B)$, $(2f_A + f_B)$, $(2f_A - f_B)$, $(f_A + 2f_B)$, $(f_A - 2f_B)$ Relative to Fundamental		−60		dB
Clock Duty Cycle	5, 10		40		60	%
t_{SET-UP} CS Falling Edge or Data Input Valid to CLK Rising Edge	5		130			ns
t_{HOLD}, Data Input Valid after CLK Rising Edge	5		80			ns

ELECTRICAL CHARACTERISTICS (Continued)

Unless otherwise specified $T_A = T_{MIN}$ to T_{MAX}, $V_{CC} = 5V \pm 10\%$, $f_{CLK} = 1.333\,MHz$, and $V_{REF/2} = 2.5V$

PARAMETER	NOTES	CONDITIONS	MIN	TYP NOTE 4	MAX	LIMIT UNITS
AC ELECTRICAL CHARACTERISTICS						
t_{pd1}, t_{pd0} — CLK Falling Edge to Output Data Valid	5, 11	$C_L = 100\,pF$ Data MSB First Data LSB First		 90 50	 200 110	 ns ns
t_{1H}, t_{0H}, — Rising Edge of CS to Data Output and SARS Hi-Z	6	$C_L = 10\,pF$, $R_L = 10k$ (see High Impedance Test Circuits)		40	90	ns
	6	$C_L = 100\,pF$, $R_L = 2k$		80	160	ns
C_{IN}, Capacitance of Logic Input				5		pF
C_{OUT}, Capacitance of Logic Outputs				5		pF

Note 1: Absolute maximum ratings are limits beyond which the life of the integrated circuit may be impaired. All voltages unless otherwise specified are measured with respect to ground.

Note 2: When the input voltage (V_{IN}) at any pin exceeds the power supply rails ($V_{IN} < GND$ or $V_{IN} > V_{CC}$) the absolute value of current at that pin should be limited to 25 mA or less.

Note 3: −55°C to +125°C operating temperature range devices are 100% tested at temperature extremes with worst-case test conditions. 0°C to 70°C and −40°C to +85°C operating temperature range devices are 100% tested with temperature limits guaranteed by 100% testing, sampling, or by correlation with worst-case test conditions.

Note 4: Typicals are parametric norm at 25°C.

Note 5: Parameter guaranteed and 100% production tested.

Note 6: Parameter guaranteed. Parameters not 100% tested are not in outgoing quality level calculation.

Note 7: Total unadjusted error includes offset, full-scale, linearity, multiplexer and sample-and-hold errors.

Note 8: For $V_{IN}(-) \geq V_{IN}(+)$ the digital output code will be 0000 0000. Two on-chip diodes are tied to each analog input (See Block Diagram) which will forward conduct for analog input voltages one diode drop below ground or one diode drop greater then the V_{CC} supply. Be careful, during testing at low V_{CC} levels (4.5 V), as high level analog inputs (5 V) can cause this input diode to conduct-especially at elevated temperatures, and cause errors for analog inputs near full-scale. The spec allows 50 mV forward bias of either diode. This means that as long as the analog V_{IN} or V_{REF} does not exceed the supply voltage by more than 50 mV, the output code will be correct. To achieve an absolute 0 V to 5 V input voltage range will therefore require a minimum supply voltage of 4.950 V_{DC} over temperature variations, initial tolerance and loading.

Note 9: Leakage current is measured with the clock not switching.

Note 10: A 40% to 60% clock duty cycle range insures proper operation at all clock frequencies. In the case that an available clock has a duty cycle outside of these limits, the minimum, time the clock is high or the minimum time the clock is low must be at least 300 ns. The maximum time the clock can be high or low is 60 μs.

Note 11: Since data, MSB first, is the output of the comparator used in the successive approximation loop, an additional delay is built in (See Block Diagram) to allow for comparator response time.

Note 12: Because of multiplexer addressing, test conditions for the ML2283 is $V_{IN} = 30\,kHz$, 5 V sine ($f_{SAMPLING} \approx 89\,kHz$).

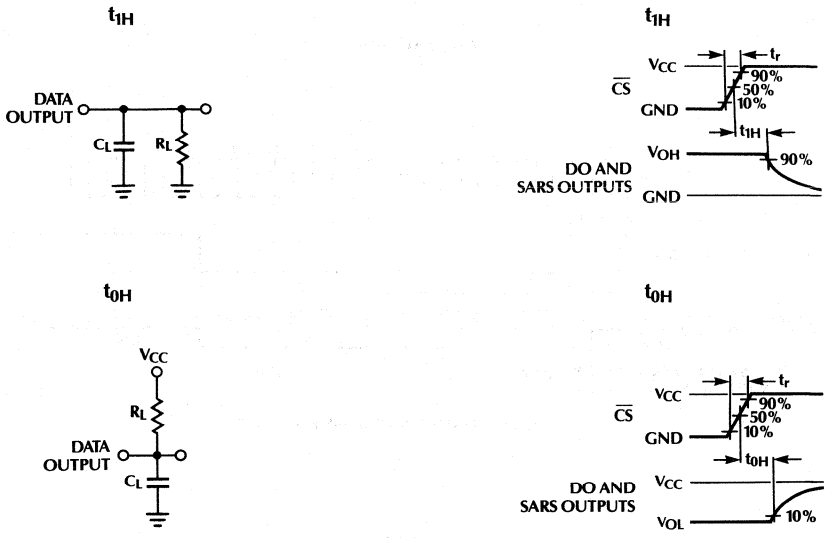


Figure 1. High Impedance Test Circuits and Waveforms

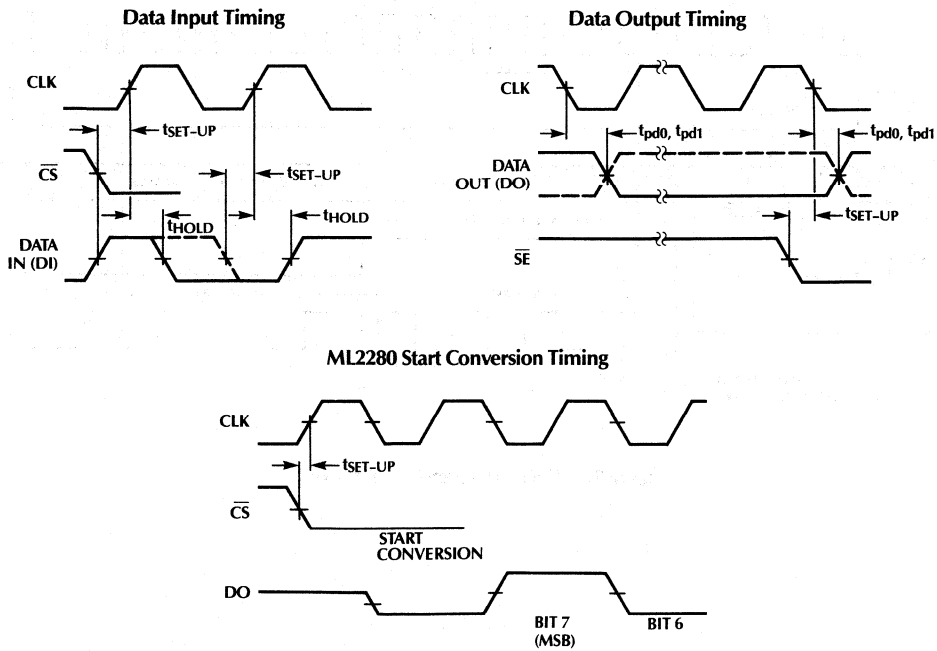
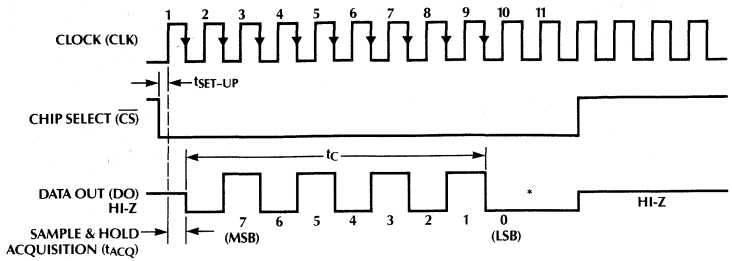


Figure 2. Timing Diagrams

ML2280 Timing



*LSB FIRST OUTPUT NOT AVAILABLE ON ML2280

ML2283 Timing

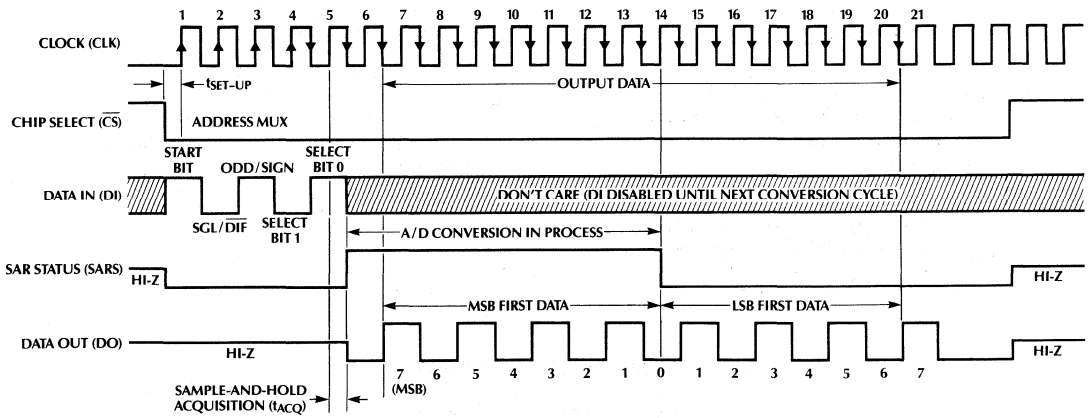


Figure 2. Timing Diagrams (Continued)

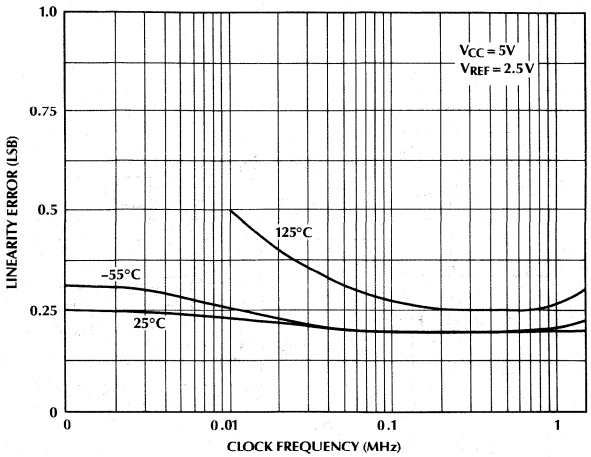


Figure 3. Linearity Error vs f_{CLK}

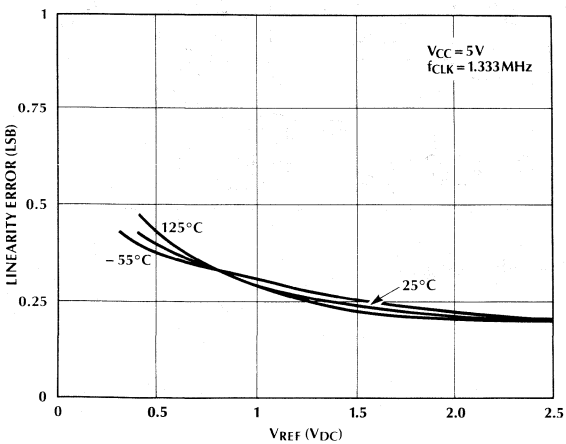


Figure 4. Linearity Error vs V_{REF} Voltage

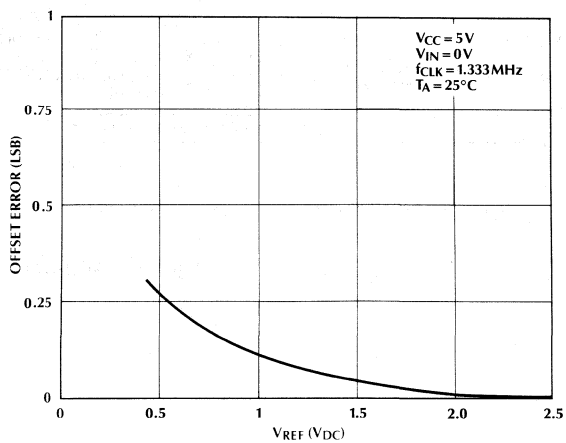


Figure 5. Unadjusted Offset Error vs V_{REF} Voltage

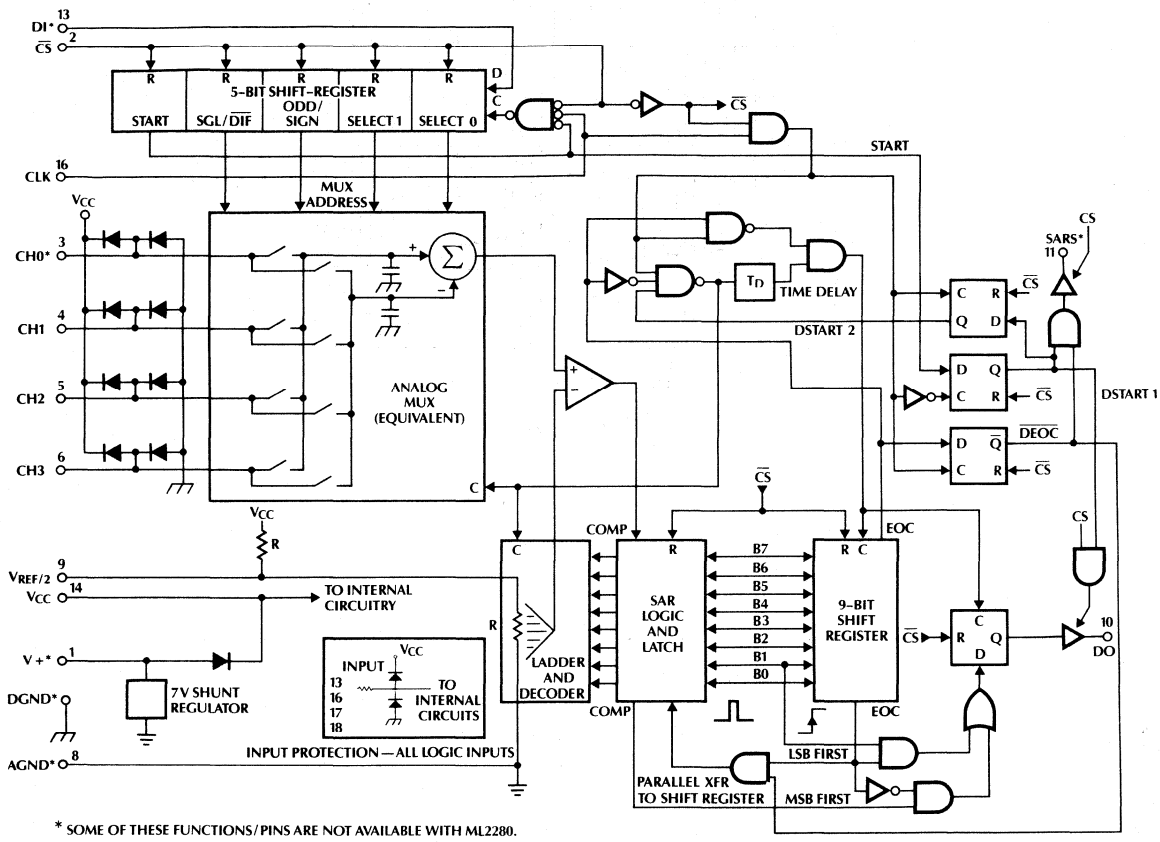


Figure 6. ML2283 Functional Block Diagram

1.0 FUNCTIONAL DESCRIPTION

1.1 Multiplexer Addressing

The design of these converters utilizes a sample data comparator structure which provides for a differential analog input to be converted by a successive approximation routine.

The actual voltage converted is always the difference between an assigned "+" input terminal and a "−" input terminal. The polarity of each input terminal of the pair being converted indicates which line the converter expects to be the most positive. If the assigned "+" input is less than the "−" input, the converter responds with an all zeros output code.

A unique input multiplexing scheme has been utilized to provide multiple analog channels with software configurable single ended, or differential options.

A particular input configuration is assigned during the MUX addressing sequence, prior to the start of a conversion. The MUX address selects which of the analog inputs are to be enabled and whether this input is single ended or differential. In the differential case, it also assigns the polarity of the analog channels. Differential inputs are restricted to adjacent channel pairs. For example, channel 0 and channel 1 may be selected as a different pair but channel 0 or channel 1 cannot act differentially with any other channel. In addition to selecting the differential mode, the sign may also be selected. Channel 0 may be selected as the positive input and channel 1 as the negative input or vice versa. This programmability is illustrated by the MUX addressing codes shown in *Table 1*.

The MUX address is shifted into the converter via the DI input. Since the ML2280 contains only one differential input channel with a fixed polarity assignment, it does not require addressing.

Since the input configuration is under software control, it can be modified, as required, at each conversion. A channel can be treated as a single-ended, ground referenced input for one conversion; then it can be reconfigured as part of a differential channel for another conversion. *Figure 7* illustrates these different input modes.

Table 1. ML2283 MUX Addressing 4 Single-Ended or 2 Differential Channel

Single-Ended MUX Mode

MUX Address				Channel #			
SGL/ DIF	ODD/ SIGN	SELECT 1	SELECT 0	0	1	2	3
1	0	0	1	+			
1	0	1	1			+	
1	1	0	1		+		
1	1	1	1				+

Differential MUX Mode

MUX Address				Channel #			
SGL/ DIF	ODD/ SIGN	SELECT 1	SELECT 0	0	1	2	3
0	0	0	1	+	−		
0	0	1	1			+	−
0	1	0	1	−	+		
0	1	1	1			−	+

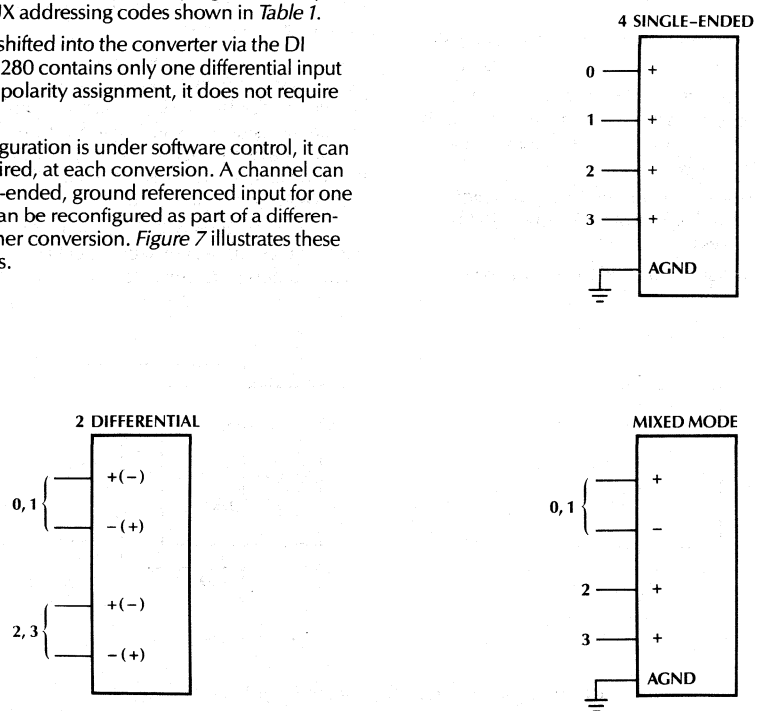


Figure 7. Analog Input Multiplexer Functional Options for ML2283

1.2 Digital Interface

The block diagram and timing diagrams in *Figures 2-5* illustrate how a conversion sequence is performed.

A conversion is initiated when $\overline{CS}$ is pulsed low. This line must be held low for the entire conversion. The converter is now waiting for a start bit and its MUX assignment word.

A clock is applied to the CLK input. On each rising edge of the clock, the data on DI is clocked into the MUX address shift register. The start bit is the first logic "1" that appears on the DI input (all leading edge zeros are ignored). After the start bit, the device clocks in the next 2 to 4 bits for the MUX assignment word.

When the start bit has been shifted into the start location of the MUX register, the input channel has been assigned and a conversion is about to begin. An interval of 1/2 clock period is used for sample-and-hold settling through the selected MUX channels. The SAR status output goes high at this time to signal that a conversion is now in progress and the DI input is ignored.

The DO output comes out of high impedance and provides a leading zero for this one clock period.

When the conversion begins, the output of the comparator, which indicates whether the analog input is greater than or less than each successive voltage from the internal DAC, appears at the DO output on each falling edge of the clock. This data is the result of the conversion being shifted out (with MSB coming first) and can be read by external logic or μP immediately.

After 8 clock periods, the conversion is completed. The SAR status line returns low to indicate this 1/2 clock cycle later.

The serial data is always shifted out MSB first during the conversion. After the conversion has been completed, the data is shifted out a second time with LSB first. The ML2280 data is shifted out only once, MSB first.

All internal registers are cleared when the $\overline{CS}$ input is high. If another conversion is desired, $\overline{CS}$ must make a high to low transition followed by address information.

The DI input and DO output can be tied together and controlled through a bidirectional μP I/O bit with one connection. This is possible because the DI input is only latched in during the MUX addressing interval while the DO output is still in the high impedance state.

1.3 Reference

The ML2280 and ML2283 are intended primarily for use in circuits requiring absolute accuracy. In this type of system, the analog inputs vary between very specific voltage limits and the reference voltage for the A/D converter must remain stable with time and temperature. For ratiometric applications, see the ML2281 and ML2284 which have a V_{REF} input that can be tied to V_{CC}.

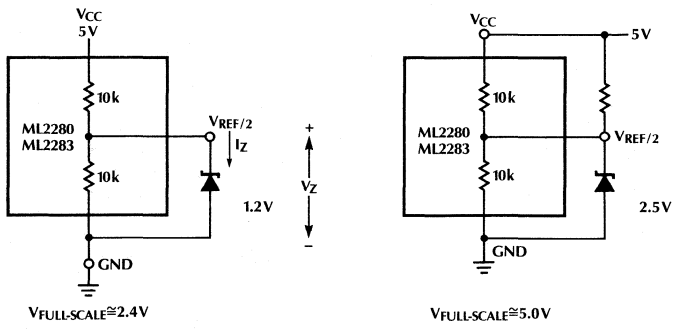
The voltage applied to the $V_{REF/2}$ pin defines the voltage span of the analog input (the difference between VIN+ and $V_{IN}-$) over which the 256 possible output codes apply. A full-scale conversion (an all 1s output code) will result when the voltage difference between a selected "+" input and "−" input is approximately *twice* the voltage at the $V_{REF/2}$ pin. This internal gain of 2 from the applied reference to the full-scale input voltage allows biasing a low voltage reference diode from the $5V_{DC}$ converter supply. To accommodate a 5V input span, only a 2.5V reference is required. The output code changes in accordance with the following equation:

$$\text{Output Code} = 256\left(\frac{V_{IN}(+) - V_{IN}(-)}{2(V_{REF}/2)}\right)$$

where the output code is the decimal equivalent of the 8-bit binary output (ranging from 0 to 255) and the term $V_{REF/2}$ is the voltage to ground.

The $V_{REF/2}$ pin is the center point of a two resistor divider (each resistor is 10kΩ) connected from V_{CC} to ground. Total ladder input resistance is the parallel combination of these two equal resistors. As shown in *Figure 8*, a reference diode with a voltage less than $V_{CC/2}$ can be connected without requiring an external biasing resistor if its current requirements meet the indicated level.

The minimum value of $V_{REF/2}$ can be quite small (See Typical Performance Curves) to allow direct conversions of transducer outputs providing less than a 5V output span. Particu-



NOTE: NO EXTERNAL BIASING RESISTOR NEEDED IF $V_Z < \frac{V_{CC}}{2}$ and I_Z min. $< \frac{V_{CC/2} - V_Z}{5k\Omega}$

Figure 8. Reference Biasing

lar care must be taken with regard to noise pickup, circuit layout and system error voltage sources when operating with a reduced span due to the increased sensitivity of the converter (1 LSB equals $V_{REF/256}$).

1.4 Analog Inputs and Sample/Hold

An important feature of the ML2280 and ML2283 is that they can be located at the source of the analog signal and then communicate with a controlling μP with just a few wires. This avoids bussing the analog inputs long distances and thus reduces noise pickup on these analog lines. However, in some cases, the analog inputs have a large common mode voltage or even some noise present along with the valid analog signal.

The differential input of these converters reduces the effects of common mode input noise. Thus, if a common mode voltage is present on both "+" and "−" inputs, such as 60 Hz, the converter will reject this common mode voltage since it only converts the difference between "+" and "−" inputs.

The ML2280 and ML2283 have a true sample-and-hold circuit which samples both "+" and "−" inputs simultaneously. This simultaneous sampling with a true S/H will give common mode rejection and AC linearity performance that is superior to devices where the two input terminals are not sampled at the same instant and where true sample-and-hold capability does not exist. Thus, these A/D converters can reject AC common mode signals from DC-50 kHz as well as maintain linearity for signals from DC-50kHz.

The signal at the analog input is sampled during the interval when the sampling switch is closed prior to conversion start. The sampling window (S/H acquisition time) is ½ CLK period wide and occurs ½ CLK period before DO goes from high impedance to active low state. When the sampling switch closes at the start of the S/H acquisition time, 8 pF of capacitance is thrown onto the analog input. ½ CLK period later, the sampling switch is opened and the signal present at the analog input is stored. Any error on the analog input at the end of the S/H acquisition time will cause additional conversion error. Care should be taken to allow adequate charging or settling time from the source. If more charging or settling time is needed to reduce these analog input errors, a longer CLK period can be used.

For latch-up immunity each analog input has dual diodes to the supply rails, and a minimum of ±25 mA (±100 mA typically) can be injected into each analog input without causing latch-up.

1.5 Zero Error Adjustment

The zero of the A/D does not require adjustment. If the minimum analog input voltage value, V_{INMIN} is not ground, a zero offset can be done. The converter can be made to output 00000000 digital code for this minimum input voltage by biasing any $V_{IN}-$ input at this V_{INMIN} value. This utilizes the differential mode operation of the A/D.

The zero error of the A/D converter relates to the location of the first riser of the transfer function and can be measured by grounding the $V_{IN}-$ input and applying a small magnitude positive voltage to the $V_{IN}+$ input. Zero error is the difference between the actual DC input voltage which is necessary to just cause an output digital code transition from 00000000 to 00000001 and the ideal ½ LSB value (½ LSB = 9.8 mV for $V_{REF/2} = 2.500 V_{DC}$).

1.6 Full-Scale Adjustment

The full-scale adjustment can be made by applying a differential input voltage which is 1½ LSB down from the desired analog full-scale voltage range and then adjusting the magnitude of the $V_{REF/2}$ input for a digital output code which is just changing from 11111110 to 11111111.

1.7 Adjustment for an Arbitrary Analog Input Voltage Range

If the analog zero voltage of the A/D is shifted away from ground (for example, to accommodate an analog input signal which does not go to ground), this new zero reference should be properly adjusted first. A $V_{IN}+$ voltage which equals this desired zero reference plus ½ LSB (where the LSB is calculated for the desired analog span, 1 LSB = analog span/256) is applied to selected "+" input and the zero reference voltage at the corresponding "−" input should then be adjusted to just obtain the 00000000 to 00000001 code transition.

The full-scale adjustment should be made by forcing a voltage to the $V_{IN}+$ input which is given by:

$V_{IN}+$ fs adjust = $V_{MAX} - 1.5*[(V_{MAX} - V_{MIN})/256]$
where V_{MAX} = high end of the analog input range
V_{MIN} = low end (offset zero) of the analog range

The V_{REF} or V_{CC} voltage is then adjusted to provide a code change from 11111110 to 11111111.

1.8 Shunt Regulator

A unique feature of the ML2283 is the inclusion of a shunt regulator connected from V+ terminal to ground which also connects to the V_{CC} terminal (which is the actual converter supply) through a silicon diode as shown in *Figure 9*. When the regulator is turned on, the V+ voltage is clamped at 11 V_{BE} set by the internal resistor ratio. The typical I-V curve of the shunt regulator is shown in *Figure 10*. It should be noted that before V+ voltage is high enough to turn on the shunt regulator (which occurs at about 5.5 V), 35 kΩ of resistance is observed between V+ and GND. When the shunt regulator is not used, V+ pin should be either left floating or tied to GND. The temperature coefficient of the regulator is −22 mV/°C.

2.0 APPLICATIONS

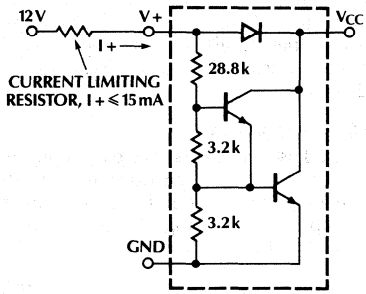


Figure 9. Shunt Regulator

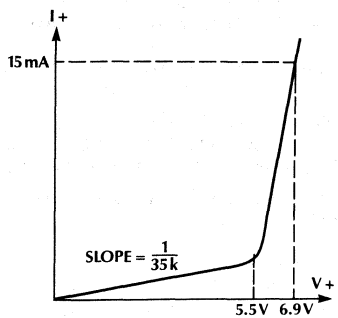
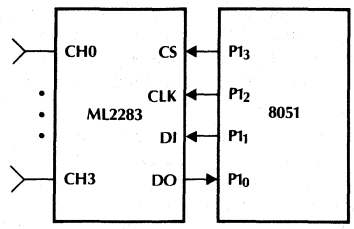


Figure 10. I–V Characteristic of the Shunt Regulator

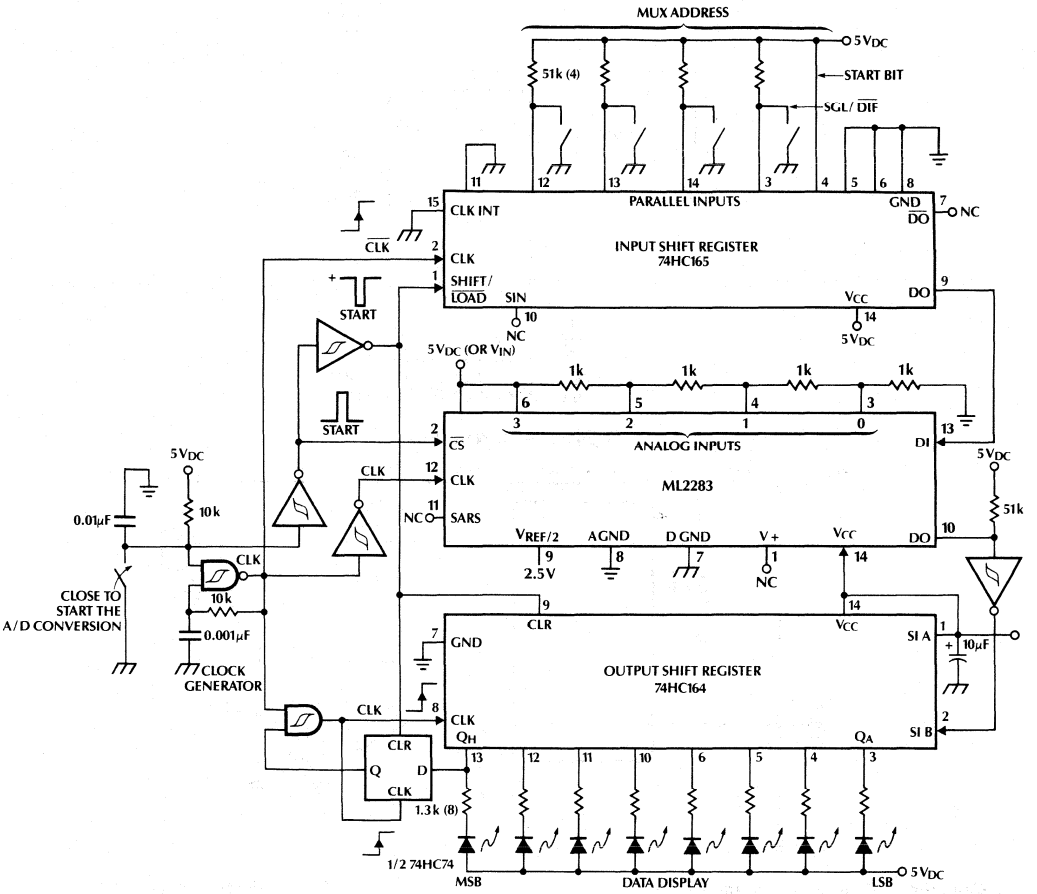
8051 Interface and Controlling Software



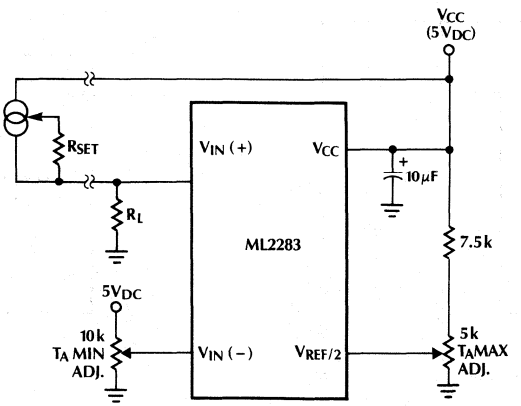
Mnemonic			Instruction
START	ANL	P1, #0F7H	;SELECT A/D (CS = 0)
	MOV	B, #5	;BIT COUNTER ← 5
	MOV	A, #ADDR	;A ← MUX BIT
LOOP 1:	RRC	A	;CY ← ADDRESS BIT
	JC	ONE	;TEST BIT ;BIT = 0
ZERO:	ANL	P1, #0FEH	;DI ← 0
	SJMP	CONT	;CONTINUE ;BIT = 1
ONE:	ORL	P1, #1	;D1 ← 1
CONT:	ACALL	PULSE	;PULSE SK 0 → 1 → 0
	DJNZ	B, LOOP 1	;CONTINUE UNTIL DONE
	ACALL	PULSE	;EXTRA CLOCK FOR SYNC
	MOV	B, #8	;BIT COUNTER ← 8
LOOP 2:	ACALL	PULSE	;PULSE SK 0 → 1 → 0
	MOV	A, P1	;CY ← DO
	RRC	A	
	RRC	A	
	MOV	A, C	;A ← RESULT
	RLC	A	;A(0) ← BIT AND SHIFT
	MOV	C, A	;C ← RESULT
	DJNZ	B, LOOP 2	;CONTINUE UNTIL DONE
RETI			
			;PULSE SUBROUTINE
PULSE:	ORL	P1, #04	;SK ← 1
	NOP		;DELAY
	ANL	P1, #0FBH	;SK ← 0
	RET		

APPLICATIONS (Continued)

ML2283 "Stand-Alone" or Evaluation Circuit

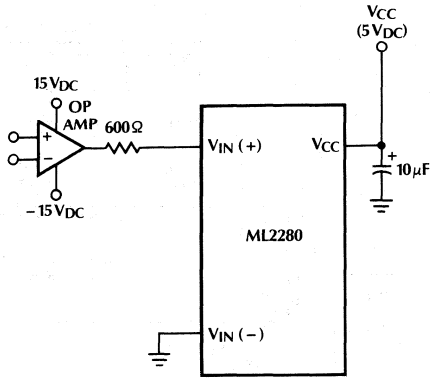


Low-Cost Remote Temperature Sensor



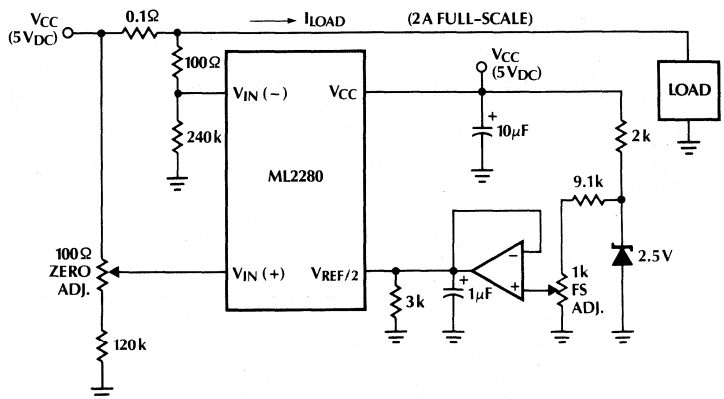
APPLICATIONS (Continued)

Protecting the Input

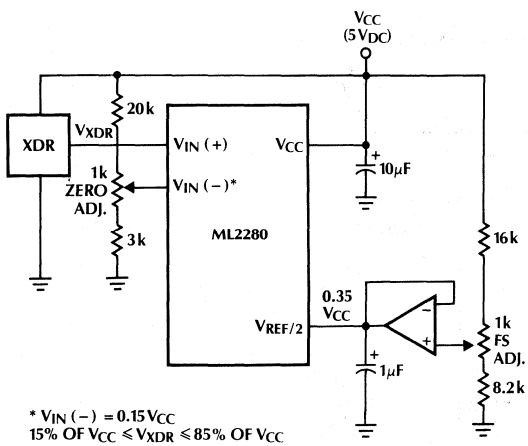


DIODE CLAMPING IS NOT NEEDED
IF CURRENT IS LIMITED TO 25 mA

Digitizing a Current Flow

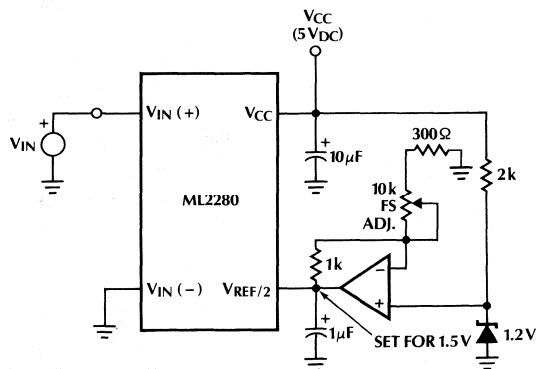


Operating with Ratiometric Transducers



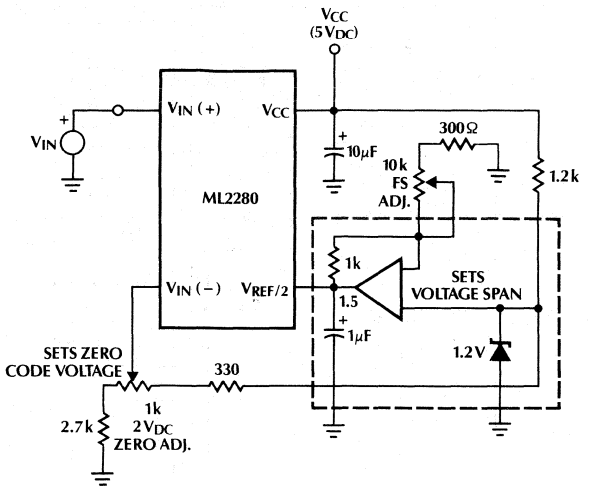
* $V_{IN}(-) = 0.15 V_{CC}$
$15\% \text{ OF } V_{CC} \leq V_{XDR} \leq 85\% \text{ OF } V_{CC}$

Span Adjust: $0V \leq V_{IN} \leq 3V$

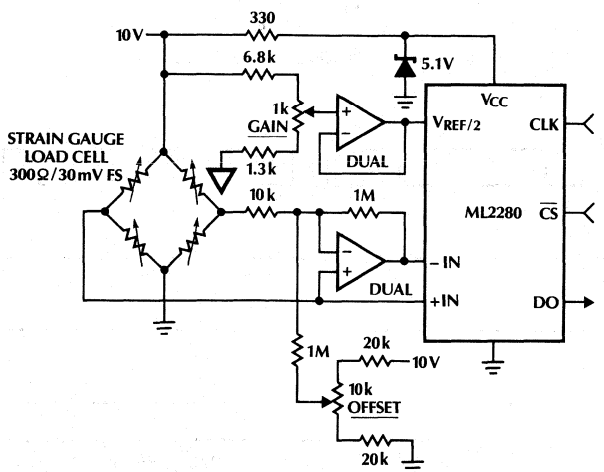


APPLICATIONS (Continued)

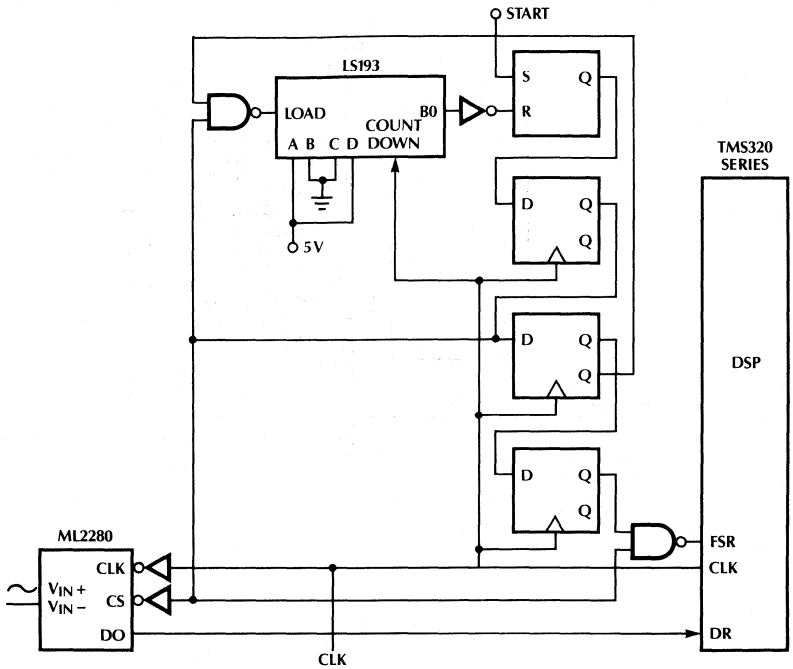
Zero-Shift and Span Adjust: $2V \leqslant V_{IN} \leqslant 5V$



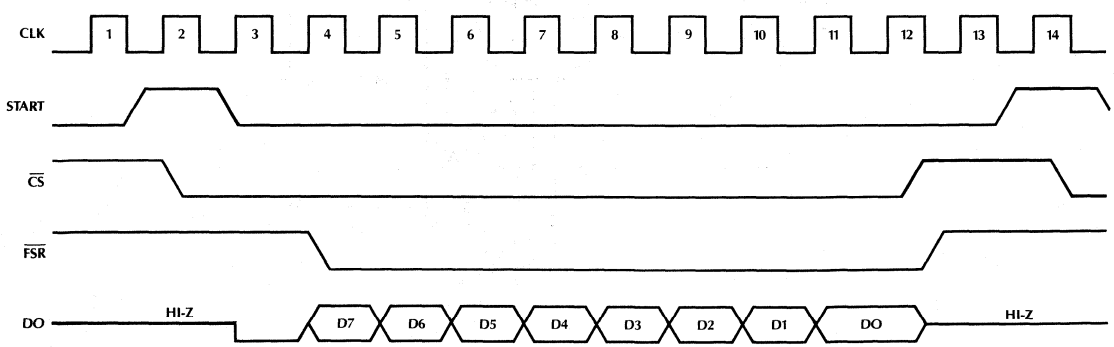
Digital Load Cell



- USES ONE MORE WIRE THAN LOAD CELL ITSELF
- TWO MINI-DIPs COULD BE MOUNTED INSIDE LOAD CELL FOR DIGITAL OUTPUT TRANSDUCER
- ELECTRONIC OFFSET AND GAIN TRIMS RELAX MECHANICAL SPECS FOR GAUGE FACTOR AND OFFSET
- LOW LEVEL CELL OUTPUT IS CONVERTED IMMEDIATELY FOR HIGH NOISE IMMUNITY



Sampling Rate 111KHz, Data Rate 1.33MHz



Interfacing ML2280 to TMS320 Series

ORDERING INFORMATION

PART NUMBER	ALTERNATE PART NUMBER	TOTAL UNADJUSTED ERROR	TEMPERATURE RANGE	PACKAGE
SINGLE ANALOG INPUT, 8-PIN PACKAGE				
ML2280BMJ		±½LSB	−55°C to +125°C	HERMETIC DIP
ML2280BIJ			−40°C to +85°C	HERMETIC DIP
ML2280BCP			0° to +70°C	MOLDED DIP
ML2280CIJ		±1LSB	−40°C to +85°C	HERMETIC DIP
ML2280CCP			0°C to +70°C	MOLDED DIP
FOUR ANALOG INPUTS, 14-PIN PACKAGE				
ML2283BMJ	ADC0833BJ	±½LSB	−55°C to +125°C	HERMETIC DIP
ML2283BIJ	ADC0833BCJ		−40°C to +85°C	HERMETIC DIP
ML2283BCP	ADC0833BCN		0° to +70°C	MOLDED DIP
ML2283CIJ	ADC0833CCJ	±1LSB	−40°C to +85°C	HERMETIC DIP
ML2283CCP	ADC0833CCN		0°C to +70°C	MOLDED DIP

2

Micro Linear

ML2281, ML2282
ML2284, ML2288

Serial I/O 8-Bit A/D Converters with Multiplexer Options

GENERAL DESCRIPTION

The ML2281 family are 8-bit successive approximation A/D converters with serial I/O and configurable input multiplexers with up to 8 input channels.

All errors of the sample-and-hold, incorporated on the ML2281 family are accounted for in the analog-to-digital converters accuracy specification.

The voltage reference can be externally set to any value between GND and V_{CC}, thus allowing a full conversion over a relatively small voltage span if desired.

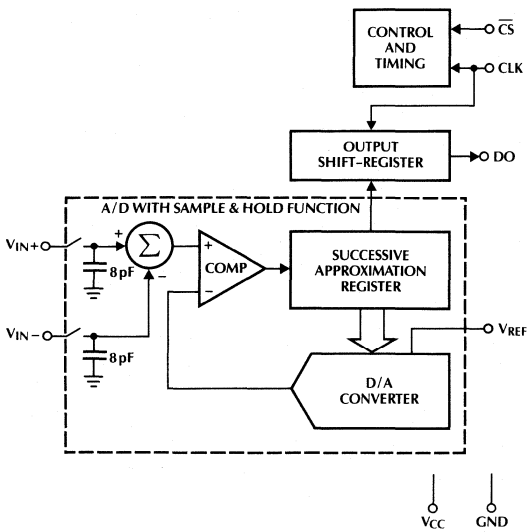
The ML2281 family is an enhanced double polysilicon CMOS pin compatible second source for the ADC0831, ADC0832, ADC0834, and ADC0838 A/D converters. The ML2281 series enhancements are faster conversion time, true sample-and-hold function, superior power supply rejection, improved AC common mode rejection, faster digital timing, and lower power dissipation. All parameters are guaranteed over temperature with a power supply voltage of 5V ±10%.

FEATURES

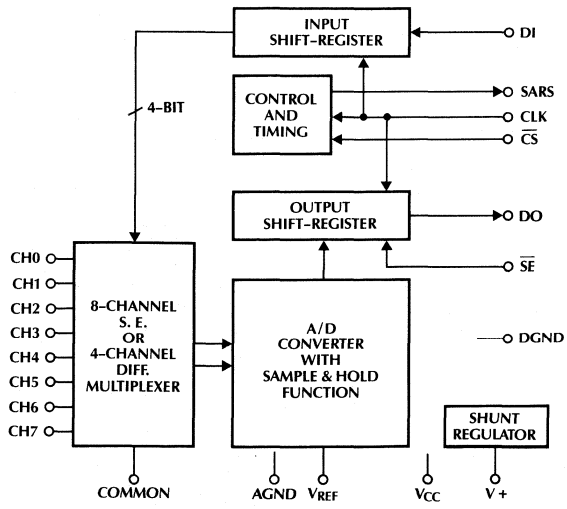
- Conversion time 6μs
- Total unadjusted error ±½LSB or ±1LSB
- Sample-and-hold 375ns acquisition
- 2, 4, or 8-input multiplexer options
- 0 to 5V analog input range with single 5V power supply
- Operates ratiometrically or with up to 5V voltage reference
- No zero or full-scale adjust required
- ML2281 capable of digitizing a 5V, 40kHz sine wave
- Low power 12.5mW MAX
- 0.3″ width 8-, 14-, or 20-pin DIP
- 20-pin surface mount PCC ML2288
- Superior pin compatible replacement for ADC0831, ADC0832, ADC0834, and ADC0838
- Analog input protection 25mA (min) per input

BLOCK DIAGRAMS

ML2281



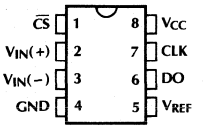
ML2288



PIN CONNECTIONS

ML2281 Single Differential Input

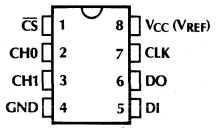
8-PIN DIP



TOP VIEW

ML2282 2-Channel MUX

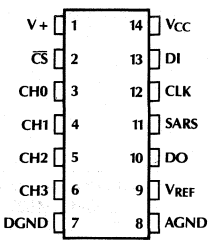
8-PIN DIP



TOP VIEW

ML2284 4-Channel MUX

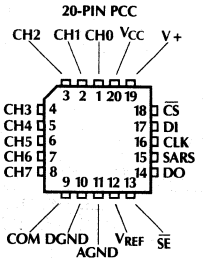
14-PIN DIP



TOP VIEW

ML2288 8-Channel MUX

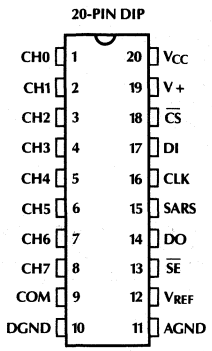
20-PIN PCC



TOP VIEW

ML2288 8-Channel MUX

20-PIN DIP



TOP VIEW

PIN DESCRIPTION

NAME	FUNCTION
V_{CC}	Positive supply. 5 volts ± 10%
DGND	Digital ground. 0 volts. All digital inputs and outputs are referenced to this point.
AGND	Analog ground. The negative reference voltage for A/D converter.
CH0-7, $V_{IN}+$, $V_{IN}-$	Analog inputs. Digitally selected to be single ended (V_{IN}) or; $V_{IN}+$ or $V_{IN}-$ of a differential input. Analog range = GND ≤ V_{IN} ≤ V_{CC}
COM	Common reference point for analog inputs. A/D conversion is performed on voltage difference between analog input and this common reference point if single-end conversion is specified.
V_{REF}	Reference. The positive reference voltage for A/D converter.
$\overline{SE}$	Shift enable. Input controls whether LSB first bit stream is shifted out on serial output DO. If $\overline{SE}$ = 1, MSB first is shifted out only. If $\overline{SE}$ = 0, an MSB first bit stream is shifted out, then a second bit stream with LSB first is shifted out after end of conversion.
V+	Input to the Shunt Regulator.

NAME	FUNCTION
DO	Data out. Digital output which contains result of A/D conversion. The serial data is clocked out on falling edges of CLK.
SARS	Successive approximation register status. Digital output which indicates that a conversion is in progress. When SARS goes to 1, the sampling window is closed and conversion begins. When SARS goes to 0, conversion is completed. When $\overline{CS}$ = 1, SARS is in high impedance state.
CLK	Clock. Digital input which clocks data in on DI on rising edges and out on DO on falling edges. Also used to generate clocks for A/D conversion.
DI	Data input. Digital input which contains serial data to program the MUX and channel assignments.
$\overline{CS}$	Chip select. Selects the chip for multiplexer and channel assignment and A/D converison. When $\overline{CS}$ = 1, all digital outputs are in high impedance state. When $\overline{CS}$ = 0, normal A/D conversion takes place.

ABSOLUTE MAXIMUM RATINGS

(Note 1)

Current into V+ 15mA
Supply Voltage, V_{CC} 6.5V
Voltage
  Logic Inputs ..... $-7V$ to V_{CC} $+7V$
  Analog Inputs ..... $-0.3V$ to V_{CC} $+0.3V$
Input Current per Pin (Note 2) ..... $\pm 25mA$
Storage Temperature ..... $-65°C$ to $+150°C$
Package Dissipation
  at $T_A = 25°C$ (Board Mount) 800mW
Lead Temperature (Soldering 10 sec.)
  Dual-In-Line Package (Molded) ..... 260°C
  Dual-In-Line Package (Ceramic) ..... 300°C
  Molded Chip Carrier Package
    Vapor Phase (60 sec.) ..... 215°C
    Infrared (15 sec.) ..... 220°C

OPERATING CONDITIONS

Supply Voltage, V_{CC} ..... $4.5V_{DC}$ to $6.3V_{DC}$
Temperature Range (Note 3) ..... $T_{MIN} \leq T_A \leq T_{MAX}$
  ML2281/2/4/8 BMJ ..... $-55°C$ to $+125°C$
  ML2281/2/4/8 CMJ
  ML2281/2/4/8 BIJ ..... $-40°C$ to $+85°C$
  ML2281/2/4/8 CIJ
  ML2281/2/4/8 BCP ..... 0°C to +70°C
  ML2281/2/4/8 CCP

ELECTRICAL CHARACTERISTICS

Unless otherwise specified $T_A = T_{MIN}$ to T_{MAX}, $V_{CC} = V_{REF} = 5V \pm 10\%$, and $f_{CLK} = 1.333MHz$

PARAMETER	NOTES	CONDITIONS	ML2281B, ML2282B ML2284B, ML2288B			ML2281C, ML2282C ML2284C, ML2288C			UNITS
			MIN	TYP NOTE 4	MAX	MIN	TYP NOTE 4	MAX	
CONVERTER AND MULTIPLEXER CHARACTERISTICS									
Total Unadjusted Error	5, 7	$V_{REF} = V_{CC}$			$\pm 1/2$			± 1	LSB
Reference Input Resistance	5,8		6	10	15	6	10	15	kΩ
Common-Mode Input Range	5,9		GND -0.05		V_{CC} $+0.05$	GND -0.05		V_{CC} $+0.05$	V
DC Common-Mode Error	6	Common Mode Voltage GND to $V_{CC/2}$		$\pm 1/16$	$\pm 1/4$		$\pm 1/16$	$\pm 1/4$	LSB
AC Common-Mode Error	6	Comon Mode Voltage GND to $V_{CC/2}$, 0 to 50kHz			$\pm 1/4$			$\pm 1/4$	LSB
DC Power Supply Sensitivity	6	$V_{CC} = 5V \pm 10\%$ $V_{REF} \leq V_{CC} + 0.1V$		$\pm 1/32$	$\pm 1/4$		$\pm 1/32$	$\pm 1/4$	LSB
AC Power Supply Sensitivity	6	$100mV_{P-P}$, 25kHz sine on V_{CC}			$\pm 1/4$			$\pm 1/4$	LSB
Change in Zero Error from $V_{CC} = 5V$ to Internal Zener Operation	6	15mA into V+ V_{CC} = N.C. $V_{REF} = 5V$		$\pm 1/2$			$\pm 1/2$		LSB
V_Z, Internal Diode Regulated Breakdown (at V+)		15mA into V+		6.9			6.9		V
V+ Input Resistance	5		20	35		20	35		kΩ
I_{Off}, Off Channel Leakage Current	5, 10	On Channel = V_{CC} Off Channel = 0V	-1			-1			μA
		On Channel = 0V Off Channel = V_{CC}			+1			+1	μA
I_{On}, On Channel Leakage Current	5, 10	On Channel = 0V Off Channel = V_{CC}	-1			-1			μA
		On Channel = V_{CC} Off Channel = 0V			+1			+1	μA

ELECTRICAL CHARACTERISTICS (Continued)

Unless otherwise specified $T_A = T_{MIN}$ to T_{MAX}, $V_{CC} = V_{REF} = 5V \pm 10\%$, and $f_{CLK} = 1.333MHz$

PARAMETER	NOTES	CONDITIONS	ML2281B, ML2282B ML2284B, ML2288B MIN	TYP NOTE 4	MAX	ML2281C, ML2282C ML2284C, ML2288C MIN	TYP NOTE 4	MAX	UNITS
DIGITAL AND DC CHARACTERISTICS									
$V_{IN(1)}$, Logical "1" Input Voltage	5		2.0			2.0			V
$V_{IN(0)}$, Logical "0" Input Voltage	5				0.8			0.8	V
$I_{IN(1)}$, Logical "1" Input Current	5	$V_{IN} = V_{CC}$			1			1	µA
$I_{IN(0)}$, Logical "0" Input Current	5	$V_{IN} = 0V$	−1			−1			µA
$V_{OUT(1)}$, Logical "1" Output Voltage	5	$I_{OUT} = -2mA$	4.0			4.0			V
$V_{OUT(0)}$, Logical "0" Output Voltage	5	$I_{OUT} = 2mA$			0.4			0.4	V
I_{OUT}, Hi-Z Output Current	5	$V_{OUT} = 0V$ $V_{OUT} = V_{CC}$	−1		 1	−1		 1	µA µA
I_{SOURCE}, Output Source Current	5	$V_{OUT} = 0V$	−6.5			−6.5			mA
I_{SINK}, Output Sink Current	5	$V_{OUT} = V_{CC}$			8.0			8.0	mA
I_{CC}, Supply Current ML2281, ML2284, ML2288	5			1.3	2.5		1.3	2.5	mA
ML2282	5	Includes Ladder Current		1.8	3.5		1.8	3.5	mA

PARAMETER	NOTES	CONDITIONS	MIN	TYP NOTE 4	MAX	LIMIT UNITS
AC ELECTRICAL CHARACTERISTICS						
f_{CLK}, Clock Frequency	5		10		1333	kHz
t_{ACQ}, Sample-and-Hold Acquistion				1/2		$1/f_{CLK}$
t_C, Conversion Time		Not including MUX Addressing Time		8		$1/f_{CLK}$
SNR, Signal to Noise Ratio ML2281	12	$V_{IN} = 40kHz$, 5V Sine. $f_{CLK} = 1.333MHz$ ($f_{SAMPLING} \cong 120kHz$). Noise is Sum of All Nonfundamental Components up to 1/2 of $f_{SAMPLING}$		47		dB
THD, Total Harmonic Distortion ML2281	12	$V_{IN} = 40kHz$, 5V Sine. $f_{CLK} = 1.333MHz$ ($f_{SAMPLING} \cong 120kHz$). THD is Sum of 2, 3, 4, 5 Harmonics Relative to Fundamental		−60		dB

ELECTRICAL CHARACTERISTICS

Unless otherwise specified $T_A = T_{MIN}$ to T_{MAX}, $V_{CC} = V_{REF} = 5V \pm 10\%$, and $f_{CLK} = 1.333MHz$

PARAMETER	NOTES	CONDITIONS	MIN	TYP NOTE 4	MAX	LIMIT UNITS
AC ELECTRICAL CHARACTERISTICS (Continued)						
IMD, Intermodulation Distortion ML2281	12	$V_{IN} = f_A + f_B$. $f_A = 40kHz$, 2.5V Sine. $f_B = 39.8kHz$, 2.5V Sine, $f_{CLK} = 1.333MHz$ ($f_{SAMPLING} \cong 120kHz$). IMD is $(f_A + f_B)$, $(f_A - f_B)$, $(2f_A + f_B)$, $(2f_A - f_B)$, $(f_A + 2f_B)$, $(f_A - 2f_B)$ Relative to Fundamental		-60		dB
Clock Duty Cycle	5, 11		40		60	%
t_{SET-UP}, $\overline{CS}$ Falling Edge or Data Input Valid to CLK Rising Edge	5		130			ns
t_{HOLD}, Data Input Valid after CLK Rising Edge	5		80			ns
t_{pd1}, t_{pd0} — CLK Falling Edge to Output Data Valid	5, 13	$C_L = 100pF$ Data MSB First Data LSB First		 90 50	 200 110	 ns ns
t_{1H}, t_{0H}, — Rising Edge of $\overline{CS}$ to Data Output and SARS Hi-Z	6	$C_L = 10pF$, $R_L = 10k$ (see High Impedance Test Circuits)		40	90	ns
	5	$C_L = 100pF$, $R_L = 2k$		80	160	ns
C_{IN}, Capacitance of Logic Input				5		pF
C_{OUT}, Capacitance of Logic Outputs				5		pF

Note 1: Absolute maximum ratings are limits beyond which the life of the integrated circuit may be impaired. All voltages unless otherwise specified are measured with respect to ground.

Note 2: When the input voltage (V_{IN}) at any pin exceeds the power supply rails ($V_{IN} < GND$ or $V_{IN} > V_{CC}$) the absolute value of current at that pin should be limited to 25mA or less.

Note 3: -55°C to +125°C operating temperature range devices are 100% tested at temperature extremes with worst-case test conditions. 0°C to 70°C and -40°C to +85°C operating temperature range devices are 100% tested with temperature limits guaranteed by 100% testing, sampling, or by correlation with worst-case test conditions.

Note 4: Typicals are parametric norm at 25°C.

Note 5: Parameter guaranteed and 100% production tested.

Note 6: Parameter guaranteed. Parameters not 100% tested are not in outgoing quality level calculation.

Note 7: Total unadjusted error includes offset, full-scale, linearity, multiplexer and sample-and-hold errors.

Note 8: Cannot be tested for ML2282.

Note 9: For $V_{IN}(-) \geq V_{IN}(+)$ the digital output code will be 0000 0000. Two on-chip diodes are tied to each analog input (see Block Diagram) which will forward conduct for analog input voltages one diode drop below ground or one diode drop greater then the V_{CC} supply. Be careful, during testing at low V_{CC} levels (4.5V), as high level analog inputs (5V) can cause this input diode to conduct-especially at elevated temperatures, and cause errors for analog inputs near full-scale. The spec allows 50mV forward bias of either diode. This means that as long as the analog V_{IN} or V_{REF} does not exceed the supply voltage by more than 50mV, the output code will be correct. To achieve an absolute 0V to 5V input voltage range will therefore require a minimum supply voltage of 4.950 V_{DC} over temperature variations, initial tolerance and loading.

Note 10: Leakage current is measured with the clock not switching.

Note 11: A 40% to 60% clock duty cycle range insures proper operation at all clock frequencies. In the case that an available clock has a duty cycle outside of these limits, the minimum, time the clock is high or the minimum time the clock is low must be at least 300ns. The maximum time the clock can be high or low is 60μs.

Note 12: Because of multiplexer addressing, test conditions for the ML2282 would be $V_{IN} = 34kHz$, 5V sine ($f_{SAMPLING} \approx 102kHz$); ML2284 $V_{IN} = 32kHz$, 5V sine ($f_{SAMPLING} \approx 95kHz$); ML2288 $V_{IN} = 30kHz$, 5V sine ($f_{SAMPLING} \approx 89kHz$).

Note 13: Since data, MSB first, is the output of the comparator used in the successive approximation loop, an additional delay is built in (see Block Diagram) to allow for comparator response time.

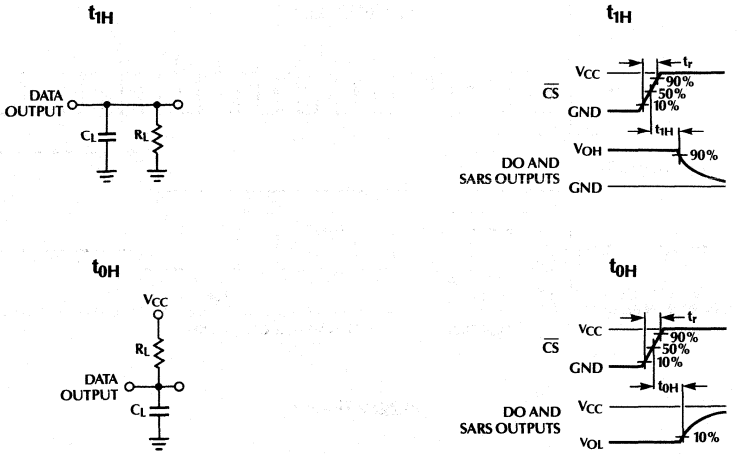


Figure 1. High Impedance Test Circuits and Waveforms

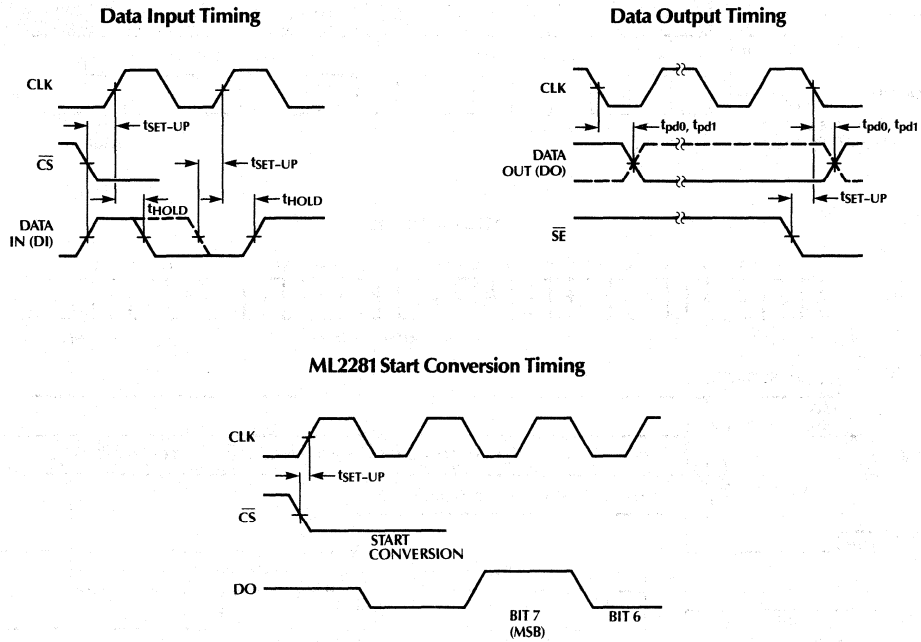
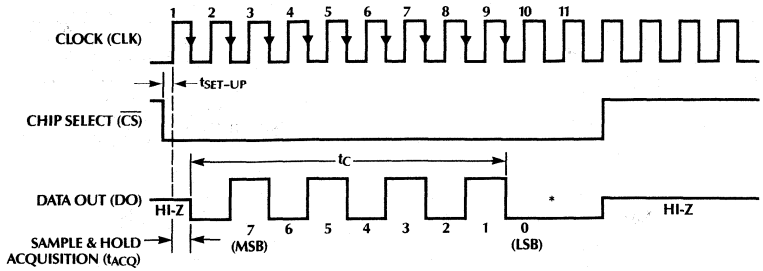


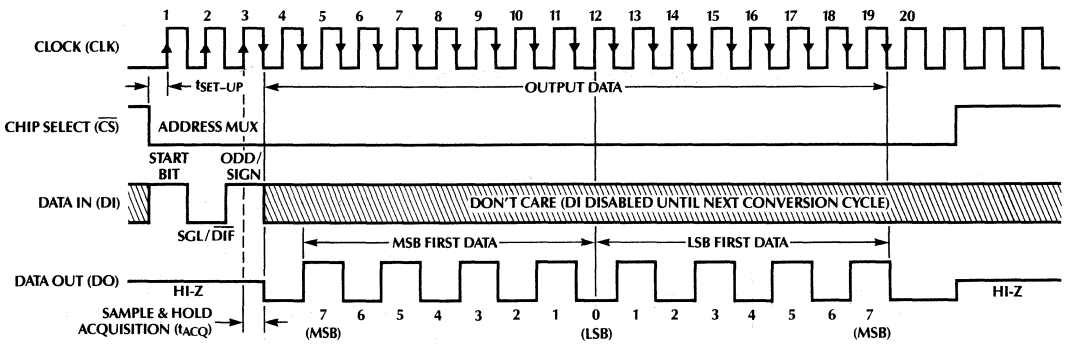
Figure 2. Timing Diagrams

ML2281 Timing



*LSB FIRST OUTPUT NOT AVAILABLE ON ML2281

ML2282 Timing



ML2284 Timing

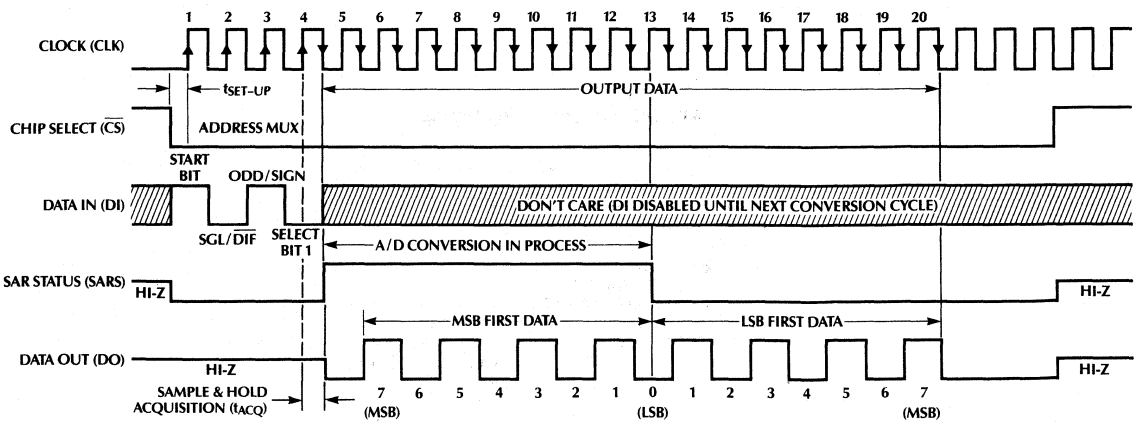
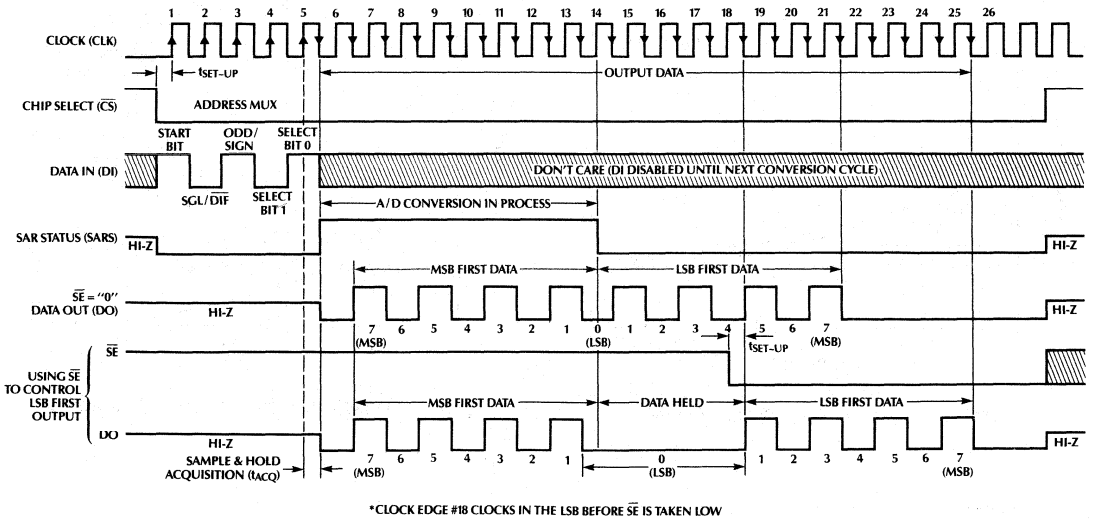


Figure 2. Timing Diagrams (Continued)

ML2288 Timing



*CLOCK EDGE #18 CLOCKS IN THE LSB BEFORE SE IS TAKEN LOW

Figure 2. Timing Diagrams (Continued)

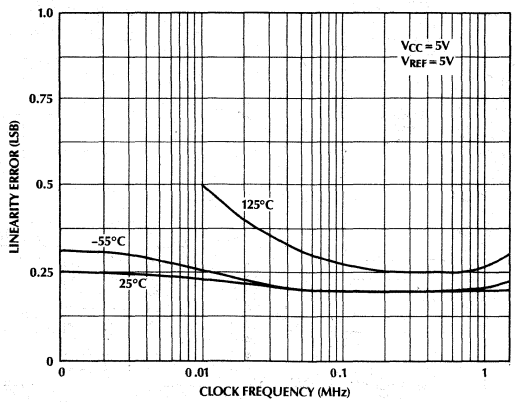


Figure 3. Linearity Error vs f_{CLK}

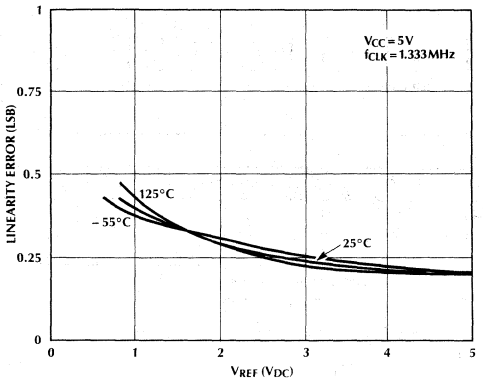


Figure 4. Linearity Error vs V_{REF} Voltage

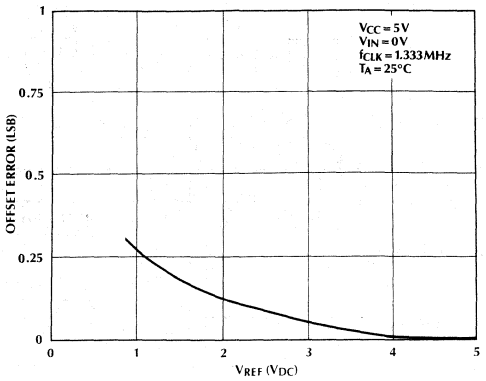
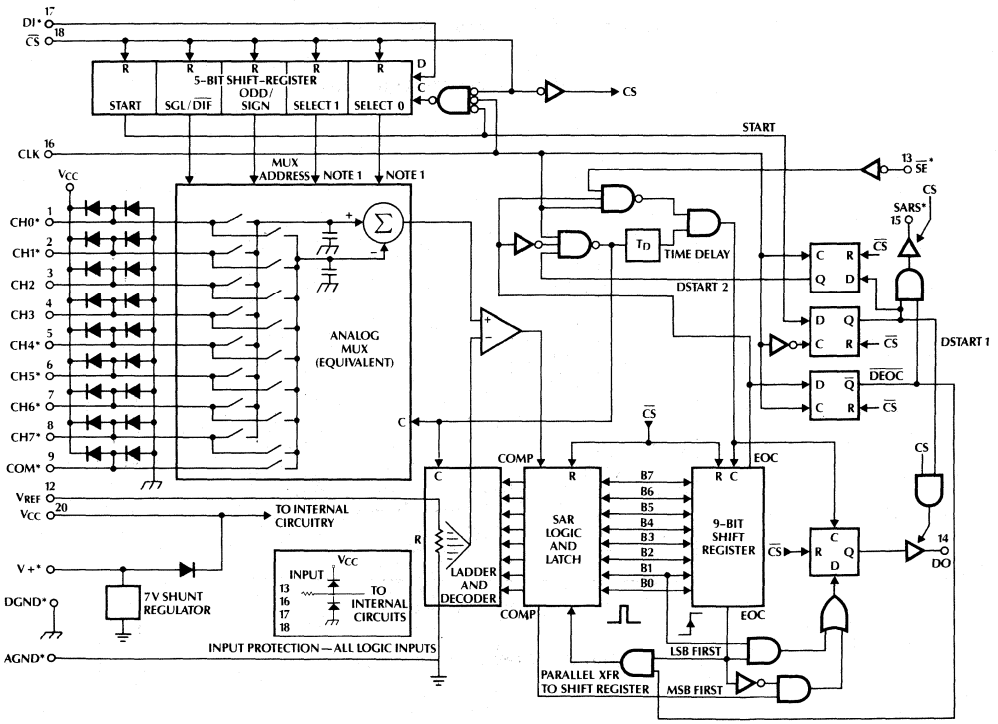


Figure 5. Unadjusted Offset Error vs V_{REF} Voltage



*SOME OF THESE FUNCTIONS/PINS ARE NOT AVAILABLE WITH OTHER OPTIONS.
NOTE 1: FOR THE ML2284 DI IS INPUT DIRECTLY TO THE D INPUT OF SELECT 1. SELECT 0 IS FORCED TO A "1". FOR THE ML2282, DI IS INPUT DIRECTLY TO THE D INPUT OF ODD/SIGN. SELECT 0 IS FORCED TO A "1" AND SELECT 1 IS FORCED TO A "0".

Figure 6. ML2288 Functional Block Diagram

1.0 FUNCTIONAL DESCRIPTION

1.1 Multiplexer Addressing

The design of these converters utilizes a sample data comparator structure which provides for a differential analog input to be converted by a successive approximation routine.

The actual voltage converted is always the difference between an assigned "+" input terminal and a "−" input terminal. The polarity of each input terminal of the pair being converted indicates which line the converter expects to be the most positive. If the assigned "+" input is less than the "−" input, the converter responds with an all zeros output code.

A unique input multiplexing scheme has been utilized to provide multiple analog channels with software configurable single ended, differential, or pseudo differential options. The pseudo differential option will convert the difference between the voltage at any analog input and a common terminal. One converter package can now accomodate ground referenced inputs and true differential inputs as well as signals with some arbitrary reference voltage.

A particular input configuration is assigned during the MUX addressing sequence, prior to the start of a conversion. The MUX address selects which of the analog inputs are to be enabled and whether this input is single ended or differential. In the differential case, it also assigns the polarity of the analog channels. Differential inputs are restricted to adjacent channel pairs. For example, channel 0 and channel 1 may be selected as a different pair but channel 0 or channel 1 cannot act differentially with any other channel. In addition to selecting the differential mode, the sign may also be selected. Channel 0 may be selected as the positive input and channel 1 as the negative input or vice versa. This programmability is illustrated by the MUX addressing codes shown in *Tables 1, 2, and 3*.

The MUX address is shifted into the converter via the DI input. Since the ML2281 contains only one differential input channel with a fixed polarity assignment, it does not require addressing.

The common input line on the ML2288 can be used as a pseudo differential input. In this mode, the voltage on the COM pin is treated as the "−" input for any of the other input channels. This voltage does not have to be analog ground; it can be any reference potential which is common to all of the inputs. This feature is most useful in single supply applications where the analog circuitry may be biased at a potential other than ground and the output signals are all referred to this potential.

Since the input configuration is under software control, it can be modified, as required, at each conversion. A channel can be treated as a single-ended, ground referenced input for one conversion; then it can be reconfigured as part of a differential channel for another conversion. *Figure 7* illustrates these different input modes.

Table 1. ML2288 MUX Addressing 8 Single-Ended or 4 Differential Channels

Single-Ended MUX Mode

MUX Address				Analog Single-Ended Channel #								
SGL/$\overline{\text{DIF}}$	ODD/SIGN	SELECT 1	SELECT 0	0	1	2	3	4	5	6	7	COM
1	0	0	0	+								−
1	0	0	1			+						−
1	0	1	0					+				−
1	0	1	1							+		−
1	1	0	0		+							−
1	1	0	1				+					−
1	1	1	0						+			−
1	1	1	1								+	−

Differential MUX Mode

MUX Address				Analog Differential Channel-Pair #							
				0		1		2		3	
SGL/$\overline{\text{DIF}}$	ODD/SIGN	SELECT 1	SELECT 0	0	1	2	3	4	5	6	7
0	0	0	0	+	−						
0	0	0	1			+	−				
0	0	1	0					+	−		
0	0	1	1							+	−
0	1	0	0	−	+						
0	1	0	1			−	+				
0	1	1	0					−	+		
0	1	1	1							−	+

Table 2. ML2284 MUX Addressing 4 Single-Ended or 2 Differential Channel

Single-Ended MUX Mode

MUX Address			Channel #			
SGL/$\overline{\text{DIF}}$	ODD/SIGN	SELECT 1	0	1	2	3
1	0	0	+			
1	0	1			+	
1	1	0		+		
1	1	1				+

COM is internally tied to A GND

Differential MUX Mode

MUX Address			Channel #			
SGL/$\overline{\text{DIF}}$	ODD/SIGN	SELECT 1	0	1	2	3
0	0	0	+	−		
0	0	1			+	−
0	1	0	−	+		
0	1	1			−	+

Table 3. ML2282 MUX Addressing 2 Single-Ended or 1 Differential Channel

Single-Ended MUX Mode

MUX Address		Channel #	
SGL/$\overline{DIF}$	ODD/SIGN	0	1
1	0	+	
1	1		+

COM is internally tied to GND

Differential MUX Mode

MUX Address		Channel #	
SGL/$\overline{DIF}$	ODD/SIGN	0	1
0	0	+	–
0	1	–	+

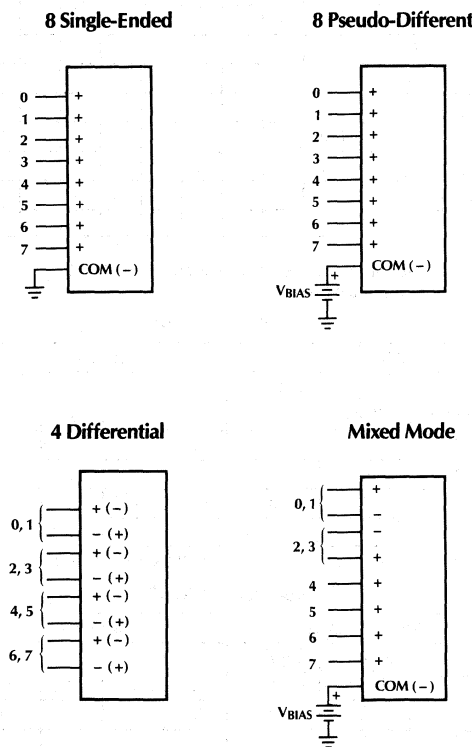


Figure 7. Analog Input Multiplexer Functional Options for ML2288

1.2 Digital Interface

The block diagram and timing diagrams in *Figures 2-5* illustrate how a conversion sequence is performed.

A conversion is initiated when $\overline{CS}$ is pulsed low. This line must be held low for the entire conversion. The converter is now waiting for a start bit and its MUX assignment word.

A clock is applied to the CLK input. On each rising edge of the clock, the data on DI is clocked into the MUX address shift register. The start bit is the first logic "1" that appears on the DI input (all leading edge zeros are ignored). After the start bit, the device clocks in the next 2 to 4 bits for the MUX assignment word.

When the start bit has been shifted into the start location of the MUX register, the input channel has been assigned and a conversion is about to begin. An interval of 1/2 clock period is used for sample & hold settling through the selected MUX channels. The SAR status output goes high at this time to signal that a conversion is now in progress and the DI input is ignored.

The DO output comes out of High impedance and provides a leading zero for this one clock period.

When the conversion begins, the output of the comparator, which indicates whether the analog input is greater than or less than each successive voltage from the internal DAC, appears at the DO output on each falling edge of the clock. This data is the result of the conversion being shifted out (with MSB coming first) and can be read by external logic or μP immediately.

After 8 clock periods, the conversion is completed. The SAR status line returns low to indicate this 1/2 clock cycle later.

The serial data is always shifted out MSB first during the conversion. After the conversion has been completed, the data can be shifted out a second time with LSB first, depending on level of $\overline{SE}$ input. For the case of ML2288, if $\overline{SE}$ = 1, the data is shifted out MSB first during the conversion only. If $\overline{SE}$ is brought low before the end of conversion (which is signalled by the high to low transition of SARS), the data is shifted out again immediately after the end of conversion; this time LSB first. If $\overline{SE}$ is brought low after end of conversion, the LSB first data is shifted out on falling edges of clock after $\overline{SE}$ goes low. For ML2282 and 2284, $\overline{SE}$ is internally tied low, so data is shifted out MSB first, then shifted out a second time LSB first at end of conversion. For ML2281, $\overline{SE}$ is internally tied high, so data is shifted out only once MSB first.

All internal registers are cleared when the $\overline{CS}$ input is high. If another conversion is desired, $\overline{CS}$ must make a high to low transition followed by address information.

The DI input and DO output can be tied together and controlled through a bidirectional μP I/O bit with one connection. This is possible because the DI input is only latched in during the MUX addressing interval while the DO output is still in the high impedance state.

1.3 Reference

The voltage applied to the reference input to these converters defines the voltage span of the analog input (the difference between V_{IN}max and V_{IN}min) over which the 256 possible output codes apply. The devices can be used in either ratiometric applications or in systems requiring absolute accuracy. The reference pin must be connected to a voltage source capable of driving the reference input resistance, typically 10k. This pin is the top of a resistor divider string used for the successive approximation conversion.

In a ratiometric system, the analog input voltage is proportional to the voltage used for the A/D reference. This voltage is typically the system power supply, so the V_{REF} pin can be tied to V_{CC}. This technique relaxes the stability requirements of the system reference as the analog input and A/D reference move together maintaining the same output code for a given input condition.

For absolute accuracy, where the analog input varies between specific voltage limits, the reference pin can be biased with a time and temperature stable voltage source.

The maximum value of the reference is limited to the V_{CC} supply voltage. The minimum value, however, can be quite small to allow direct conversion of inputs with less than 5 volts of voltage span. Particular care must be taken with regard to noise pickup, circuit layout and system error voltage sources when operating with a reduced span due to the increased sensitivity of the converter.

1.4 Analog Inputs and Sample/Hold

An important feature of the ML2281 family of devices is that they can be located at the source of the analog signal and then communicate with a controlling μP with just a few wires. This avoids bussing the analog inputs long distances and thus reduces noise pickup on these analog lines. However, in some cases, the analog inputs have a large common mode voltage or even some noise present along with the valid analog signal.

The differential input of these converters reduces the effects of common mode input noise. Thus, if a common mode voltage is present on both "+" and "−" inputs, such as 60Hz, the converter will reject this common mode voltage since it only converts the difference between "+" and "−" inputs.

The ML2281 family have a true sample and hold circuit which samples both "+" and "−" inputs simultaneously. This simultaneous sampling with a true S/H will give common mode rejection and AC linearity performance that is superior to devices where the two input terminals are not sampled at the same instant and where true sample and hold capability does not exist. Thus, the ML2281 family of devices can reject AC common mode signals from DC-50kHz as well as maintain linearity for signals from DC-50kHz.

The signal at the analog input is sampled during the interval when the sampling switch is closed prior to conversion start. The sampling window (S/H acquisition time) is 1/2 CLK period wide and occurs 1/2 CLK period before DO goes from high impedance to active low state. When the sampling switch closes at the start of the S/H acquisition time, 8pF of capacitance is thrown onto the analog input. 1/2 CLK period later, the sampling switch is opened and the signal present at the analog input is stored. Any error on the analog input at the end of the S/H acquisition time will cause additional conversion error. Care should be taken to allow adequate charging or settling time from the source. If more charging or settling time is needed to reduce these analog input errors, a longer CLK period can be used.

The ML2281X family has improved latchup immunity. Each analog input has dual diodes to the supply rails, and a minimum of +/− 25mA (+/−100mA typically) can be injected into each analog input without causing latchup.

1.5 Dynamic Performance

Signal-to-Noise-Ratio

Signal-to-noise ratio (SNR) is the measured signal-to-noise at the output of the converter. The signal is the RMS magnitude of the fundamental. Noise is the RMS sum of all the nonfundamental signals up to half the sampling frequency. SNR is dependent on the number of quantization levels used in the digitization process; the more levels, the smaller the quantization noise. The theoretical SNR for a sine wave is given by

$$SNR = (6.02N + 1.76)\,dB$$

where N is the number of bits. Thus for ideal 8-bit converter, SNR = 49.92dB.

Harmonic Distortion

Harmonic distortion is the ratio of the RMS sum of harmonics to the fundamental. Total harmonic distortion (THD) of the ML2281 Series is defined as

$$20 \log \frac{(V_2^2 + V_3^2 + V_4^2 + V_5^2)^{1/2}}{V_1}$$

where V_1 is the RMS amplitude of the fundamental and V_2, V_3, V_4, V_5 are the RMS amplitudes of the individual harmonics.

Intermodulation Distortion

With inputs consisting of sine waves at two frequencies, f_A and f_B, any active device with nonlinearities will create distortion products, of order (m+n), at sum and difference frequencies of $mf_A + nf_B$, where m, n = 0, 1, 2, 3,... . Intermodulation terms are those for which m or n is not equal to zero. The (IMD) intermodulation distortion specification includes the second order terms ($f_A + f_B$) and ($f_A - f_B$) and the third order terms ($2f_A + f_B$), ($2f_A - f_B$), ($f_A + 2f_B$) and ($f_A - 2f_B$) only.

1.6 Zero Error Adjustment

The zero of the A/D does not require adjustment. If the minimum analog input voltage value, V_{IN}min is not ground, a zero offset can be done. The converter can be made to output 00000000 digital code for this minimum input voltage by biasing any $V_{IN}-$ input at this V_{IN} min value. This utilizes the differential mode operation of the A/D.

2

The zero error of the A/D converter relates to the location of the first riser of the transfer function and can be measured by grounding the $V_{IN}-$ input and applying a small magnitude positive voltage to the $V_{IN}+$ input. Zero error is the difference between the actual DC input voltage which is necessary to just cause an output digital code transition from 00000000 to 00000001 and the ideal 1/2 LSB value (1/2 LSB = 9.8 mV for $V_{REF} = 5.000 V_{DC}$).

1.7 Full-Scale Adjustment

The full-scale adjustment can be made by applying a differential input voltage which is 1 1/2 LSB down from the desired analog full-scale voltage range and then adjusting the magnitude of the V_{REF} input or V_{CC} for a digital output code which is just changing from 11111110 to 11111111.

1.8 Adjustment for an Arbitrary Analog Input Voltage Range

If the analog zero voltage of the A/D is shifted away from ground (for example, to accommodate an analog input signal which does not go to ground), this new zero reference should be properly adjusted first. A $V_{IN}+$ voltage which equals this desired zero reference plus 1/2 LSB (where the LSB is calculated for the desired analog span, 1 LSB = analog span/256) is applied to selected "+" input and the zero reference voltage at the corresponding "−" input should then be adjusted to just obtain the 00000000 to 00000001 code transition.

The full-scale adjustment should be made by forcing a voltage to the $V_{IN}+$ input which is given by:

$V_{IN}+$ fs adjust = Vmax − 1.5*[(Vmax-Vmin)/256]
where Vmax = high end of the analog input range
Vmin = low end (offset zero) of the analog range

The V_{REF} or V_{CC} voltage is then adjusted to provide a code change from 11111110 to 11111111.

1.9 Shunt Regulator

A unique feature of ML2288 and ML2284 is the inclusion of a shunt regulator connected from V+ terminal to ground which also connects to the V_{CC} terminal (which is the actual converter supply) through a silicon diode as shown in *Figure 8*. When the regulator is turned on, the V+ voltage is clamped at 11 V_{BE} set by the internal resistor ratio. The typical I-V curve of the shunt regulator is shown in *Figure 9*. It should be noted that before V+ voltage is high enough to turn on the shunt regulator (which occurs at about 5.5 V), 35 kΩ of resistance is observed between V+ and GND. When the shunt regulator is not used, V+ pin should be either left floating or tied to GND. The temperature coefficient of the regulator is −22 mV/°C.

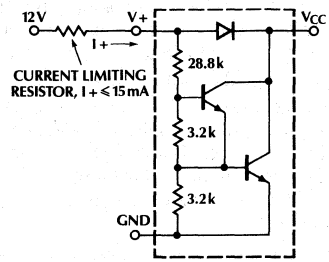


Figure 8. Shunt Regulator

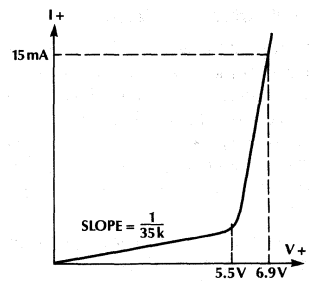
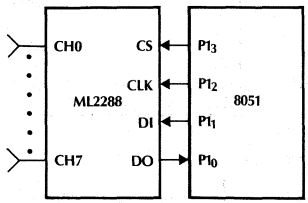


Figure 9. I-V Characteristic of the Shunt Regulator

2.0 APPLICATIONS

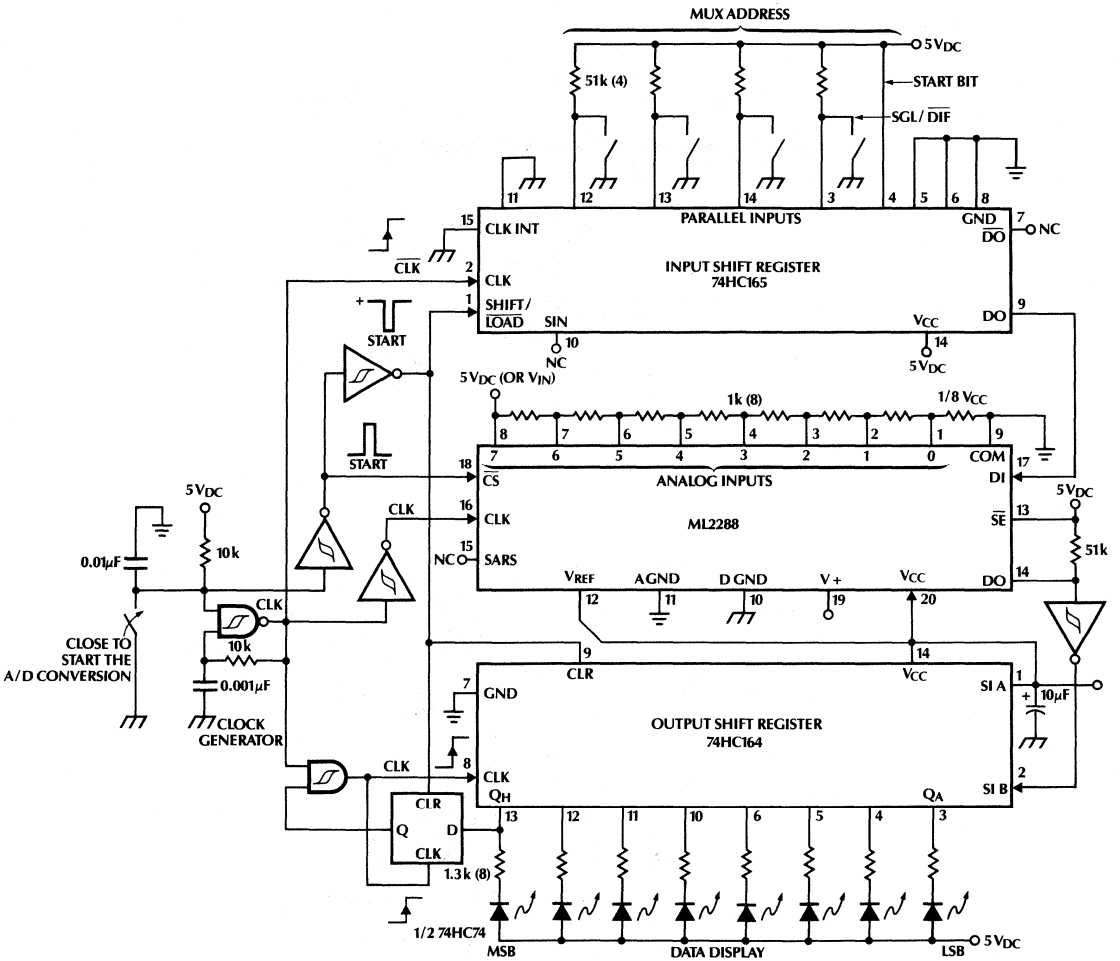
8051 Interface and Controlling Software



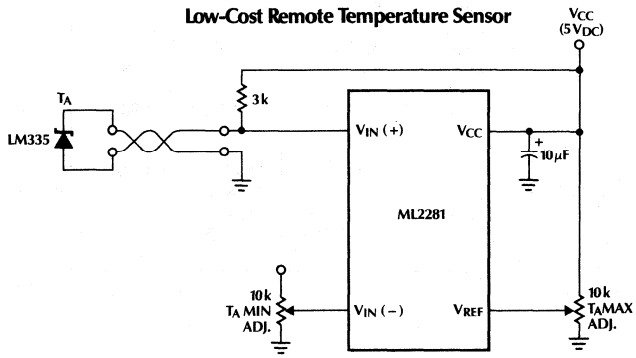
Mnemonic			Instruction
START	ANL	P1, #0F7H	;SELECT A/D (CS = 0)
	MOV	B, #5	;BIT COUNTER ← 5
	MOV	A, #ADDR	;A ← MUX BIT
LOOP 1:	RRC	A	;CY ← ADDRESS BIT
	JC	ONE	;TEST BIT ;BIT = 0
ZERO:	ANL	P1, #0FEH	;DI ← 0
	SJMP	CONT	;CONTINUE ;BIT = 1
ONE:	ORL	P1, #1	;D1 ← 1
CONT:	ACALL	PULSE	;PULSE SK 0 → 1 → 0
	DJNZ	B, LOOP 1	;CONTINUE UNTIL DONE
	ACALL	PULSE	;EXTRA CLOCK FOR SYNC
	MOV	B, #8	;BIT COUNTER ← 8
LOOP 2:	ACALL	PULSE	;PULSE SK 0 → 1 → 0
	MOV	A, P1	;CY ← DO
	RRC	A	
	RRC	A	
	MOV	A, C	;A ← RESULT
	RLC	A	;A(0) ← BIT AND SHIFT
	MOV	C, A	;C ← RESULT
	DJNZ	B, LOOP 2	;CONTINUE UNTIL DONE
RETI			
			;PULSE SUBROUTINE
PULSE:	ORL	P1, #04	;SK ← 1
	NOP		;DELAY
	ANL	P1, #0FBH	;SK ← 0
	RET		

APPLICATIONS (Continued)

ML2288 "Stand-Alone" or Evaluation Circuit

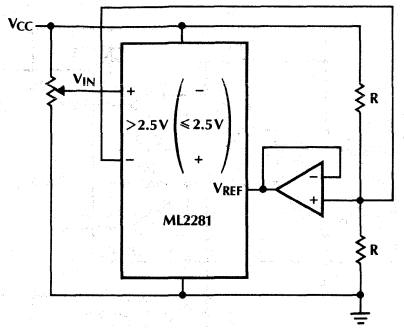


Low-Cost Remote Temperature Sensor



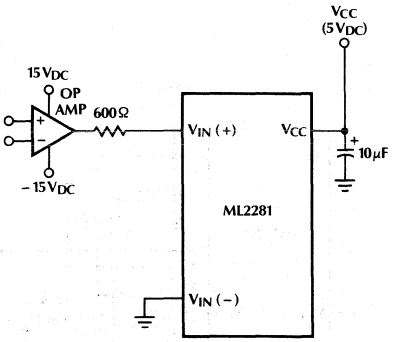
APPLICATIONS (Continued)

Obtaining 9-Bit Resolution



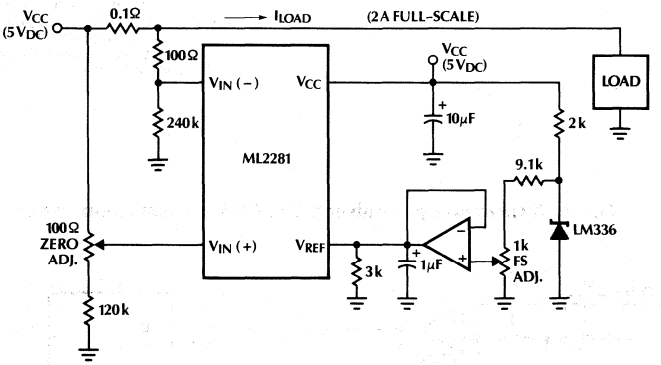
CONTROLLER PERFORMS A ROUTINE TO DETERMINE WHICH INPUT POLARITY PROVIDES A NON-ZERO OUTPUT CODE. THIS INFORMATION PROVIDES THE EXTRA BITS.

Protecting the Input

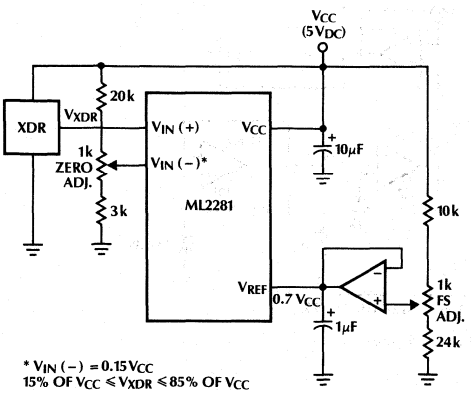


DIODE CLAMPING IS NOT NEEDED IF CURRENT IS LIMITED TO 25mA

Digitizing a Current Flow

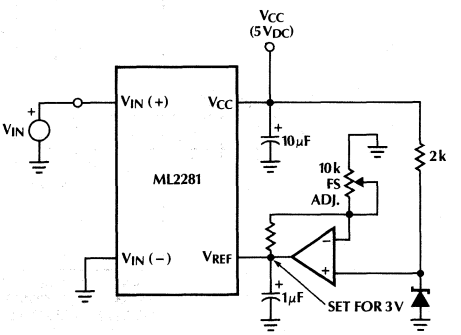


Operating with Ratiometric Transducers



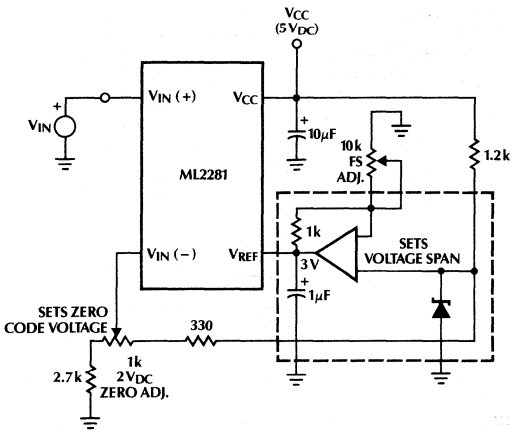
* $V_{IN}(-) = 0.15V_{CC}$
$15\% \text{ OF } V_{CC} \leq V_{XDR} \leq 85\% \text{ OF } V_{CC}$

Span Adjust: $0V \leq V_{IN} \leq 3V$

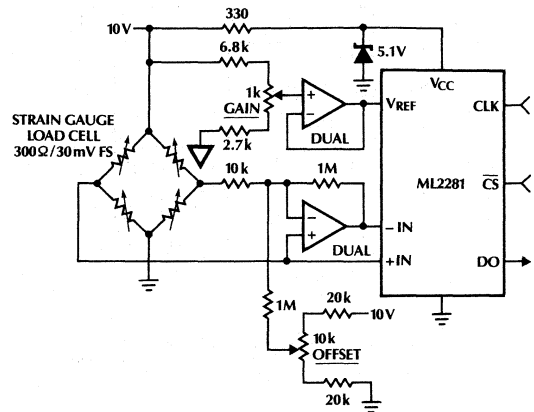


APPLICATIONS (Continued)

Zero-Shift and Span Adjust: $2V \leq V_{IN} \leq 5V$

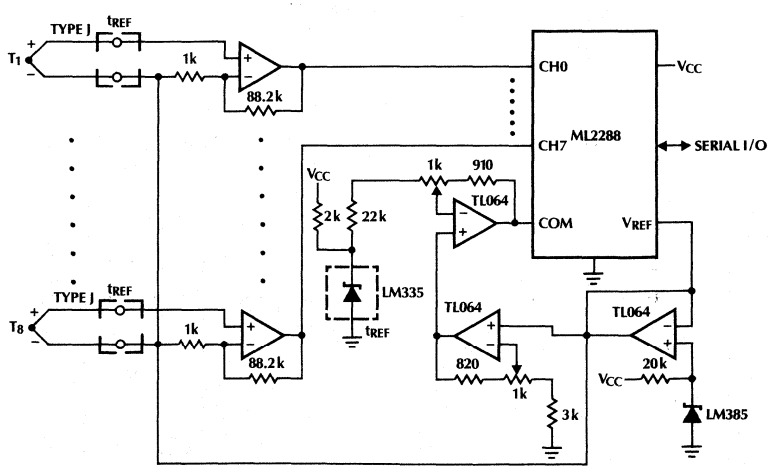


Digital Load Cell



- USES ONE MORE WIRE THAN LOAD CELL ITSELF
- TWO MINI-DIPs COULD BE MOUNTED INSIDE LOAD CELL FOR DIGITAL OUTPUT TRANSDUCER
- ELECTRONIC OFFSET AND GAIN TRIMS RELAX MECHANICAL SPECS FOR GAUGE FACTOR AND OFFSET
- LOW LEVEL CELL OUTPUT IS CONVERTED IMMEDIATELY FOR HIGH NOISE IMMUNITY

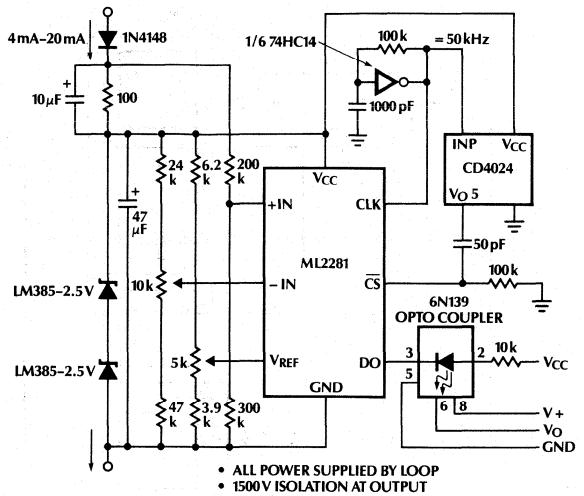
Convert 8 Thermocouples with only One Cold-Junction Compensator



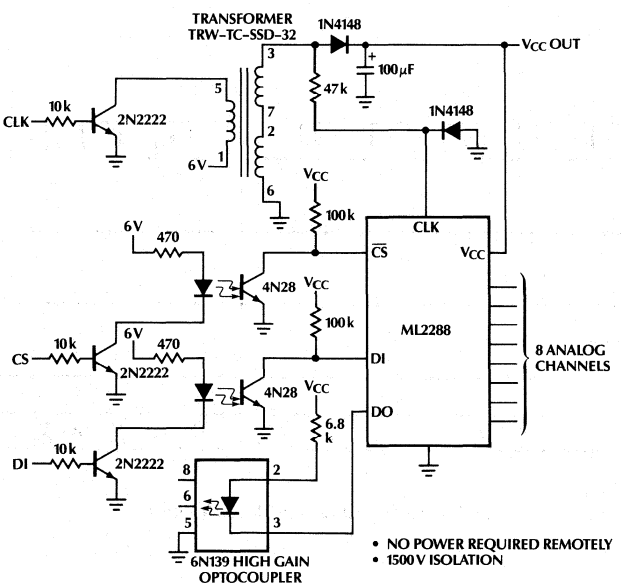
USES THE PSEUDO-DIFFERENTIAL MODE TO KEEP THE DIFFERENTIAL INPUTS CONSTANT WITH CHANGES IN REFERENCE TEMPERATURE (T_{REF}).

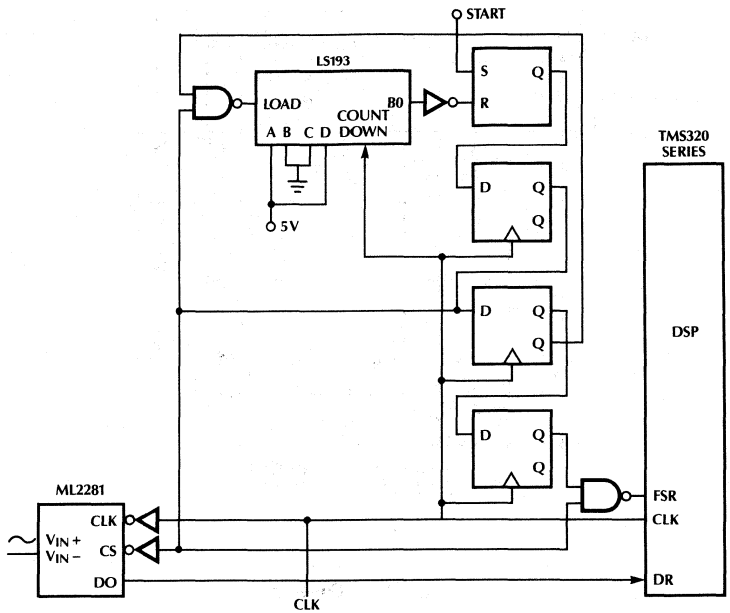
APPLICATIONS (Continued)

4 mA–20 mA Current Loop Converter

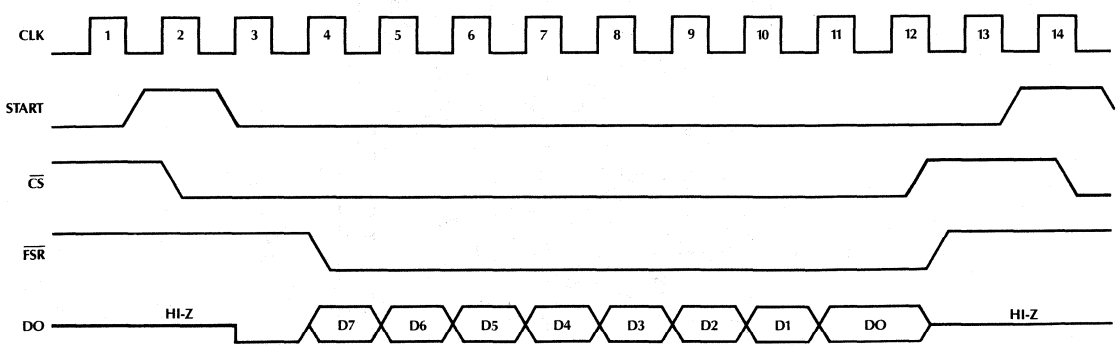


Isolated Data Converter





SAMPLING RATE 111kHz, DATA RATE 1.33MHz



Interfacing ML2281 to TMS320 Series

ORDERING INFORMATION

PART NUMBER	ALTERNATE PART NUMBER	TOTAL UNADJUSTED ERROR	TEMPERATURE RANGE	PACKAGE
SINGLE ANALOG INPUT, 8-PIN PACKAGE				
ML2281BMJ	ADC0831BJ	±½LSB	−55°C to +125°C	HERMETIC DIP
ML2281BIJ	ADC0831BCJ		−40°C to +85°C	HERMETIC DIP
ML2281BCP	ADC0831BCN		0° to +70°C	MOLDED DIP
ML2281CIJ	ADC0831CCJ	±1LSB	−40°C to +85°C	HERMETIC DIP
ML2281CCP	ADC0831CCN		0°C to +70°C	MOLDED DIP
TWO ANALOG INPUTS, 8-PIN PACKAGE				
ML2282BMJ	ADC0832BJ	±½LSB	−55°C to +125°C	HERMETIC DIP
ML2282BIJ	ADC0832BCJ		−40°C to +85°C	HERMETIC DIP
ML2282BCP	ADC0832BCN		0°C to +70°C	MOLDED DIP
ML2282CIJ	ADC0832CCJ	±1LSB	−40°C to +85°C	HERMETIC DIP
ML2282CCP	ADC0832CCN		0°C to +70°C	MOLDED DIP
FOUR ANALOG INPUTS, 14-PIN PACKAGE				
ML2284BMJ	ADC0834BJ	±½LSB	−55°C to +125°C	HERMETIC DIP
ML2284BIJ	ADC0834BCJ		−40°C to +85°C	HERMETIC DIP
ML2284BCP	ADC0834BCN		0° to +70°C	MOLDED DIP
ML2284CIJ	ADC0834CCJ	±1LSB	−40°C to +85°C	HERMETIC DIP
ML2284CCP	ADC0834CCN		0°C to +70°C	MOLDED DIP
EIGHT ANALOG INPUTS, 20-PIN PACKAGE				
ML2288BMJ	ADC0838BJ	±½LSB	−55°C to +85°C	HERMETIC DIP
ML2288BIJ	ADC0838BCJ		−40°C to +85°C	HERMETIC DIP
ML2288BCP	ADC0838BCN		0°C to +70°C	MOLDED DIP
ML2288BCQ	ADC0838BCV		0°C to +70°C	MOLDED DIP (PCC)
ML2288CIJ	ADC0838CCJ	±1LSB	−40°C to +85°C	HERMETIC DIP
ML2288CCP	ADC0838CCN		0°C to +70°C	MOLDED DIP
ML2288CCQ	ADC0838CCV		0°C to +70°C	MOLDED DIP (PCC)

Micro Linear

ML2340, ML2350

Single Supply, Programmable 8-Bit D/A Converters

GENERAL DESCRIPTION

The ML2340 and ML2350 are CMOS voltage output, 8-bit D/A converters with an internal voltage reference and a μP interface. These devices are designed to be powered by a single supply, although they can be powered from dual power supplies. The output voltage swings above zero scale (V_{ZS}) in the unipolar mode or around zero scale (V_{ZS}) in the bipolar mode, both with programmable gain. V_{ZS} can be set to any voltage from AGND to 2.25V below V_{CC}. The digital and analog grounds, DGND and AGND, are totally independent of each other. DGND can be set to any voltage from AGND to 4.5V below V_{CC} for easy interfacing to standard TTL and CMOS logic families.

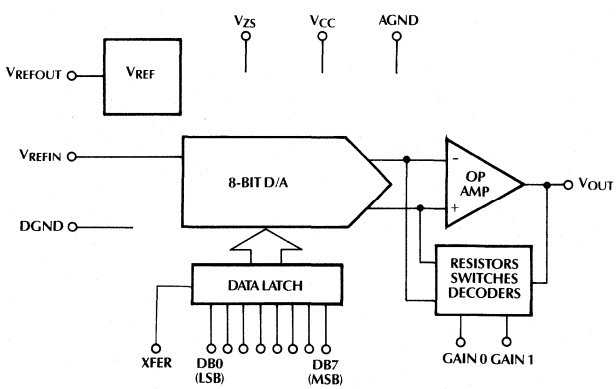
The high level of integration and versatility of the ML2340 and ML2350 makes them ideal for a wide range of applications in hard disk drives, automotive, telecom, and a variety of general purpose industrial. One specific intended application is controlling a hard disk voice coil.

The internal reference of the ML2340 provides a 2.25V or 4.50V output for use with A/D converters that use a single 5V ± 10% power supply, while the ML2350 provide a 2.50V or 5.00V reference output.

FEATURES

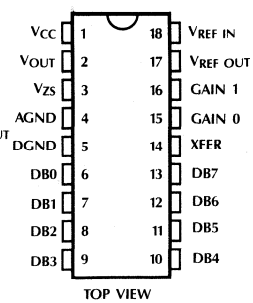
- Programmable output voltage gain settings of 2, 1, ½, ¼ provide 8-, 9-, 10-, or 11-bit effective resolution around zero
- AGND to V_{CC} output voltage swing
- Bipolar or unipolar output voltage
- 4.5V to 13.2V single supply or ±2.25V to ±6.5V dual-supply operation
- Transparent latch allows microprocessor interface with 30ns setup time
- Data flow through mode
- Voltage reference output
  - ML2340 ..... 2.25V or 4.50V
  - ML2350 ..... 2.50V or 5.00V
- Nonlinearity ..... ±¼ LSB or ±½ LSB
- Output voltage settling time over temperature and supply voltage tolerance
  - Within 1V of V_{CC} and AGND ..... 2.5μs max
  - Within 100mV of V_{CC} and AGND ..... 5μs max
- TTL and CMOS compatible digital inputs
- Low supply current (5V supply) ..... 5mA max
- 18-pin DIP or surface mount SOIC
- Operating temperature range of 0°C to +70°C, –40°C to +85°C, and –55°C to +125°C

BLOCK DIAGRAM



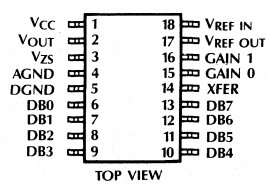
PIN CONNECTIONS

ML2340 ML2350 18-Pin DIP



TOP VIEW

ML2340 ML2350 18-Pin SOIC



TOP VIEW

PIN DESCRIPTION

PIN #	NAME	FUNCTION
1	V_{CC}	Positive supply.
2	V_{OUT}	Voltage output of the D/A converter. V_{OUT} is referenced to V_{ZS}.
3	V_{ZS}	Zero Scale Voltage. V_{OUT} is referenced to V_{ZS}. V_{ZS} is normally tied to AGND in the unipolar mode or to mid-supply in the bipolar mode. When the device is operated from a single power supply, V_{ZS} has a maximum current requirement of –300μA in the bipolar mode.
4	AGND	Analog ground.
5	DGND	Digital ground. This is the ground reference level for all digital inputs. The range is AGND < (V_{CC} – 4.5V). DGND is normally tied to system ground.
6	DB0	Data input — Bit 0 (LSB).
7	DB1	Data input — Bit 1.
8	DB2	Data input — Bit 2.
9	DB3	Data input — Bit 3.
10	DB4	Data input — Bit 4.
11	DB5	Data input — Bit 5.
12	DB6	Data input — Bit 6.
13	DB7	Data input — Bit 7 (MSB).
14	XFER	Transfer enable input. The data is transferred into the transparent latch at the high level of XFER.
15	GAIN 0	Digital gain setting input 0.
16	GAIN 1	Digital gain setting input 1.
17	$V_{REF\ OUT}$	Voltage reference output. $V_{REF\ OUT}$ is referenced to AGND. $V_{REF\ OUT}$ is set to 2.5V and 5.0V in a low-voltage and high-voltage operation, respectively for the ML2350; 2.25V and 4.5V for the ML2340.
18	$V_{REF\ IN}$	Voltage reference input. $V_{REF\ IN}$ is referenced to AGND.

ABSOLUTE MAXIMUM RATINGS
(Note 1)

Supply Voltage V_{CC} with Respect to AGND 14.2V
DGND ..... –0.3V to V_{CC} + 0.3V
V_{ZS}, $V_{REF\ IN}$ ..... –0.3V to V_{CC} + 0.3V
Logic Inputs ..... –0.3V to V_{CC} + 0.3V
Input Current per Pin (Note 2) ..... ±25mA
Storage Temperature ..... –65°C to +150°C
Package Dissipation at T_A = 25°C (Board Mount) 875mW
Lead Temperature (Soldering 10 sec.)
Dual-In-Line Package (Molded) ..... 260°C
Dual-In-Line Package (Ceramic) ..... 300°C
Molded Small Outline IC Package
Vapor Phase (60 sec.) ..... 215°C
Infrared (15 sec.) ..... 220°C

OPERATING CONDITIONS
(Note 1)

Supply Voltage, V_{CC} ..... $4.5V_{DC}$ to $13.2V_{DC}$
Temperature Range (Note 3) ..... $T_{MIN} \leq T_A \leq T_{MAX}$
ML2340BMJ, ML2340CMJ
ML2350BMJ, ML2350CMJ ..... –55°C to +125°C
ML2340BIJ, ML2340CIJ
ML2350BIJ, ML2350CIJ ..... –40°C to +85°C
ML2340BCP, ML2340CCP
ML2350BCP, ML2350CCP
ML2340BCS, ML2340CCS
ML2350BCS, ML2350CCS ..... 0°C to +70°C

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, $T_A = T_{MIN}$ to T_{MAX}, V_{CC} – AGND = 5V ± 10% and 12V ± 10%, $V_{REF\ IN}$ for ML2340 = 2.25V and 4.50V, for ML2350 $V_{REF\ IN}$ = 2.50V and 5.00V, V_{OUT} load is R_L = 1K and C_L = 100pF, V_{REF} load is R_L = 1K and C_L = 100pF and input control signals with $t_R = t_F \leq 20$ns.

PARAMETER	NOTES	CONDITIONS	ML2340XCX, ML2350XCX			ML2340XIX, ML2340XMX ML2350XIX, ML2350XMX			UNITS
			MIN	TYP (Note 4)	MAX	MIN	TYP (Note 4)	MAX	
Converter and Programmable Gain Amplifier									
Converter Resolution	5		8			8			Bits
Integral Linearity Error ML2340BXX, ML2350BXX ML2340CXX, ML2350CXX	5	GAIN = 2, 1, ½, or ¼			 ±¼ ±½			 ±¼ ±½	 LSB LSB
Differential Linearity Error ML2340BXX, ML2350BXX ML2340CXX, ML2350CXX	5	GAIN = 2, 1, ½, or ¼			 ±¼ ±½			 ±¼ ±½	 LSB LSB
Mode Select Unipolar Output Bipolar Output	5	V_{ZS} with respect to AGND	 0 1.50		 1.0 V_{CC}–2.25	 0 1.50		 1.0 V_{CC}–2.25	 V V
Offset Error Unipolar Mode	5	Figure 1 GAIN = ¼, ½, 1 GAIN = 2			 ±10 ±20			 ±12 ±24	 mV mV
Bipolar Mode	5	Figure 1 GAIN = ¼, ½, 1, 2			±10 plus ±2½ LSB			±10 plus ±2½ LSB	mV
Gain Error Unipolar Mode Bipolar Mode	5	Figure 1 GAIN = ¼, ½, 1, 2 GAIN = ¼, ½, 1, 2		 ±.5 ±.5	 ±2 ±2		 ±.5 ±.5	 ±2.5 ±2.5	 %FS %FS
Reference									
$V_{REF\ OUT}$ Voltage ML2340BXX	5	 $V_{CC} \leq 7.0$V T_A = 25°C T_{MIN} to T_{MAX}	 2.23 2.22	 2.25	 2.27 2.28	 2.23 2.18	 2.25	 2.27 2.32	 V V
		$V_{CC} \geq 8.0$V T_A = 25°C T_{MIN} to T_{MAX}	4.48 4.46	4.50	4.52 4.54	4.48 4.43	4.50	4.52 4.57	V V
ML2340CXX		$V_{CC} \leq 7.0$V T_A = 25°C T_{MIN} to T_{MAX}	2.22 2.20	2.25	2.29 2.30	2.22 2.18	2.25	2.28 2.32	V V
		$V_{CC} \geq 8.0$V T_A = 25°C T_{MIN} to T_{MAX}	4.45 4.40	4.50	4.55 4.60	4.45 4.35	4.50	4.55 4.65	V V
ML2350BXX	5	$V_{CC} \leq 7.0$V T_A = 25°C T_{MIN} to T_{MAX}	2.48 2.47	2.50	2.52 2.53	2.48 2.43	2.50	2.52 2.57	V V
		$V_{CC} \geq 8.0$V T_A = 25°C T_{MIN} to T_{MAX}	4.98 4.96	5.00	5.02 5.04	4.98 4.90	5.00	5.02 5.10	V V
ML2350CXX		$V_{CC} \leq 7.0$V T_A = 25°C T_{MIN} to T_{MAX}	2.45 2.44	2.50	2.55 2.58	2.46 2.42	2.50	2.55 2.59	V V
		$V_{CC} \geq 8.0$V T_A = 25°C T_{MIN} to T_{MAX}	4.95 4.90	5.00	5.05 5.10	4.95 4.85	5.00	5.05 5.15	V V
Temperature Coefficient $V_{REF\ OUT}$				50			50		ppm/°C
V_{REF} Output Current	5		–1		5	–1		5	mA
$V_{REF\ OUT}$ Power Supply Rejection Ratio	5	100mV_{P-P}, 1kHz Sinewave on V_{CC}	–40	–60		–40	–60		dB

ELECTRICAL CHARACTERISTICS (Continued)

Unless otherwise specified, $T_A = T_{MIN}$ to T_{MAX}, V_{CC} - AGND = 5V ± 10% and 12V ± 10%, $V_{REF\ IN}$ for ML2340 = 2.25V and 4.50V; for ML2350 $V_{REF\ IN}$ = 2.50V and 5.00V, V_{OUT} load is R_L = 1K and C_L = 100pF, V_{REF} load is R_L = 1K and C_L = 100pF and input control signals with $t_R = t_F \leq 20ns$.

PARAMETER	NOTES	CONDITIONS	ML2340XCX, ML2350XCX			ML2340XIX, ML2340XMX ML2350XIX, ML2350XMX			UNITS
			MIN	TYP (Note 4)	MAX	MIN	TYP (Note 4)	MAX	
$V_{REF\ IN}$ and V_{ZS}									
$V_{REF\ IN}$ Input Range	5	$V_{CC} \leq 7.00V$	AGND+2		AGND+2.6	AGND+2		AGND+2.6	V
		$V_{CC} \geq 8.00V$	AGND+2		AGND+5.5	AGND+2		AGND+5.5	V
$V_{REF\ IN}$ DC Input Resistance	5		10			10			MΩ
V_{ZS} Voltage Range	5, 8		AGND		$V_{CC}/2 \times 1.1$	AGND		$V_{CC}/2 \times 1.1$	V
Analog Output									
V_{OUT} Output Swing Unipolar Mode	5, 8	R_L = 100K	AGND+0.01		$V_{CC}-.04$	AGND+0.01		$V_{CC}-.04$	V
		R_L = 1K	AGND+1.0		$V_{CC}-1.0$	AGND+1.0		$V_{CC}-1.0$	V
Bipolar Mode	5	R_L = 100K	AGND+0.1		$V_{CC}-0.1$	AGND+0.1		$V_{CC}-0.1$	V
		R_L = 1K	AGND+1.0		$V_{CC}-1.0$	AGND+1.0		$V_{CC}-1.0$	V
V_{OUT} Output Current	5	$AGND+1V<V_{OUT}<V_{CC}-1V$	-10		+10	-10		+10	mA
Power Supply Rejection Ratio		100mV$_{P-P}$, 1kHz sinewave on V_{CC}		-60			-60		dB
Digital and DC									
$V_{IN(0)}$ Logical "0" Input Voltage	5				0.8			0.8	V
$V_{IN(1)}$ Logical "1" Input Voltage	5		2.0			2.0			V
$I_{IN(0)}$ Logical "0" Input Current	5	V_{IN} = DGND	-1			-1			μA
$I_{IN(1)}$ Logical "1" Input Current	5	$V_{IN} = V_{CC}$			1			1	μA
Supply Current, Bipolar Mode									
I_{CC}, V_{CC} Current	5	V_{CC} = 5V ± 10%			5.3			5.3	mA
I_{AGND}, Analog Ground Current					-5.0			-5.0	mA
I_{VZS}, V_{ZS} Current				-90	-300		-90	-300	μA
I_{CC}, V_{CC} Current	5	V_{CC} = 12V ± 10%			9.3			9.3	mA
I_{AGND}, Analog Ground Current					-9.0			-9.0	mA
I_{VZS}, V_{ZS} Current				-90	-300		-90	-300	μA

ELECTRICAL CHARACTERISTICS (Continued)

Unless otherwise specified, $T_A = T_{MIN}$ to T_{MAX}, V_{CC} – AGND = 5V ± 10% and 12V ± 10%, $V_{REF\ IN}$ for ML2340 = 2.25V and 4.50V, for ML2350 $V_{REF\ IN}$ = 2.50V and 5.00V, V_{OUT} load is R_L = 1K and C_L = 100pF, V_{REF} load is R_L = 1K and C_L = 100pF and input control signals with $t_R = t_F \leq 20$ns.

PARAMETER	NOTES	CONDITIONS	ML2340XCX, ML2350XCX			ML2340XIX, ML2340XMX ML2350XIX, ML2350XMX			UNITS
			MIN	TYP (Note 4)	MAX	MIN	TYP (Note 4)	MAX	
Digital and DC (Continued)									
Supply Current, Unipolar Mode									
I_{CC}, V_{CC} Current	5	V_{CC} = 5V ± 10%			6.0			6.0	mA
I_{AGND}, Analog Ground Current					–4.3			–4.3	mA
I_{VZS}, V_{ZS} Current					–1.7			–1.7	mA
I_{CC}, V_{CC} Current	5	V_{CC} = 12V ± 10%			11.0			11.0	mA
I_{AGND}, Analog Ground Current					–7.3			–7.3	mA
I_{VZS}, V_{ZS} Current					–3.7			–3.7	mA
AC Performance									
Settling Time t_{S1}	5	Figure 2, Output Step of AGND + 1V to V_{CC} – 1V, R_L = 1K		1.2	2.5		1.2	3.0	µs
t_{S2}		Output Step of AGND + 100mV to V_{CC}–100mV, R_L = 100K		2.5	5		2.5	6	µs
t_{S3}		Output Step of ±1LSB			1			1	µs
t_{S4}, Gain Change		Change of Any Gain Setting		1.1	2.5		1.1		µs
t_{XFER}, XFER Pulse Width	5	Figure 3	60			60			ns
t_{DBS}, DB0–DB7 Setup Time	5	Figure 3	40			45			ns
t_{DBH}, DB0–DB7 Hold Time	5	Figure 3	0			0			ns
t_{RESET}, Power-On Reset Time	6				16			16	µs

Note 1: Absolute maximum ratings are limits beyond which the life of the integrated circuit may be impaired. All voltages unless otherwise specified are measured with respect to analog ground.

Note 2: When the voltage at any pin exceeds the power supply rails (V_{IN} < AGND or V_{IN} > V_{CC}) the absolute value of current at that pin should be limited to 25mA or less.

Note 3: –55°C to +125°C operating temperature range devices are 100% tested at temperature extremes with worst-case test conditions. –40°C to +85°C operating temperature range devices are 100% tested with temperature limits guaranteed by 100% testing, sampling, or by correlation with worst-case test conditions.

Note 4: Typicals are parametric norm at 25°C.

Note 5: Parameter guaranteed and 100% production tested.

Note 6: Parameter guaranteed. Parameters not 100% tested are not in outgoing quality level calculation.

Note 7: Supply current and analog ground current are specified with the digital inputs stable and no load on V_{OUT}.

Note 8: In unipolar operation with V_{ZS} and AGND tied together, digital codes that represent an analog value of less than 100mV from AGND should be avoided.

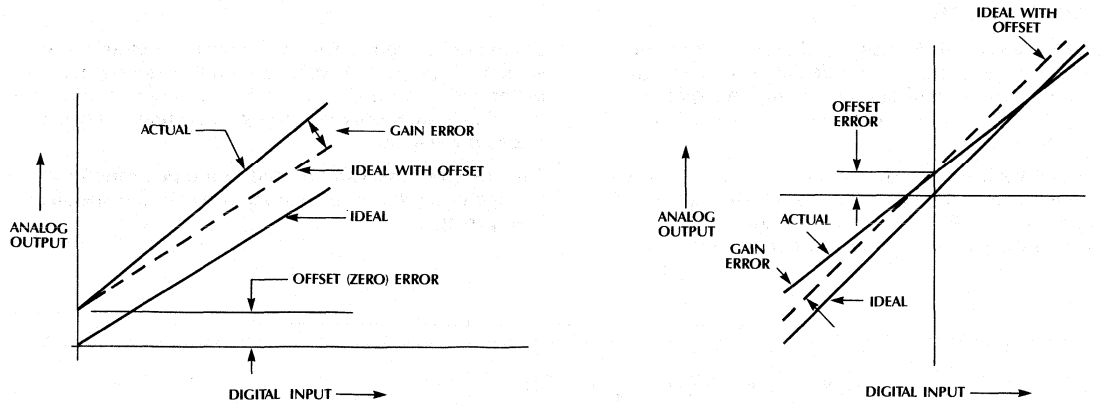


Figure 1. Gain and Offset Error

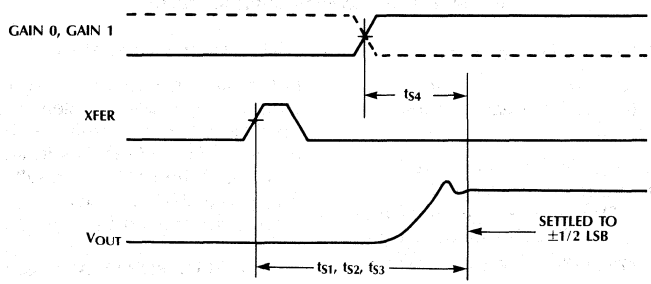


Figure 2. Settling Time

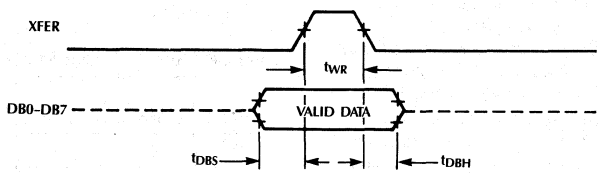


Figure 3. Single Buffered Mode

1.0 FUNCTIONAL DESCRIPTION

1.1 D/A CONVERTER

The D/A converter is implemented using an array of equal current sources that are decoded semi linearly for the four most significant bits to improve differential linearity and to reduce output glitch around major carries. See Figure 4.

The input voltage reference of the D/A converter is the difference between $V_{REF\ IN}$ and AGND. This difference voltage is converted to a reference current using an internal resistor to set up the appropriate current level in the D/A converter. The D/A converter output current is then converted to a voltage output by an output buffer and a resistive network. The matching among the on-chip resistors preserves the gain accuracy between these conversions.

The D/A converter can be used in a multiplying mode by modulating the reference input within the specified $V_{REF\ IN}$ range.

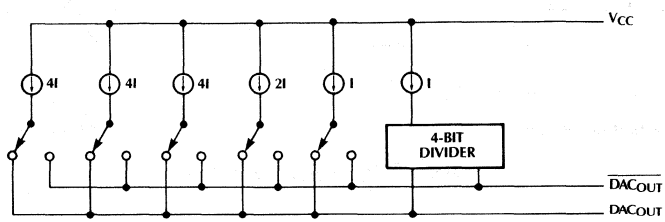


Figure 4. D/A Converter Implementation

1.2 SINGLE-SUPPLY vs. DUAL-SUPPLY OPERATION

ML2340 and ML2350 can be powered from a single supply ranging from 4.5V to 13.2V or dual supplies ranging from ±2.25V to ±6.6V.

The internal digital and analog circuitry is powered between V_{CC} and AGND. The range of DGND is AGND ≤ DGND ≤ V_{CC} – 4.5V with the logic thresholds set between .8V and 2.0V above DGND (standard TTL logic level). The range of V_{ZS} is AGND ≤ V_{ZS} ≤ (V_{CC} – 2.25V).

1.3 UNIPOLAR AND BIPOLAR OUTPUT VOLTAGE SWING

The ML2340 and ML2350 can operate in either unipolar and bipolar output voltage mode. Unipolar/bipolar mode selection is determined by comparing the zero scale voltage (V_{ZS}) of these devices to a precise internal reference that is referred to AGND. V_{ZS} is ideally the voltage that will be produced at the DAC voltage output when the digital input data is set to all "0's". Unipolar mode is selected when V_{ZS} is lower than 1.00 volt, and bipolar mode is selected when V_{ZS} is greater than 1.50 volts.

1.3.1 Unipolar Output Mode

In the unipolar mode, V_{OUT} swings above V_{ZS}. Ideally the 00000000 code results in an output voltage of V_{ZS}, and the 11111111 code results in an output voltage of V_{FS} × 255/256, where V_{FS} is the full-scale voltage determined by $V_{REF\ IN}$ and the gain setting.

1.3.2 Bipolar Output Mode

In the bipolar mode, V_{OUT} swings around V_{ZS}. The input data is in 2's complement binary format. Ideally, the 00000000 code results in an output voltage of V_{ZS}; the 10000000 code results in an output voltage of (V_{ZS} – V_{FS}); and the 01111111 results in an output voltage of (V_{ZS} + V_{FS} 127/128), where V_{FS} is the full scale output voltage determined by $V_{REF\ IN}$ and the gain setting.

1.4 OUTPUT BUFFER AND GAIN SETTING

The output buffer converts the D/A output current to a voltage output using a resistive network with proper gain setting determined by the GAIN 0 and GAIN 1 inputs. There are four possible gain settings for unipolar output voltage mode and bipolar output voltage mode as listed below:

Unipolar Output Voltage Mode

GAIN 1	GAIN 0	GAIN	Voltage Output Swing Relative to V_{ZS}
0	0	¼	$V_{REF\ IN}$ × ¼
0	1	½	$V_{REF\ IN}$ × ½
1	0	1	$V_{REF\ IN}$ × 1
1	1	2	$V_{REF\ IN}$ × 2

Bipolar Output Voltage Mode

GAIN 1	GAIN 0	GAIN	Voltage Output$_{P-P}$
0	0	¼	$\pm V_{REF\ IN} \times \frac{1}{8}$
0	1	½	$\pm V_{REF\ IN} \times \frac{1}{4}$
1	0	1	$\pm V_{REF\ IN} \times \frac{1}{2}$
1	1	2	$\pm V_{REF\ IN} \times 1$

The output buffer can source or sink as much as 10mA of current with an output voltage of at least 1V from either V_{CC} or AGND. As the output voltage approaches V_{CC} or AGND the current sourcing/sinking capability of the output buffer is reduced. The output buffer can still swing down to within 10mV of AGND and up to within 40mV of V_{CC} with a 100K load at V_{OUT} to AGND in the unipolar operation. In the bipolar operation, the output buffer swing is limited to about 100mV from either rails.

1.5 VOLTAGE REFERENCE

A bandgap voltage reference is incorporated on the ML2340 and ML2350. Two reference voltages can be produced by each device. An internal comparator monitors the power supply voltage to determine the selection of the reference voltage. A reference voltage of 2.25 volts on the ML2340 and 2.50 volts on the ML2350 is selected when the supply voltage is less than approximately 7.50 volts. Otherwise, a reference voltage of 4.50 volts and 5.00 volts is selected. To prevent the comparator from oscillating between the two selections, avoid operation with a power supply between 7.0 and 8.0 volts.

The bandgap reference is trimmed for zero Temperature Coefficient (TC) at 35°C to minimize output voltage drift over the specified operating temperature range.

The internal reference is buffered for use by the DAC and external circuits. The reference buffer will source more than 5mA of current and sink more than 1mA of current. With $V_{REF\ IN}$ connected to $V_{REF\ OUT}$, the following output voltage ranges of the DAC are obtained:

ML2340

Gain Setting	V_{REF} = 2.25V with $V_{CC} \leq$ 7.0V		V_{REF} = 4.5V with $V_{CC} \geq$ 8.0V	
	Unipolar	Bipolar	Unipolar	Bipolar
¼	0 to 0.562V	–0.281V to +0.281V	0 to 1.125V	–0.562V to +0.562V
½	0 to 1.125V	–0.562V to +0.562V	0 to 2.250V	–1.125V to +1.125V
1	0 to 2.250V	–1.125V to +1.125V	0 to 4.500V	–2.250V to +2.250V
2	0 to 4.500V	–2.250V to +2.250V	0 to 9.000V	–4.500V to +4.500V

ML2350

Gain Setting	V_{REF} = 2.50V with $V_{CC} \leq$ 7.0V		V_{REF} = 5.00V with $V_{CC} \geq$ 8.0V	
	Unipolar	Bipolar	Unipolar	Bipolar
¼	0 to 0.625V	–0.3125V to +0.3125V	0 to 1.25V	–0.625V to +0.625V
½	0 to 1.250V	–0.6250V to +0.6250V	0 to 2.50V	–1.250V to +1.250V
1	0 to 2.500V	–1.2500V to +1.2500V	0 to 5.00V	–2.500V to +2.500V
2	0 to 5.000V	–2.5000V to +2.5000V	0 to 10.00V	–5.000V to +5.000V

An external reference can alternatively be used on $V_{REF\ IN}$ to set the desired full scale voltage. The linearity of the D/A converter depends on the reference used, however. To insure integral linearity at an 8-bit level, a reference voltage of no less than 2V and no more than 7V (2.75V for operation with a low-voltage power supply) should be used.

1.6 DIGITAL INTERFACE

The digital interface of the ML2340 and ML2350 consist of a transfer input (XFER) and eight data inputs, DB0 through DB7. The digital interface operates in one of the two modes:

1.6.1 Single-Buffered Mode

Digital input data on DB0–DB7 is passed through an 8-bit transparent input latch on the rising edge of XFER. Because the outputs of the latch are connected directly to the inputs of the internal DAC, changes on the digital data while the XFER input is still active will cause an immediate change in the DAC output voltage. To hold the input data on the latch, the XFER input needs to be deactivated while the data is still stable.

1.6.2 Flow-Through Mode

In the flow-through mode, the input latch is bypassed. When XFER is set to logic "1", a change of data inputs, DB0–DB7, results in an immediate update of the output voltage.

1.7 POWER-ON-RESET

The ML2340 and ML2350 have an internal power-on-reset circuit to initialize the device when power is first applied to the device. The power-on-reset interval of typically 8μs begins when the supply voltage, V_{CC} reaches approximately 2.0V. During the power-on-reset interval, the transparent latch is reset to all "0's".

2.0 TYPICAL APPLICATIONS

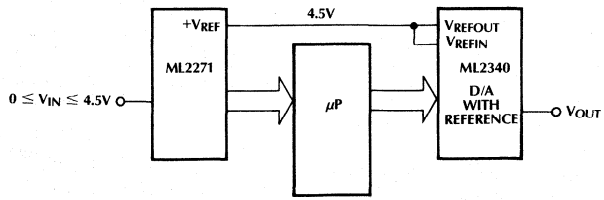


Figure 5. Using 4.50V Reference of D/A for Reference of A/D Using Single 5V V_{CC} ± 10%

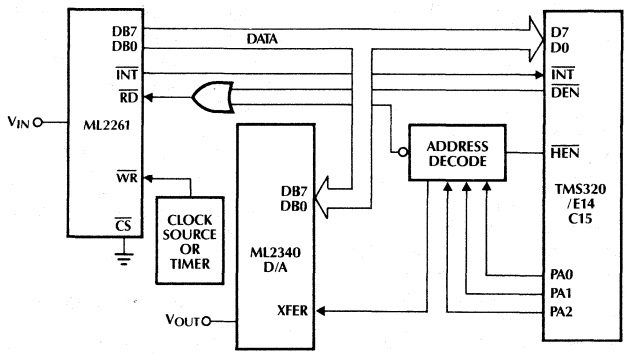


Figure 6. TMS320 Interface

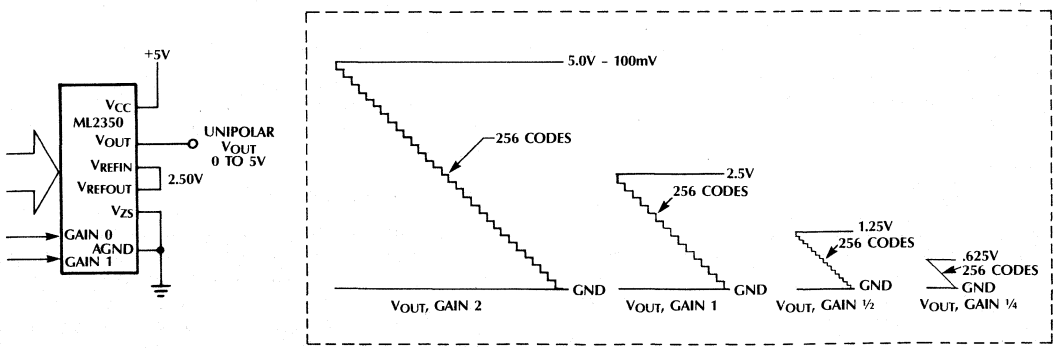


Figure 7. Single 5V Supply Unipolar V_{OUT}

2.0 TYPICAL APPLICATIONS (Continued)

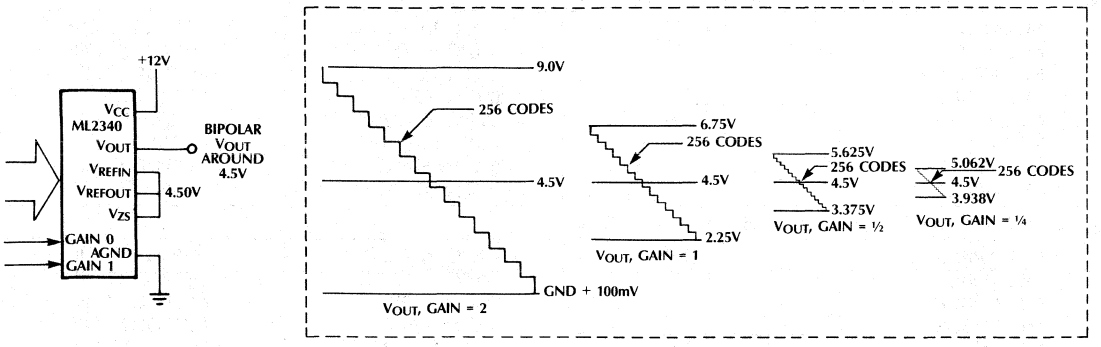


Figure 8. Single 12V Supply, Bipolar V_{OUT} with 11-Bits Resolution Around Zero

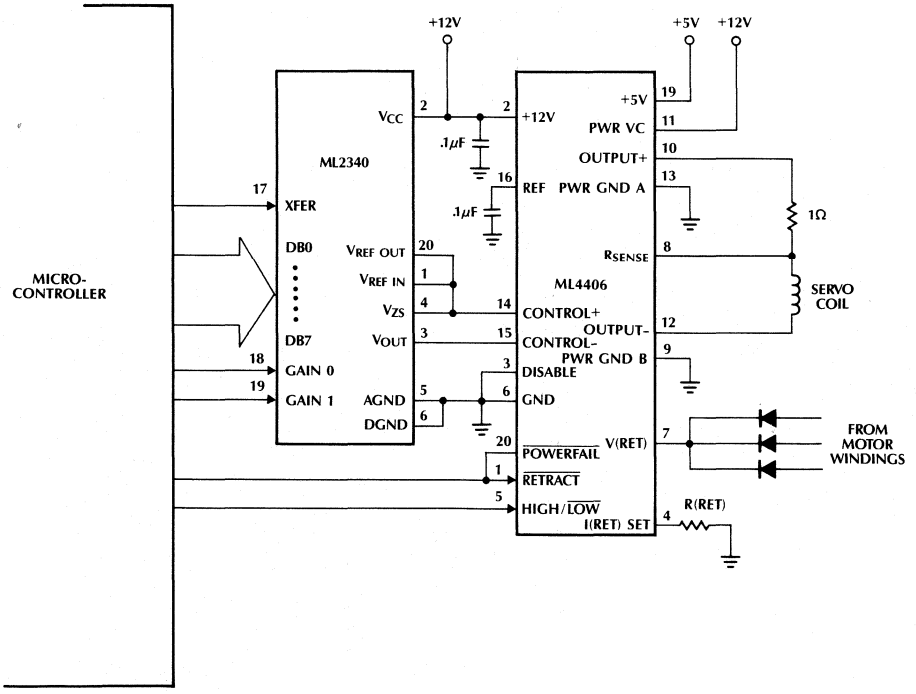


Figure 9. Hard Disc Drive Servo Coil Driver Providing 13-Bit Effective Resolution

ORDERING INFORMATION

PART NUMBER	INTEGRAL & DIFFERENTIAL NON-LINEARITY	TEMPERATURE RANGE	PACKAGE
$V_{REF\ OUT}$ = 4.50V with $V_{CC} \geq$ 8V and 2.25V with $V_{CC} \leq$ 7V			
ML2340BMJ	±¼ LSB	–55°C to +125°C	HERMETIC DIP
ML2340BIJ		–40°C to +85°C	HERMETIC DIP
ML2340BCP		0°C to +70°C	MOLDED DIP
ML2340BCS		0°C to +70°C	MOLDED SOIC
ML2340CMJ	±½ LSB	–55°C to +125°C	HERMETIC DIP
ML2340CIJ		–40°C to +85°C	HERMETIC DIP
ML2340CCP		0°C to +70°C	MOLDED DIP
ML2340CCS		0°C to +70°C	MOLDED SOIC
$V_{REF\ OUT}$ = 5.00V with $V_{CC} \geq$ 8V and 2.50V with $V_{CC} \leq$ 7V			
ML2350BMJ	±¼ LSB	–55°C to +125°C	HERMETIC DIP
ML2350BIJ		–40°C to +85°C	HERMETIC DIP
ML2350BCP		0°C to +70°C	MOLDED DIP
ML2350BCS		0°C to +70°C	MOLDED SOIC
ML2350CMJ	±½ LSB	–55°C to +125°C	HERMETIC DIP
ML2350CIJ		–40°C to +85°C	HERMETIC DIP
ML2350CCP		0°C to +70°C	MOLDED DIP
ML2350CCS		0°C to +70°C	MOLDED SOIC

Micro Linear

ML2341, ML2351

Single Supply, Programmable 8-Bit D/A Converters

GENERAL DESCRIPTION

The ML2341 and ML2351 are CMOS voltage output, 8-bit D/A converters with an internal voltage reference and a μP interface. These devices are designed to be powered by a single supply, although they can be powered from dual power supplies. The output voltage swings above zero scale (V_{ZS}) in the unipolar mode or around zero scale (V_{ZS}) in the bipolar mode, both with programmable gain. V_{ZS} can be set to any voltage from AGND to 2.25V below V_{CC}. The digital and analog grounds, DGND and AGND, are totally independent of each other. DGND can be set to any voltage from AGND to 4.5V below V_{CC} for easy interfacing to standard TTL and CMOS logic families.

The high level of integration and versatility of the ML2341 and ML2351 makes them ideal for a wide range of applications in hard disk drives, automotive, telecom, and a variety of general purpose industrial. One specific intended application is controlling a hard disk voice coil.

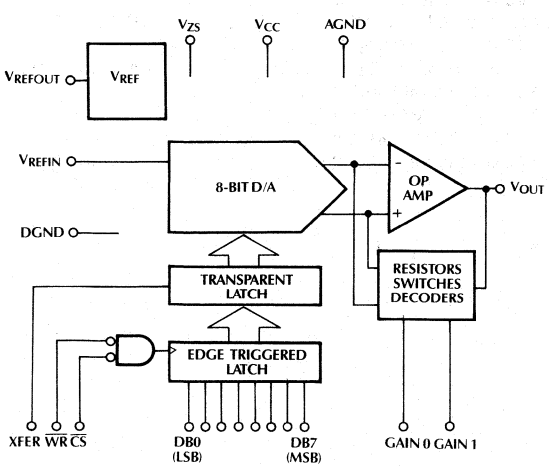
The ML2341 provides a 2.25V or 4.50V reference output for use with A/D converters that use a single 5V ± 10% power supply, while the ML2351 provides a 2.50V or 5.00V reference output.

FEATURES

- Programmable output voltage gain settings of 2, 1, ½, ¼ provide 8-, 9-, 10-, or 11-bit effective resolution around zero
- AGND to V_{CC} output voltage swing
- Bipolar or unipolar output voltage
- 4.5V to 13.2V single supply or ±2.25V to ±6.5V dual-supply operation
- Single- and double-buffered, edge-triggered interface with 30ns write time, 0ns hold time
- Voltage reference output
  - ML2341 ..... 2.25V or 4.50V
  - ML2351 ..... 2.50V or 5.00V
- Nonlinearity ..... ±¼ LSB or ±½ LSB
- Output voltage settling time over temperature and supply voltage tolerance
  - Within 1V of V_{CC} and AGND ..... 2.5μs max
  - Within 100mV of V_{CC} and AGND ..... 5μs max
- TTL and CMOS compatible digital inputs
- Low supply current ($V_{REF} \leq 2.5V$) ..... 5mA max
- 20-pin DIP or PCC
- Operating temperature range of 0°C to +70°C, –40°C to +85°C, and –55°C to +125°C

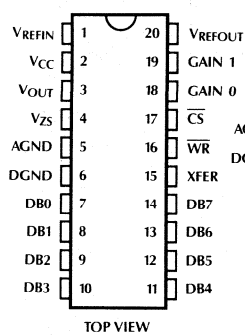
2

BLOCK DIAGRAM



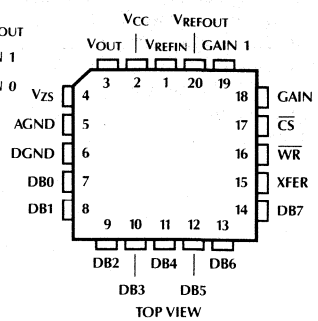
PIN CONNECTIONS

ML2341
ML2351
20-Pin DIP



TOP VIEW

ML2341
ML2351
20-Pin PCC



TOP VIEW

PIN DESCRIPTION

PIN #	NAME	FUNCTION
1	$V_{REF\ IN}$	Voltage reference input. $V_{REF\ IN}$ is referenced to AGND.
2	V_{CC}	Positive supply.
3	V_{OUT}	Voltage output of the D/A converter. V_{OUT} is referenced to V_{ZS}.
4	V_{ZS}	Zero Scale Voltage. V_{OUT} is referenced to V_{ZS}. V_{ZS} is normally tied to AGND in the unipolar mode or to mid-supply in the bipolar mode. When the device is operated from a single power supply, V_{ZS} has a maximum current requirement of –300μA in the bipolar mode.
5	AGND	Analog ground.
6	DGND	Digital ground. This is the ground reference level for all digital inputs. The range is AGND < (V_{CC} – 4.5V). DGND is normally tied to system ground.
7	DB0	Data input — Bit 0 (LSB).
8	DB1	Data input — Bit 1.
9	DB2	Data input — Bit 2.
10	DB3	Data input — Bit 3.
11	DB4	Data input — Bit 4.
12	DB5	Data input — Bit 5.
13	DB6	Data input — Bit 6.
14	DB7	Data input — Bit 7 (MSB).
15	XFER	Transfer enable input. In the double buffered mode of operation, the data in the input latch is transferred to the D/A converter at the high level of XFER.
16	$\overline{WR}$	Write enable input. While $\overline{CS}$ is low, data inputs are latched into the input latch on the rising edge of $\overline{WR}$.
17	$\overline{CS}$	Chip select input. Active low input which enables latching in the data on the rising edge of $\overline{WR}$.
18	GAIN 0	Digital gain setting input 0.
19	GAIN 1	Digital gain setting input 1.
20	$V_{REF\ OUT}$	Voltage reference output. $V_{REF\ OUT}$ is referenced to AGND. $V_{REF\ OUT}$ is set to 2.5V and 5.0V in a low-voltage and high-voltage operation, respectively for the ML2351; 2.25V and 4.5V for the ML2341.

ABSOLUTE MAXIMUM RATINGS
(Note 1)

Supply Voltage V_{CC} with Respect to AGND 14.2V
DGND ..... –0.3V to V_{CC} + 0.3V
V_{ZS}, $V_{REF\ IN}$ ..... –0.3V to V_{CC} + 0.3V
Logic Inputs ..... –0.3V to V_{CC} + 0.3V
Input Current per Pin (Note 2) ..... ±25mA
Storage Temperature ..... –65°C to +150°C
Package Dissipation at T_A = 25°C (Board Mount) 875mW
Lead Temperature (Soldering 10 sec.)
Dual-In-Line Package (Plastic) ..... 260°C
Dual-In-Line Package (Ceramic) ..... 300°C
Molded Chip Carrier Package
Vapor Phase (60 sec.) ..... 215°C
Infrared (15 sec.) ..... 220°C

OPERATING CONDITIONS
(Note 1)

Supply Voltage, V_{CC} ..... $4.5V_{DC}$ to $13.2V_{DC}$
Temperature Range (Note 3) ..... $T_{MIN} \leq T_A \leq T_{MAX}$
ML2341BMJ, ML2341CMJ
ML2351BMJ, ML2351CMJ ..... –55°C to +125°C
ML2341BIJ, ML2341CIJ
ML2351BIJ, ML2351CIJ ..... –40°C to +85°C
ML2341BCQ, ML2341CCQ
ML2351BCQ, ML2351CCQ
ML2341BCP, ML2341CCP
ML2351BCP, ML2351CCP ..... 0°C to +70°C

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, $T_A = T_{MIN}$ to T_{MAX}, V_{CC} – AGND = 5V ± 10% and 12V ± 10%, $V_{REF\ IN}$ for ML2341 = 2.25V and 4.50V, for ML2351 $V_{REF\ IN}$ = 2.50V and 5.00V, V_{OUT} load is R_L = 1k and C_L = 100pF, V_{REF} load is R_L = 1K and C_L = 100pF and input control signals with $t_R = t_F \leq 20$ns.

PARAMETER	NOTES	CONDITIONS	ML2341XCX, ML2351XCX MIN	ML2341XCX, ML2351XCX TYP (Note 4)	ML2341XCX, ML2351XCX MAX	ML2341XIX, ML2341XMX ML2351XIX, ML2351XMX MIN	ML2341XIX, ML2341XMX ML2351XIX, ML2351XMX TYP (Note 4)	ML2341XIX, ML2341XMX ML2351XIX, ML2351XMX MAX	UNITS
Converter and Programmable Gain Amplifier									
Converter Resolution	5		8			8			Bits
Integral Linearity Error ML2341BXX, ML2351BXX ML2341CXX, ML2351CXX	5	GAIN = 2, 1, ½, or ¼			 ±¼ ±½			 ±¼ ±½	 LSB LSB
Differential Linearity Error ML2341BXX, ML2351BXX ML2341CXX, ML2351CXX	5	GAIN = 2, 1, ½, or ¼			 ±¼ ±½			 ±¼ ±½	 LSB LSB
Mode Select Unipolar Output Bipolar Output	5	V_{ZS} with respect to AGND	 0 1.50		 1.0 V_{CC}–2.25	 0 1.50		 1.0 V_{CC}–2.25	 V V
Offset Error Unipolar Mode	5	Figure 1 GAIN = ¼, ½, 1 GAIN = 2			 ±10 ±20			 ±12 ±24	 mV mV
Bipolar Mode	5	Figure 1 GAIN = ¼, ½, 1, 2			±10 plus ±2½ LSB			±10 plus ±2½ LSB	mV
Gain Error Unipolar Mode Bipolar Mode	5	Figure 1 GAIN = ¼, ½, 1, 2 GAIN = ¼, ½, 1, 2		 ±.5 ±.5	 ±2 ±2		 ±.5 ±.5	 ±2.5 ±2.5	 %FS %FS
Reference									
$V_{REF\ OUT}$ Voltage ML2341BXX	5	$V_{CC} \leq 7.0V$ $T_A = 25°C$ T_{MIN} to T_{MAX}	2.23 2.22	2.25	2.27 2.28	2.23 2.18	2.25	2.27 2.32	V V
		$V_{CC} \geq 8.0V$ $T_A = 25°C$ T_{MIN} to T_{MAX}	4.48 4.46	4.50	4.52 4.54	4.48 4.43	4.50	4.52 4.57	V V
ML2341CXX		$V_{CC} \leq 7.0V$ $T_A = 25°C$ T_{MIN} to T_{MAX}	2.22 2.20	2.25	2.29 2.30	2.22 2.18	2.25	2.28 2.32	V V
		$V_{CC} \geq 8.0V$ $T_A = 25°C$ T_{MIN} to T_{MAX}	4.45 4.40	4.50	4.55 4.60	4.45 4.35	4.50	4.55 4.65	V V
ML2351BXX	5	$V_{CC} \leq 7.0V$ $T_A = 25°C$ T_{MIN} to T_{MAX}	2.48 2.47	2.50	2.52 2.53	2.48 2.43	2.50	2.52 2.57	V V
		$V_{CC} \geq 8.0V$ $T_A = 25°C$ T_{MIN} to T_{MAX}	4.98 4.96	5.00	5.02 5.04	4.98 4.90	5.00	5.02 5.10	V V
ML2351CXX		$V_{CC} \leq 7.0V$ $T_A = 25°C$ T_{MIN} to T_{MAX}	2.45 2.44	2.50	2.55 2.58	2.46 2.42	2.50	2.55 2.59	V V
		$V_{CC} \geq 8.0V$ $T_A = 25°C$ T_{MIN} to T_{MAX}	4.95 4.90	5.00	5.05 5.10	4.95 4.85	5.00	5.05 5.15	V V
Temperature Coefficient $V_{REF\ OUT}$				50			50		ppm/°C
V_{REF} Output Current	5		–1		5	–1		5	mA
$V_{REF\ OUT}$ Power Supply Rejection Ratio	5	100mV_{P-P}, 1kHz Sinewave on V_{CC}	–40	–60		–40	–60		dB

2

ELECTRICAL CHARACTERISTICS (Continued)

Unless otherwise specified, $T_A = T_{MIN}$ to T_{MAX}, V_{CC} – AGND = 5V ± 10% and 12V ± 10%. $V_{REF\ IN}$ for ML2341 = 2.25V and 4.50V; for ML2351 $V_{REF\ IN}$ = 2.50V and 5.00V, V_{OUT} load is R_L = 1k and C_L = 100pF, V_{REF} load is R_L = 1K and C_L = 100pF and input control signals with $t_R = t_F \leq 20$ns.

			ML2341XCX, ML2351XCX			ML2341XIX, ML2341XMX ML2351XIX, ML2351XMX			
PARAMETER	NOTES	CONDITIONS	MIN	TYP (Note 4)	MAX	MIN	TYP (Note 4)	MAX	UNITS
$V_{REF\ IN}$ and V_{ZS}									
$V_{REF\ IN}$ Input Range	5	$V_{CC} \leq 7.00V$	AGND+2		AGND+2.6	AGND+2		AGND+2.6	V
		$V_{CC} \geq 8.00V$	AGND+2		AGND+5.5	AGND+2		AGND+5.5	V
$V_{REF\ IN}$ DC Input Resistance	5		10			10			MΩ
V_{ZS} Voltage Range	5, 8		AGND		$V_{CC}/2 \times 1.1$	AGND		$V_{CC}/2 \times 1.1$	V
Analog Output									
V_{OUT} Output Swing Unipolar Mode	5, 8	R_L = 100K	AGND+0.01		V_{CC}–.04	AGND+0.01		V_{CC}–.04	V
		R_L = 1K	AGND+1.0		V_{CC}–1.0	AGND+1.0		V_{CC}–1.0	V
Bipolar Mode	5	R_L = 100K	AGND+0.1		V_{CC}–0.1	AGND+0.1		V_{CC}–0.1	V
		R_L = 1K	AGND+1.0		V_{CC}–1.0	AGND+1.0		V_{CC}–1.0	V
V_{OUT} Output Current	5	AGND+1V<V_{OUT}<V_{CC}–1V	–10		+10	–10		+10	mA
Power Supply Rejection Ratio		100mV_{P-P}, 1kHz sinewave on V_{CC}		–60			–60		dB
Digital and DC									
$V_{IN(0)}$ Logical "0" Input Voltage	5				0.8			0.8	V
$V_{IN(1)}$ Logical "1" Input Voltage	5		2.0			2.0			V
$I_{IN(0)}$ Logical "0" Input Current	5	V_{IN} = DGND	–1			–1			µA
$I_{IN(1)}$ Logical "1" Input Current	5	$V_{IN} = V_{CC}$			1			1	µA
Supply Current, Bipolar Mode									
I_{CC}, V_{CC} Current	5	V_{CC} = 5V ± 10%			5.3			5.3	mA
I_{AGND}, Analog Ground Current					–5.0			–5.0	mA
I_{VZS}, V_{ZS} Current				–90	–300		–90	–300	µA
I_{CC}, V_{CC} Current	5	V_{CC} = 12V ± 10%			9.3			9.3	mA
I_{AGND}, Analog Ground Current					–9.0			–9.0	mA
I_{VZS}, V_{ZS} Current				–90	–300		–90	–300	µA

ELECTRICAL CHARACTERISTICS (Continued)

Unless otherwise specified, $T_A = T_{MIN}$ to T_{MAX}, V_{CC} – AGND = 5V ± 10% and 12V ± 10%. $V_{REF\ IN}$ for ML2341 = 2.25V and 4.50V; for ML2351 $V_{REF\ IN}$ = 2.50V and 5.00V, V_{OUT} load is R_L = 1k and C_L = 100pF, V_{REF} load is R_L = 1K and C_L = 100pF and input control signals with $t_R = t_F \leq 20$ns.

PARAMETER	NOTES	CONDITIONS	ML2341XCX, ML2351XCX			ML2341XIX, ML2341XMX ML2351XIX, ML2351XMX			UNITS
			MIN	TYP (Note 4)	MAX	MIN	TYP (Note 4)	MAX	
Digital and DC (Continued)									
Supply Current, Unipolar Mode									
I_{CC}, V_{CC} Current	5	V_{CC} = 5V ± 10%			6.0			6.0	mA
I_{AGND}, Analog Ground Current					–4.3			–4.3	mA
I_{VZS}, V_{ZS} Current					–1.7			–1.7	mA
I_{CC}, V_{CC} Current	5	V_{CC} = 12V ± 10%			11.0			11.0	mA
I_{AGND}, Analog Ground Current					–7.3			–7.3	mA
I_{VZS}, V_{ZS} Current					–3.7			–3.7	mA
AC Performance									
Settling Time	5	Figure 2,							
t_{S1}		Output Step of AGND + 1V to V_{CC} – 1V, R_L = 1K		1.2	2.5		1.2	3.0	µs
t_{S2}		Output Step of AGND + 100mV to V_{CC}–100mV, R_L = 100K		2.5	5		2.5	6	µs
t_{S3}		Output Step of ±1LSB			1			1	µs
t_{S4}, Gain Change		Change of Any Gain Setting		1.1	2.5		1.1	3	µs
t_{WR}, $\overline{WR}$ Pulse Width	5	Figure 3	30			30			ns
t_{XFER}, XFER Pulse Width	5	Figure 3	60			60			ns
t_{XW}, $\overline{WR}$↑ to XFER↓	6	Figure 3	60			60			ns
t_{DBS}, DB0–DB7 Setup Time	5	Figure 3	40			45			ns
t_{DBH}, DB0–DB7 Hold Time	5	Figure 3	0			0			ns
t_{CSS}, $\overline{CS}$ Setup Time	5	Figure 3	50			50			ns
t_{CSH}, $\overline{CS}$ Hold Time	5	Figure 3	0			0			ns
t_{RESET}, Power-On Reset Time	6				16			16	µs

Note 1: Absolute maximum ratings are limits beyond which the life of the integrated circuit may be impaired. All voltages unless otherwise specified are measured with respect to analog ground.

Note 2: When the voltage at any pin exceeds the power supply rails (V_{IN} < AGND or V_{IN} > V_{CC}) the absolute value of current at that pin should be limited to 25mA or less.

Note 3: –55°C to +125°C operating temperature range devices are 100% tested at temperature extremes with worst-case test conditions. –40°C to +85°C operating temperature range devices are 100% tested with temperature limits guaranteed by 100% testing, sampling, or by correlation with worst-case test conditions.

Note 4: Typicals are parametric norm at 25°C.

Note 5: Parameter guaranteed and 100% production tested.

Note 6: Parameter guaranteed. Parameters not 100% tested are not in outgoing quality level calculation.

Note 7: Supply current and analog ground current are specified with the digital inputs stable and no load on V_{OUT}.

Note 8: In unipolar operation with V_{ZS} and AGND tied together, digital codes that represent an analog value of less than 100mV from AGND should be avoided.

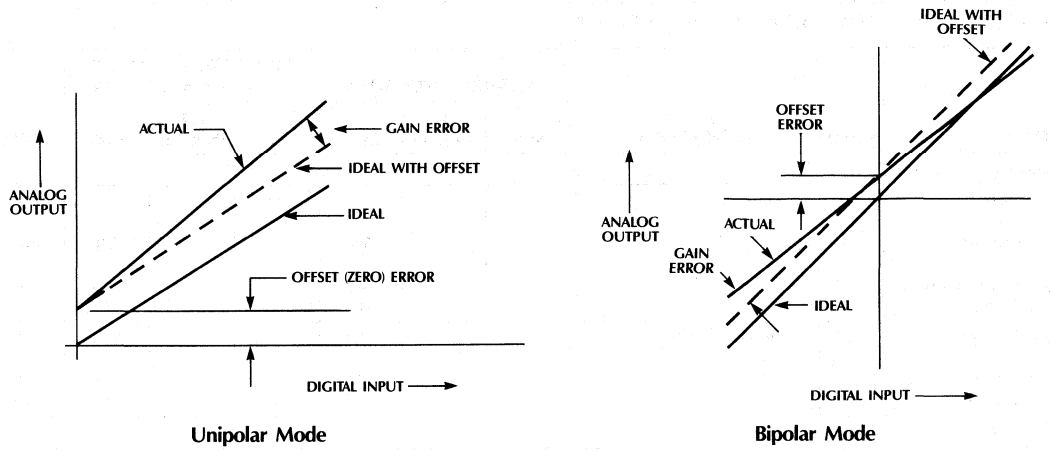


Figure 1. Gain and Offset Error

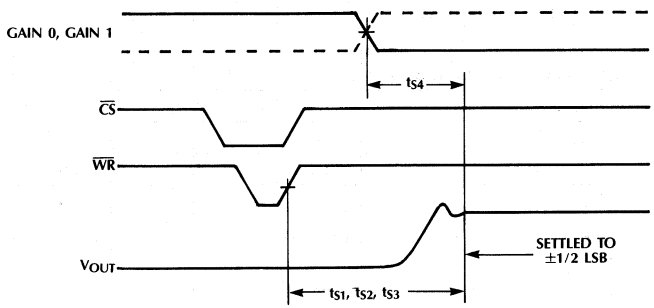


Figure 2. Settling Time

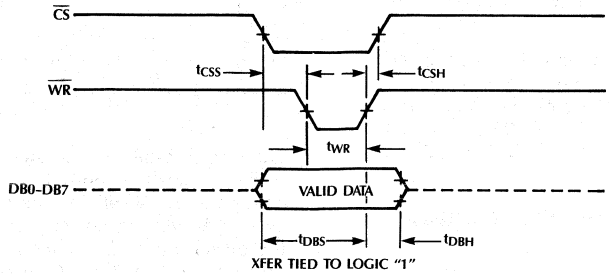


Figure 3a. Single Buffered Mode

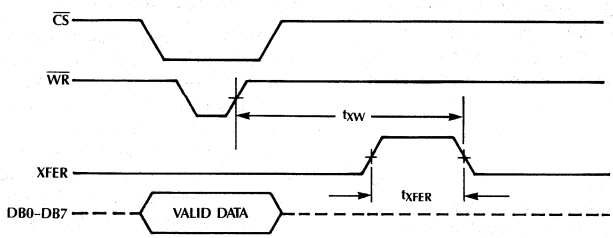


Figure 3b. Double Buffered Mode

1.0 FUNCTIONAL DESCRIPTION

1.1 D/A CONVERTER

The D/A converter is implemented using an array of equal current sources that are decoded semi linearly for the four most significant bits to improve differential linearity and to reduce output glitch around major carries. See Figure 4.

The input voltage reference of the D/A converter is the difference between $V_{REF\ IN}$ and AGND. This difference voltage is converted to a reference current using an internal resistor to set up the appropriate current level in the D/A converter. The D/A converter output current is then converted to a voltage output by an output buffer and a resistive network. The matching among the on-chip resistors preserves the gain accuracy between these conversions.

The D/A converter can be used in a multiplying mode by modulating the reference input within the specified $V_{REF\ IN}$ range.

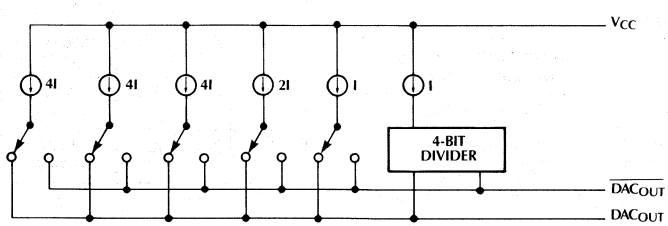


Figure 4. D/A Converter Implementation

1.2 SINGLE-SUPPLY vs. DUAL-SUPPLY OPERATION

ML2341 and ML2351 can be powered from a single supply ranging from 4.5V to 13.2V or dual supplies ranging from ±2.25V to ±6.6V.

The internal digital and analog circuitry is powered between V_{CC} and AGND. The range of DGND is AGND ≤ DGND ≤ V_{CC} – 4.5V with the logic thresholds set between .8V and 2.0V above DGND (standard TTL logic level). The range of V_{ZS} is AGND ≤ V_{ZS} ≤ (V_{CC} – 2.25V).

1.3 UNIPOLAR AND BIPOLAR OUTPUT VOLTAGE SWING

The ML2341 and ML2351 can operate in either unipolar and bipolar output voltage mode. Unipolar/bipolar mode selection is determined by comparing the zero scale voltage (V_{ZS}) of these devices to a precise internal reference that is referred to AGND. V_{ZS} is ideally the voltage that will be produced at the DAC voltage output when the digital input data is set to all "0's". Unipolar mode is selected when V_{ZS} is lower than 1.00 volt, and bipolar mode is selected when V_{ZS} is greater than 1.50 volts.

1.3.1 Unipolar Output Mode

In the unipolar mode, V_{OUT} swings above V_{ZS}. Ideally the 00000000 code results in an output voltage of V_{ZS}, and the 11111111 code results in an output voltage of V_{FS} × 255/256, where V_{FS} is the full-scale voltage determined by $V_{REF\ IN}$ and the gain setting.

1.3.2 Bipolar Output Mode

In the bipolar mode, V_{OUT} swings around V_{ZS}. The input data is in 2's complement binary format. Ideally, the 00000000 code results in an output voltage of V_{ZS}; the 10000000 code results in an output voltage of (V_{ZS} – V_{FS}); and the 01111111 results in an output voltage of (V_{ZS} + V_{FS} 127/128), where V_{FS} is the full scale output voltage determined by $V_{REF\ IN}$ and the gain setting.

1.4 OUTPUT BUFFER AND GAIN SETTING

The output buffer converts the D/A output current to a voltage output using a resistive network with proper gain setting determined by the GAIN 0 and GAIN 1 inputs. There are four possible gain settings for unipolar output voltage mode and bipolar output voltage mode as listed below:

Unipolar Output Voltage Mode

GAIN 1	GAIN 0	GAIN	Voltage Output Swing Relative to V_{ZS}
0	0	¼	$V_{REF\ IN}$ × ¼
0	1	½	$V_{REF\ IN}$ × ½
1	0	1	$V_{REF\ IN}$ × 1
1	1	2	$V_{REF\ IN}$ × 2

Bipolar Output Voltage Mode

GAIN 1	GAIN 0	GAIN	Voltage $Output_{P-P}$
0	0	¼	±$V_{REF\ IN}$ × ⅛
0	1	½	±$V_{REF\ IN}$ × ¼
1	0	1	±$V_{REF\ IN}$ × ½
1	1	2	±$V_{REF\ IN}$ × 1

The output buffer can source or sink as much as 10mA of current with an output voltage of at least 1V from either V_{CC} or AGND. As the output voltage approaches V_{CC} or AGND the current sourcing/sinking capability of the output buffer is reduced. The output buffer can still swing down to within 10mV of AGND and up to within 40mV of V_{CC} with a 100K load at V_{OUT} to AGND in the unipolar operation. In the bipolar operation, the output buffer swing is limited to about 100mV from either rails.

1.5 VOLTAGE REFERENCE

A bandgap voltage reference is incorporated on the ML2341 and ML2351. Two reference voltages can be produced by each device. An internal comparator monitors the power supply voltage to determine the selection of the reference voltage. A reference voltage of 2.25 volts on the ML2341 and 2.50 volts on the ML2351 is selected when the supply voltage is less than approximately 7.50 volts. Otherwise, a reference voltage of 4.50 volts and 5.00 volts is selected. To prevent the comparator from oscillating between the two selections, avoid operation with a power supply between 7.0 and 8.0 volts.

The bandgap reference is trimmed for zero Temperature Coefficient (TC) at 35°C to minimize output voltage drift over the specified operating temperature range.

The internal reference is buffered for use by the DAC and external circuits. The reference buffer will source more than 5mA of current and sink more than 1mA of current. With $V_{REF\ IN}$ connected to $V_{REF\ OUT}$, the following output voltage ranges of the DAC are obtained:

ML2341

Gain Setting	V_{REF} = 2.25V with V_{CC} ≤ 7.0V		V_{REF} = 4.5V with V_{CC} ≥ 8.0V	
	Unipolar	Bipolar	Unipolar	Bipolar
¼	0 to 0.562V	–0.281V to +0.281V	0 to 1.125V	–0.562V to +0.562V
½	0 to 1.125V	–0.562V to +0.562V	0 to 2.250V	–1.125V to +1.125V
1	0 to 2.250V	–1.125V to +1.125V	0 to 4.500V	–2.250V to +2.250V
2	0 to 4.500V	–2.250V to +2.250V	0 to 9.000V	–4.500V to +4.500V

ML2351

Gain Setting	V_{REF} = 2.50V with $V_{CC} \leq$ 7.0V		V_{REF} = 5.00V with $V_{CC} \geq$ 8.0V	
	Unipolar	Bipolar	Unipolar	Bipolar
¼	0 to 0.625V	–0.3125V to +0.3125V	0 to 1.25V	–0.625V to +0.625V
½	0 to 1.250V	–0.6250V to +0.6250V	0 to 2.50V	–1.250V to +1.250V
1	0 to 2.500V	–1.2500V to +1.2500V	0 to 5.00V	–2.500V to +2.500V
2	0 to 5.000V	–2.5000V to +2.5000V	0 to 10.00V	–5.000V to +5.000V

An external reference can alternatively be used on $V_{REF\ IN}$ to set the desired full scale voltage. The linearity of the D/A converter depends on the reference used, however. To insure integral linearity at an 8-bit level, a reference voltage of no less than 2V and no more than 7V (2.75V for operation with a low-voltage power supply) should be used.

1.6 DIGITAL INTERFACE

The digital interface of the device consists of a chip select input, $\overline{CS}$, a write input, $\overline{WR}$, a transfer input, XFER and eight data inputs, DB0 through DB7. The digital interface operates in one of the two modes:

1.6.1 Single-Buffered Mode

To use the ML2341 and ML2351 in the single-buffered mode, tie XFER to logic "1". This will put the D/A latch in the transparent mode and the rising edge of $\overline{WR}$ at low level of $\overline{CS}$ will latch the data on DB0–DB7 into the input latch as well as update the D/A output voltage.

1.6.2 Double-Buffered Mode

To use the devices in the double-buffered mode, timing information is applied to $\overline{WR}$ as well as XFER inputs. The rising edge of $\overline{WR}$ at low level of $\overline{CS}$ will latch the data on DB0–DB7 into the input latch. The D/A output voltage will not be updated, however, until XFER is brought to a high level, which transfers the data from input latch to D/A latch. Note that the D/A latch is a transparent latch controlled by the level, not edge, of the XFER input, any write operation to the input latch while XFER is still at a high level results in the immediate update of the D/A output voltage.

1.7 POWER-ON-RESET

The ML2341 and ML2351 have an internal power-on-reset circuit to initialize the device when power is first applied to the device. The power-on-reset interval of typically 8μs begins when the supply voltage, V_{CC} reaches approximately 2.0V. During the power-on-reset interval, both the input and data latch are reset to all "0's".

2.0 TYPICAL APPLICATIONS

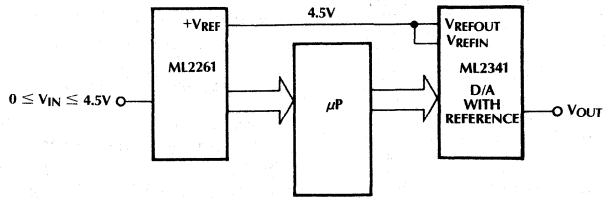


Figure 5. Using 4.50V Reference of D/A for Reference of A/D Using Single 5V V_{CC} ± 10%

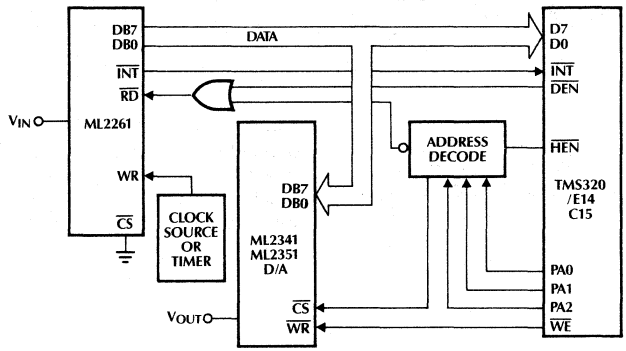


Figure 6. TMS320 Interface with D/A Output

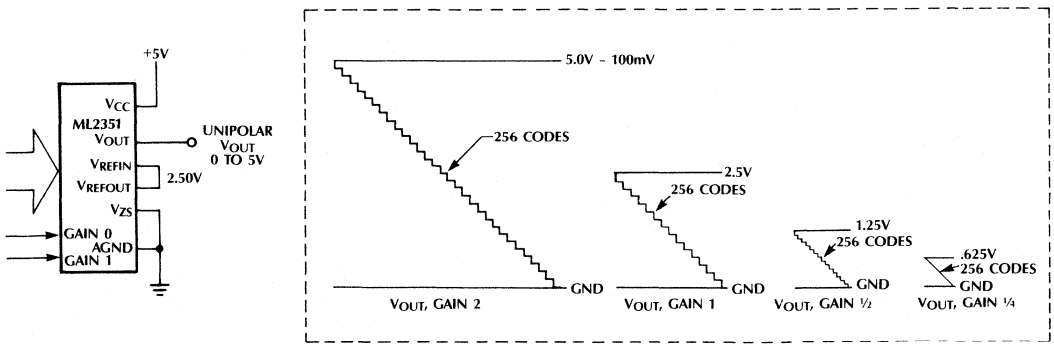


Figure 7. Single 5V Supply Unipolar V_{OUT}

2.0 TYPICAL APPLICATIONS (Continued)

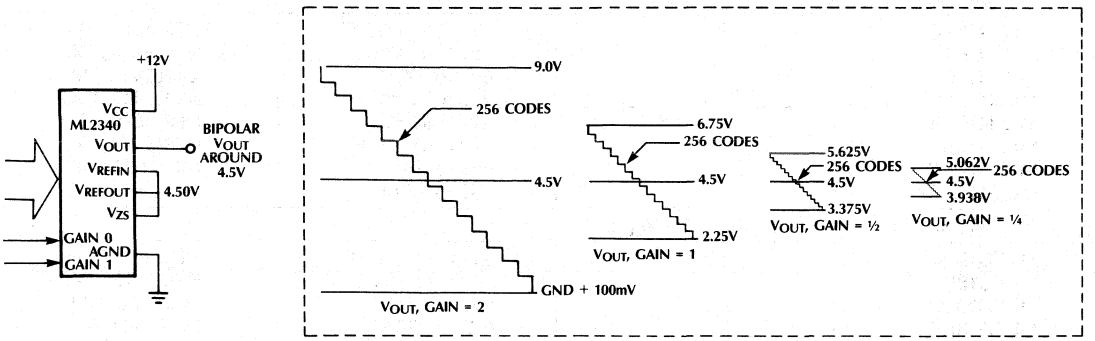


Figure 8. Single 12V Supply, Bipolar V_{OUT} with 11-Bits Resolution Around Zero

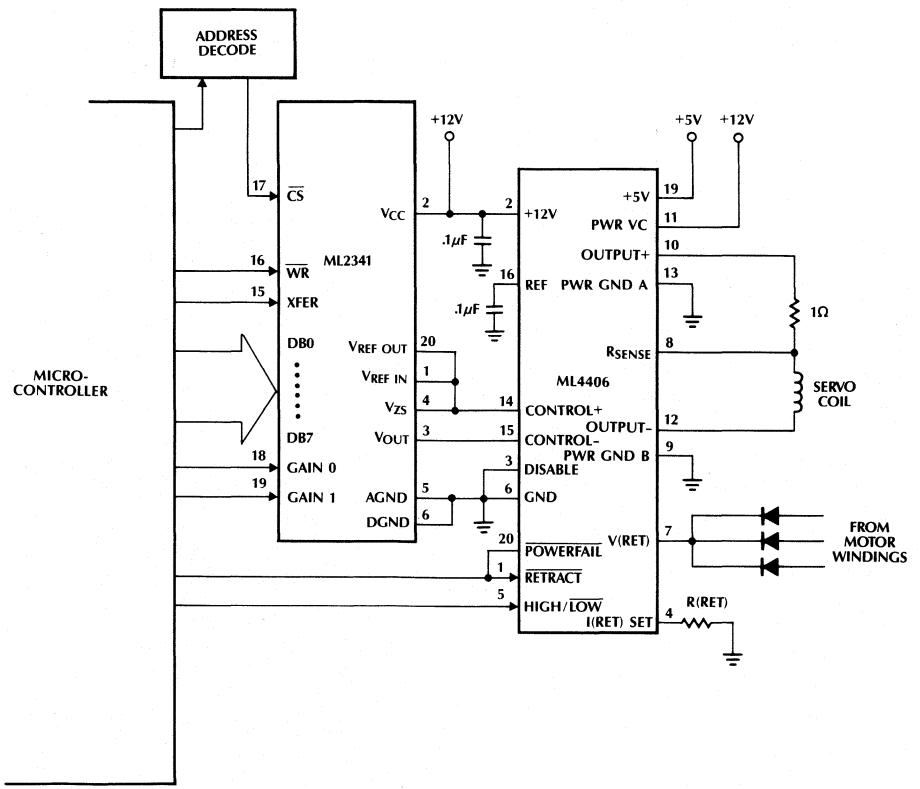


Figure 9. Hard Disc Drive Servo Coil Driver Providing 13-Bit Effective Resolution

ORDERING INFORMATION

PART NUMBER	INTEGRAL & DIFFERENTIAL NON-LINEARITY	TEMPERATURE RANGE	PACKAGE
$V_{REF\ OUT}$ = 4.50V with $V_{CC} \geq$ 8V and 2.25V with $V_{CC} \leq$ 7V			
ML2341BMJ	±¼ LSB	–55°C to +125°C	HERMETIC DIP
ML2341BIJ		–40°C to +85°C	HERMETIC DIP
ML2341BCP		0°C to +70°C	MOLDED DIP
ML2341BCQ		0°C to +70°C	MOLDED PCC
ML2341CMJ	±½ LSB	–55°C to +125°C	HERMETIC DIP
ML2341CIJ		–40°C to +85°C	HERMETIC DIP
ML2341CCP		0°C to +70°C	MOLDED DIP
ML2341CCQ		0°C to +70°C	MOLDED PCC
$V_{REF\ OUT}$ = 5.00V with $V_{CC} \geq$ 8V and 2.50V with $V_{CC} \leq$ 7V			
ML2351BMJ	±¼ LSB	–55°C to +125°C	HERMETIC DIP
ML2351BIJ		–40°C to +85°C	HERMETIC DIP
ML2351BCP		0°C to +70°C	MOLDED DIP
ML2351BCQ		0°C to +70°C	MOLDED PCC
ML2351CMJ	±½ LSB	–55°C to +125°C	HERMETIC DIP
ML2351CIJ		–40°C to +85°C	HERMETIC DIP
ML2351CCP		0°C to +70°C	MOLDED DIP
ML2351CCQ		0°C to +70°C	MOLDED PCC

Telecom Communications

Section 3

Selection Guide

Gain/Attenuators

Part Number	Gain Range (dB)	Resolution (dB Steps)	Noise (dBrnc @ Max Gain)	Harmonic Distortion (dB)	Digital Interface	Power Supplies (V)	Temperature Range C	Temperature Range I	Package
ML2003	-24 to +24	0.1	0	-60	Serial, Hard Wire	±5	X	X	18-pin DIP 20-pin PCC
ML2004	-24 to +24	0.1	0	-60	Serial	±5	X	X	14-pin DIP
ML2008	-24 to +24	0.1	0	-60	8-Bit µP	±5	X	X	18-pin DIP 20-pin PCC
ML2009	-24 to +24	0.1	0	-60	16-Bit µP	±5	X	X	18-pin DIP 20-pin PCC

Equalizers

Part Number	Frequency Response Adjustable	Idle Channel Noise (dBrnc)	Harmonic Distortion (dB)	Comment	Interface Interface	Power Supplies (V)	Temperature Range C	Temperature Range I	Package
ML2020	Slope, Height Bandwidth	8	-48	60 Hz Rejection	Serial	±5	X	X	16-pin DIP 18-pin SOIC
ML2021	Slope Height Bandwidth	8	-48	Group Delay Optimized	Serial	±5	X	X	16-pin DIP 18-pin SOIC

Tone Detectors

Part Number	Detect Frequency (Hz)	Dynamic Range Detect (dBm)	Frequency Template (Hz)	Comment	Power Supplies (V)	Temperature Range C	Temperature Range I	Package
ML2031	1K to 4K	-34 to +6	Detect ±10 No Detect ±36	Exceed Bell Pub 43004, Clock Outputs of CLK_{IN} ÷2, ÷8	±5	X	X	8-pin DIP
ML2032	1K to 4K	-34 to +6	Detect ±10 No Detect ±36	Exceed Bell Pub 43004, Uncommitted Op Amp	±5	X	X	8-pin DIP

Programmable Sinewave Generators

Part Number	Frequency Range (Hz)	Min Resolution (Hz)	Gain Error (dB)	Harmonic Distortion (dB)	Comment	Digital Interface	Power Supplies (V)	Temperature Range C	Temperature Range I	Package
ML2035	DC to 25K	±.75	±.1	-45	Voltage Amplitude $V_{CC}/2$	Serial	±5	X	X	8-pin DIP
ML2036	DC to 50K	±.75	±.1	-45	Adj. Voltage Amplitude, Clock Outputs of CLK_{IN} ÷2, ÷8	Serial	±5	X	X	14-pin DIP 16-pin SOIC

ML2003, ML2004

Logarithmic Gain/Attenuator

GENERAL DESCRIPTION

The ML2003 and ML2004 are digitally controlled logarithmic gain/attenuators with a range of -24 to +24dB in 0.1dB steps.

The gain settings are selected by a 9-bit digital word. The ML2003 digital interface is either parallel or serial. The ML2004 is packaged in a 14-pin DIP with a serial interface only.

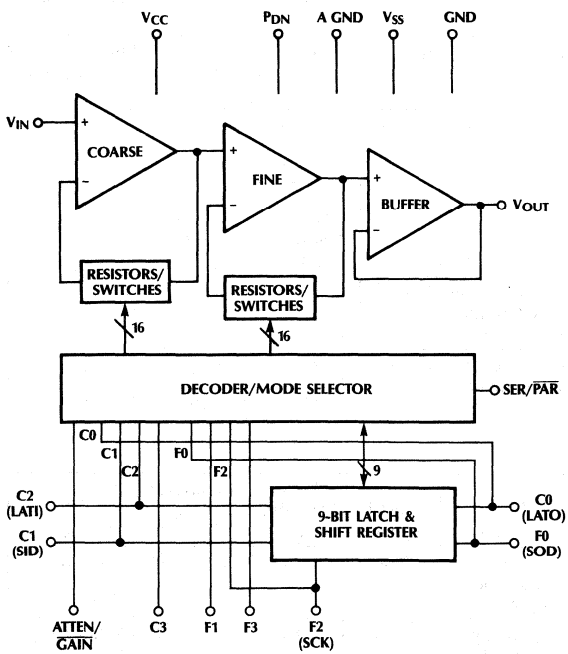
Absolute gain accuracy is 0.05dB max over supply tolerance of ±10% and temperature range.

These CMOS logarithmic gain/attenuators are designed for a wide variety of applications in telecom, audio, sonar, or general purpose function generation. One specific intended application is analog telephone lines.

FEATURES

- Low noise 0 dBrnc max with +24dB gain
- Low harmonic distortion -60dB max
- Gain range -24 to +24dB
- Resolution 0.1dB steps
- Flat frequency response ±.05dB from .3-4kHz
  ±.10dB from .1-20kHz
- Low supply current 4mA max from ±5V supplies
- TTL/CMOS compatible digital interface
- ML2003 has pin selectable serial or parallel interface; ML2004 serial interface only
- Standard 14-pin or 18-pin 0.3" center DIP or 20-pin molded chip carrier package

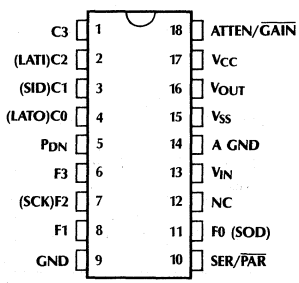
BLOCK DIAGRAM



NOTE: SERIAL MODE FUNCTIONS INDICATED BY PARENTHESES.

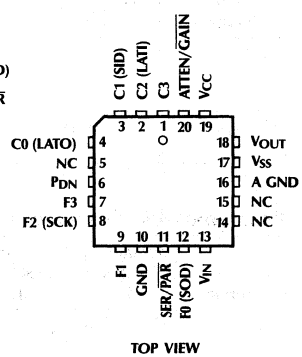
PIN CONNECTIONS

ML2003
18-PIN DIP



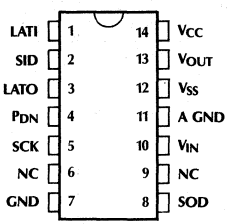
TOP VIEW

ML2003
20-PIN PCC



TOP VIEW

ML2004
14-PIN DIP



TOP VIEW

PIN DESCRIPTION

NAME	FUNCTION
C3	In serial mode, pin is unused. In parallel mode, coarse gain select bit. Pin has internal pulldown resistor to GND.
(LATI) C2	In serial mode, input latch clock which loads the data from the shift register into the latch. In parallel mode, coarse gain select bit. Pin has internal pulldown resistor to GND.
(SID) C1	In serial mode, serial data input that contains serial 9 bit data word which controls the gain setting. In parallel mode, coarse gain select bit. Pin has internal pulldown resistor to GND.
(LATO) C0	In serial mode, output latch clock which loads the 9 bit data word back into the shift register from the latch. In parallel mode, coarse gain select bit. Pin has internal pulldown resistor to GND.
P_{DN}	Powerdown input. When P_{DN} = 1, device is in powerdown mode. When P_{DN} = 0, device is in normal operation. Pin has internal pulldown resistor to GND.
F3	In serial mode, pin is unused. In parallel mode, fine gain select bit. Pin has internal pulldown resistor to GND.
(SCK) F2	In serial mode, shift register clock which shifts the serial data on SID into the shift register on rising edges and out on SOD on falling edges. In parallel mode, fine gain select bit. Pin has internal pulldown resistor to GND.
F1	In serial mode, pin is unused. In parallel mode, fine gain select bit. Pin has internal pulldown resistor to GND.
GND	Digital ground. 0 volts. All digital inputs and output are referenced to this ground.
SER/$\overline{PAR}$	Serial or parallel select input. When SER/$\overline{PAR}$ = 1, device is in serial mode. When SER/$\overline{PAR}$ = 0, device is in parallel mode. Pin has internal pullup resistor to V_{CC}.
(SOD) F0	In serial mode, serial output data which is the output of the shift register. In parallel mode, fine gain select bit. Pin has internal pulldown resistor to GND.
V_{IN}	Analog input.
AGND	Analog ground. 0 volts. Analog input and output are referenced to this ground.
V_{SS}	Negative supply. -5 volts ±10%.
V_{OUT}	Analog output.
V_{CC}	Positive supply. +5 volts ±10%.
ATTEN/$\overline{GAIN}$	In serial mode, pin is unused. In parallel mode, attenuation/gain select bit. Pin has internal pulldown resistor to GND.

ABSOLUTE MAXIMUM RATINGS
(Note 1)

Supply Voltage
- V_{CC} ..... +6.5V
- V_{SS} ..... -6.5V

AGND with respect to GND ..... ±.5V
Analog Input and Output ..... V_{SS} - 0.3V to V_{CC} + 0.3V
Digital Inputs and Outputs ..... GND - 0.3V to V_{CC} + 0.3V
Input Current Per Pin ..... ±25mA
Power Dissipation 750mW
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10 sec) ..... 300°C

OPERATING CONDITIONS

Temperature Range (Note 2)
- ML2003CP, ML2004CP, ML2004CQ ..... 0°C to +70°C
- ML2003IJ, ML2004IJ ..... -40°C to +85°C

Supply Voltage
- V_{CC} ..... 4V to 6V
- V_{SS} ..... -4V to -6V

ELECTRICAL CHARACTERISTICS

Unless otherwise specified $T_A = T_{MIN}$ to T_{MAX}, V_{CC} = 5V ±10%, V_{SS} = -5V ±10%, Data Word: ATTEN/$\overline{GAIN}$ = 1, Other Bits = 0 (0dB Ideal Gain), C_L = 100pF, R_L = 600Ω, SCK = LATI = LATO = 0, dBm measurements use 600Ω as reference load, digital timing measured at 1.4V.

SYMBOL	PARAMETER	NOTES	CONDITIONS	MIN	TYP NOTE 3	MAX	UNITS
Analog							
AG	Absolute gain accuracy	4	V_{IN} = 8dBm, 1kHz	-0.05		+0.05	dB
RG	Relative gain accuracy	4	100000001 000000000 000000001 All other gain settings All values referenced to 100000000 gain when ATTEN/$\overline{GAIN}$ = 1, V_{IN} = 8dBm when ATTEN/GAIN = 0, V_{IN} = (8dBm - Ideal Gain) in dB	-.05 -.05 -.05 -0.1		+.05 +.05 +.05 +0.1	dB dB dB dB
FR	Frequency response	4	300–4000Hz 100–20,000 Hz Relative to 1kHz	-0.05 -0.1		+0.05 +0.1	dB dB
VOS	Output Offset Voltage	4	V_{IN} = 0, +24dB gain			±100	mV
ICN	Idle Channel Noise	4 5	V_{IN} = 0, +24dB gain, C msg. Weighted V_{IN} = 0, +24dB gain, 1kHz		-6 450	0 900	dBrnc nv/√Hz
HD	Harmonic Distortion	4	V_{IN} = 8dBm, 1kHz Measure 2nd, 3rd harmonic relative to fundamental			-60	dB
SD	Signal to Distortion	4	V_{IN} = 8dBm, 1kHz. C msg. weighted	+60			dB
PSRR	Power Supply Rejection	4	200mV_{p-p}, 1kHz sine, V_{IN} = 0 on V_{CC} on V_{SS}		 -60 -60	 -40 -40	 dB dB
Z_{IN}	Input Impedance, V_{IN}	4		1			Meg
V_{INR}	Input Voltage Range	4		±3.0			V
V_{OSW}	Output Voltage Swing	4		±3.0			V
Digital and DC							
V_{IL}	Digital Input Low Voltage	4				.8	V
V_{IH}	Digital Input High Voltage	4		2.0			V
V_{OL}	Digital Output Low Voltage	4	I_{OL} = 2mA			.4	V
V_{OH}	Digital Output High Voltage	4	I_{OH} = -1mA	4.0			V
I_{NS}	Input Current, SER/$\overline{PAR}$	4	V_{IH} = GND	-5		-100	µA
I_{ND}	Input Current, All Digital Inputs Except SER/PAR	4	V_{IH} = V_{CC}	5		100	µA
I_{CC}	V_{CC} Supply Current	4	No output load, V_{IL} = GND, V_{IH} = V_{CC}, V_{IN} = 0			4	mA
I_{SS}	V_{SS} Supply Current	4	No output load, V_{IL} = GND, V_{IH} = V_{CC}, V_{IN} = 0			-4	mA
I_{CCP}	V_{CC} Supply Current, Powerdown Mode	4	No output load, V_{IL} = GND, V_{IH} = V_{CC}			.5	mA
I_{SSP}	V_{SS} Supply Current Powerdown Mode	4	No output load, V_{IL} = GND, V_{IH} = V_{CC}			-.1	mA

ELECTRICAL CHARACTERISTICS (Continued)

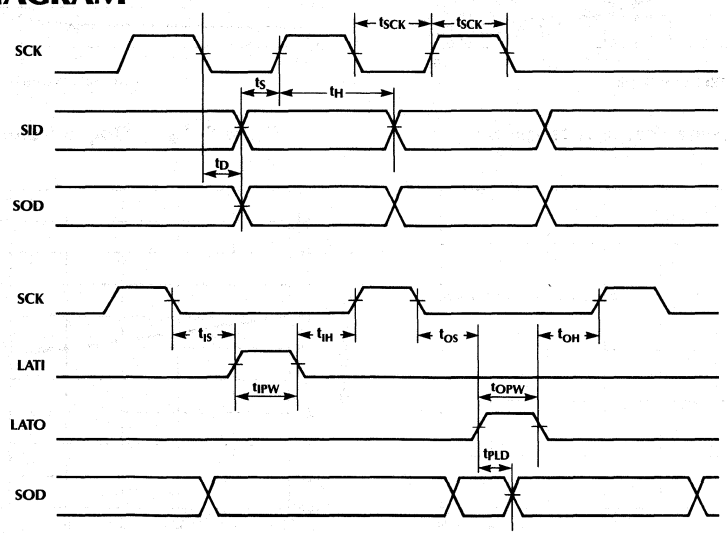
Unless otherwise specified $T_A = T_{MIN}$ to T_{MAX}, V_{CC} = 5V ±10%, V_{SS} = -5V ±10%, Data Word: ATTEN/$\overline{GAIN}$ = 1, Other Bits = 0 (0dB Ideal Gain), C_L = 100pF, R_L = 600Ω, SCK = LATI = LATO = 0, dBm measurements use 600Ω as reference load, digital timing measured at 1.4V. C_L = 100pF or SOD.

SYMBOL	PARAMETER	NOTES	CONDITIONS	MIN	TYP NOTE 3	MAX	UNITS
AC Characteristics							
t_{SET}	V_{OUT} Settling Time	4	V_{IN} = 0.185V. Change gain from -24 to +24dB. Measure from LATI rising edge to when V_{OUT} settles to within 0.05dB of final value.			20	µs
t_{STEP}	V_{OUT} Step Response	4	Gain = +24dB. V_{IN} = -0.185V to +0.185V step. Measured when V_{OUT} settles to within 0.05dB of final value.			20	µs
t_{SCK}	SCK On/Off Period	4		250			ns
t_S	SID Data Setup Time	4		50			ns
t_H	SID Data Hold Time	4		50			ns
t_D	SOD Data Delay	4		0		125	ns
t_{IPW}	LATI Pulse Width	4		50			ns
t_{OPW}	LATO Pulse Width	4		50			ns
t_{IS}, t_{OS}	LATI, LATO Setup Time	4		50			ns
t_{IH}, t_{OH}	LATI, LATO Hold Time	5		50			ns
t_{PLD}	SOD Parallel Load Delay	4		0		125	ns

Note 1: Absolute maximum ratings are limits beyond which the life of the integrated circuit may be impaired. All voltages unless otherwise specified are measured with respect to ground.
Note 2: 0°C to 70°C and -40°C to +85°C operating temperature range devices are 100% tested with temperature limits guaranteed by 100% testing, sampling, or by correlation with worst-case test conditions.
Note 3: Typicals are parametric norm at 25°C.
Note 4: Parameter guaranteed and 100% production tested.
Note 5: Parameter guaranteed. parameters not 100% tested are not in outgoing quality level calculation.

3

TIMING DIAGRAM



TIMING PARAMETERS ARE REFERENCED TO THE 1.4 VOLT MIDPOINT.

Figure 1. Serial Mode Timing Diagram

TYPICAL PERFORMANCE CURVES

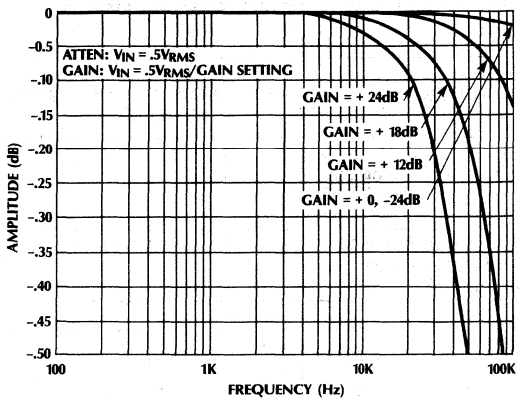


Figure 2. Amplitude vs Frequency (V_{IN}/V_{OUT} = .5V_{RMS})

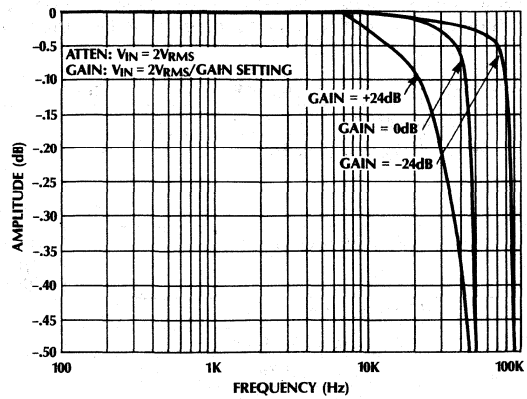


Figure 3. Amplitude vs Frequency (V_{IN}/V_{OUT} = 2V_{RMS})

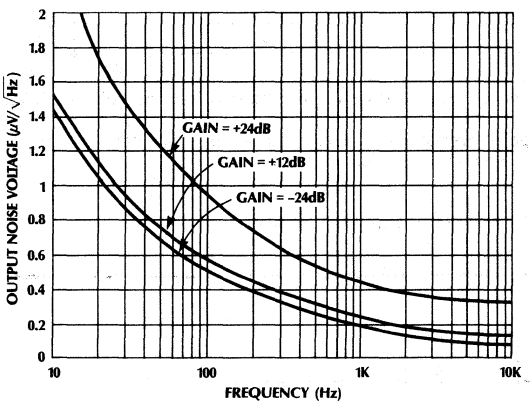


Figure 4. Output Noise Voltage vs Frequency

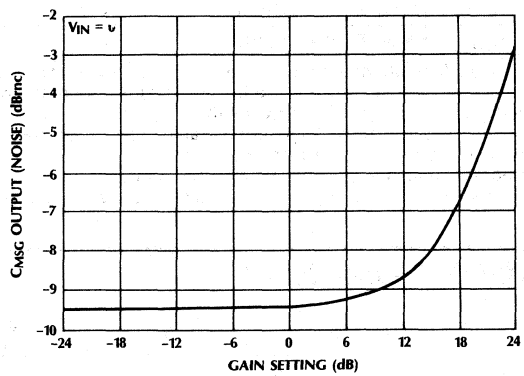


Figure 5. C_{MSG} Output Noise vs Gain Setting

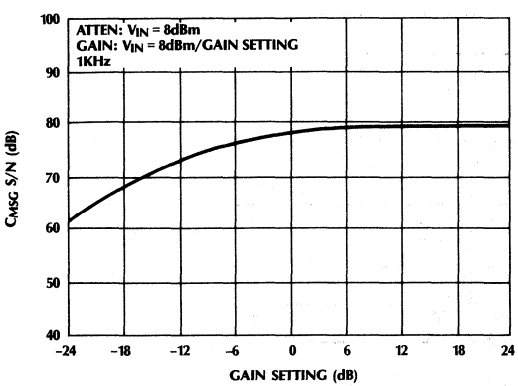


Figure 6. C_{MSG} S/N vs Gain Setting

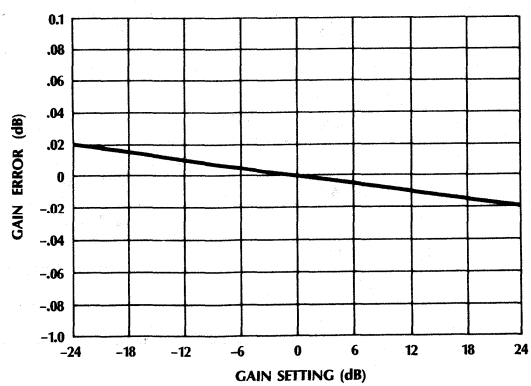


Figure 7. Gain Error vs Gain Setting

TYPICAL PERFORMANCE CURVES (Continued)

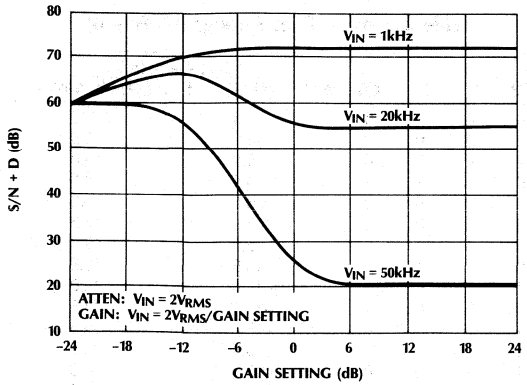


Figure 8. S/N + D vs Gain Setting (V_{IN}/V_{OUT} = $2V_{RMS}$)

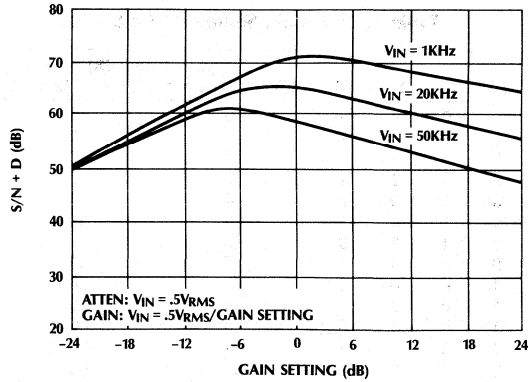


Figure 9. S/N + D vs Gain Setting (V_{IN}/V_{OUT} = $.5V_{RMS}$)

1.0 FUNCTIONAL DESCRIPTION

The ML2003 consists of a coarse gain stage, a fine gain stage, an output buffer, and a serial/parallel digital interface.

1.1 Gain Stages

The analog input, V_{IN}, goes directly into the op amp input in the coarse gain stage. The coarse gain stage has a gain range of 0 to 22.5dB in 1.5dB steps.

The fine gain stage is cascaded onto the coarse section. The fine gain stage has a gain range of 0 to 1.5dB in 0.1dB steps.

In addition, both sections can be programmed for either gain or attenuation, thus doubling the effective gain range.

The logarithmic steps in each gain stage are generated by placing the input signal across a resistor string of 16 series resistors. Analog switches allow the voltage to be tapped from the resistor string at 16 points. The resistors are sized such that each output voltage is at the proper logarithmic ratio relative to the input signal at the top of the string. Attenuation is implemented by using the resistor string as a simple voltage divider, and gain is implemented by using the resistor string as a feedback resistor around an internal op amp.

1.2 Gain Settings

Since the coarse and fine gain stages are cascaded, their gains can be summed logarithmically. Thus, any gain from -24dB to +24dB in 0.1dB steps can be obtained by combining the coarse and fine gain settings to yield the desired gain setting. The relationship between the digital select bits and the corresponding analog gain values is shown in Tables 1 and 2. Note that C3–C0 selects the coarse gain, F3–F0 selects the fine gain, and ATTEN/GAIN selects either attenuation or gain.

1.3 Output Buffer

The final analog stage is the output buffer. This amplifier has internal gain of 1 and is designed to drive 600 ohms and 100pF loads. Thus, it is suitable for driving a telephone hybrid circuit directly without any external amplifier.

1.4 Power Supplies

The digital section is powered between V_{CC} and GND, or 5 volts. The analog section is powered between V_{CC} and V_{SS} and uses AGND as the reference point, or ±5 volts.

GND and AGND are totally isolated inside the device to minimize coupling from the digital section into the analog section. However, AGND and GND should be tied together physically near the device and ideally close to the common power supply ground connection.

Typically, the power supply rejection of V_{CC} and V_{SS} to the analog output is greater than -60dB at 1kHz. If decoupling of the power supplies is still necessary in a system, V_{CC} and V_{SS} should be decoupled with respect to AGND.

3

FUNCTIONAL DESCRIPTION (Continued)

Table 1. Fine Gain Settings (C3–C0 = 0)

F3	F2	F1	F0	Ideal Gain (dB) ATTEN/GAIN = 1	Ideal Gain (dB) ATTEN/GAIN = 0
0	0	0	0	.0	.0
0	0	0	1	–.1	.1
0	0	1	0	–.2	.2
0	0	1	1	–.3	.3
0	1	0	0	–.4	.4
0	1	0	1	–.5	.5
0	1	1	0	–.6	.6
0	1	1	1	–.7	.7
1	0	0	0	–.8	.8
1	0	0	1	–.9	.9
1	0	1	0	–1.0	1.0
1	0	1	1	–1.1	1.1
1	1	0	0	–1.2	1.2
1	1	0	1	–1.3	1.3
1	1	1	0	–1.4	1.4
1	1	1	1	–1.5	1.5

Table 2. Coarse Gain Settings (F3–F0 = 0)

C3	C2	C1	C0	Ideal Gain (dB) ATTEN/GAIN = 1	Ideal Gain (dB) ATTEN/GAIN = 0
0	0	0	0	.0	.0
0	0	0	1	–1.5	1.5
0	0	1	0	–3.0	3.0
0	0	1	1	–4.5	4.5
0	1	0	0	–6.0	6.0
0	1	0	1	–7.5	7.5
0	1	1	0	–9.0	9.0
0	1	1	1	–10.5	10.5
1	0	0	0	–12.0	12.0
1	0	0	1	–13.5	13.5
1	0	1	0	–15.0	15.0
1	0	1	1	–16.5	16.5
1	1	0	0	–18.0	18.0
1	1	0	1	–19.5	19.5
1	1	1	0	–21.0	21.0
1	1	1	1	–22.5	22.5

1.5 Powerdown Mode

A powerdown mode can be selected with pin P_{DN}. When P_{DN} = 1, the device is powered down. In this state, the power consumption is reduced by removing power from the analog section and forcing the analog output, V_{OUT}, to a high impedance state. While the device is in powerdown mode, the digital section is still functional and the current data word remains stored in the latch when in serial mode. When P_{DN} = 0, the device is in normal operation.

1.6 Digital Section

The ML2003 can be operated with a serial or parallel interface. The SER/PAR pin selects the desired interface. When SER/PAR = 1, the serial mode is selected. When SER/PAR = 0, the parallel mode is selected. The ML2004 digital interface is serial only.

1.6.1 Serial Mode

Serial mode is selected by setting SER/$\overline{\text{PAR}}$ pin high. The serial interface allows the gain settings to be set from a serial data word.

The timing for the serial mode is shown in Figure 10. The serial input data, SID, is loaded into a shift register on rising edges of the shift clock, SCK. The data can be parallel loaded into a latch when the input latch signal, LATI, is high. The LATI pulse must occur when SCK is low. In this way, a new data word can be loaded into the shift register without disturbing the existing data word in the latch.

The parallel outputs of the latch control the attenuation/gain setting. The order of the data word bits in the latch is shown in Figure 11. Note that bit 0 is the first bit of the data word clocked into the shift register. Tables 1 and 2 describe how the data word programs the gain.

The device also has the capability to read out the data word stored in the latch. This can be done by parallel loading the data from the latch back into the shift register when the latch signal, LATO, is high. The LATO pulse must occur when SCK is low. Then, the data word can be shifted out of the shift register serially to the output, SOD, on falling edges of the shift clock, SCK.

The loading and reading of the data word can be done continuously or in bursts. Since the shift register and latch circuitry inside the device is static, there are no minimum frequency requirements on the clocks or data pulses. However, there is coupling (typically less than 100μV) of the digital signals into the analog section. This coupling can be minimized by clocking the data bursts in during noncritical intervals or at a frequency outside the analog frequency range.

1.6.2 Parallel Mode

The parallel mode is selected by setting SER/$\overline{\text{PAR}}$ pin low. The parallel interface allows the gain settings to be set with external switches or from a parallel microprocessor interface.

In parallel mode, the shift register and latch are bypassed and connections are made directly to the gain select bits with external pins ATTEN/$\overline{\text{GAIN}}$, C3–C0, and F3–F0. Tables 1 and 2 describe how these pins program the gain. The pins ATTEN/$\overline{\text{GAIN}}$, C3–C0, and F3–F0 have internal pulldown resistors to GND. The typical value of these pulldown resistors is 100kΩ.

FUNCTIONAL DESCRIPTION (Continued)

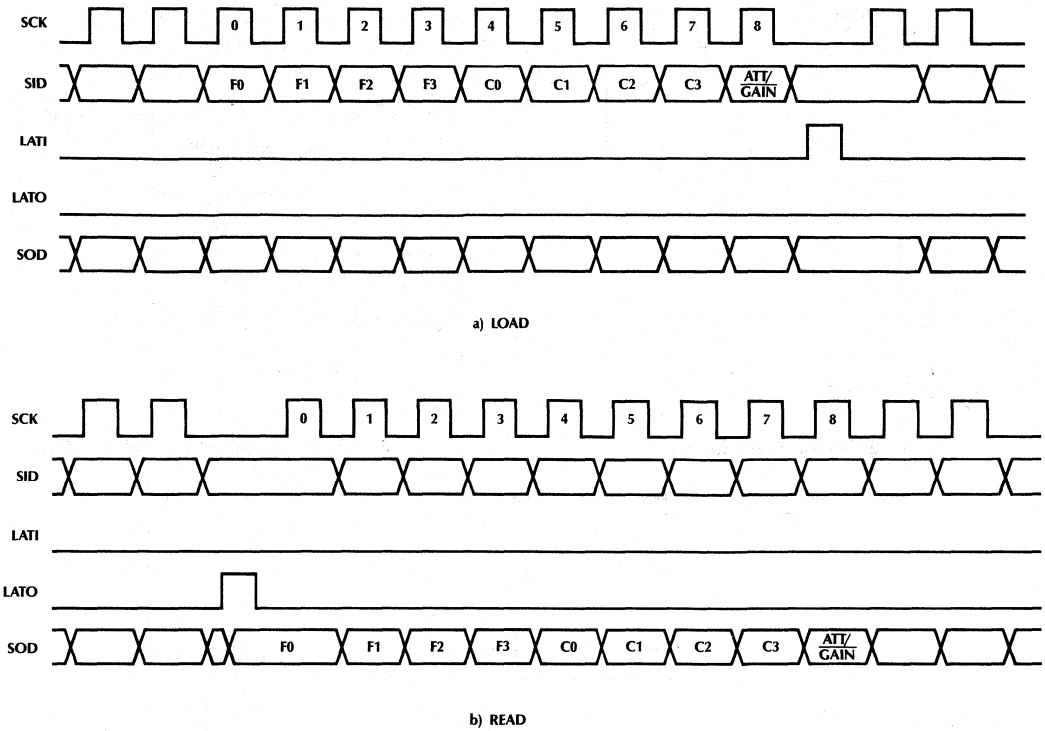


Figure 10. Serial Mode Timing

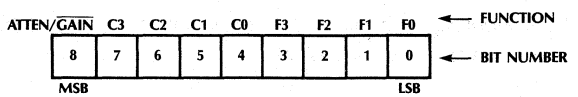


Figure 11. 9-Bit Latch

APPLICATIONS

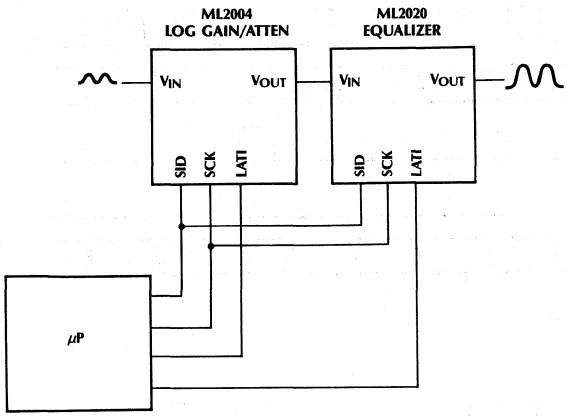


Figure 12. Typical Serial Interface

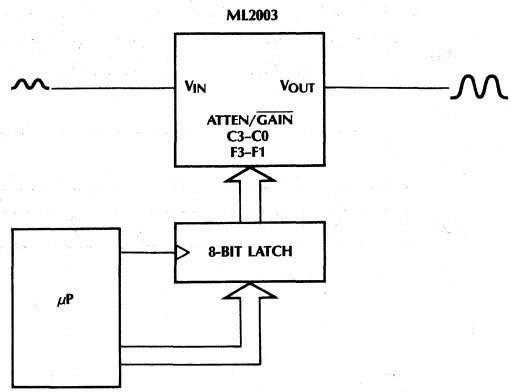


Figure 13. Typical μP Parallel Interface

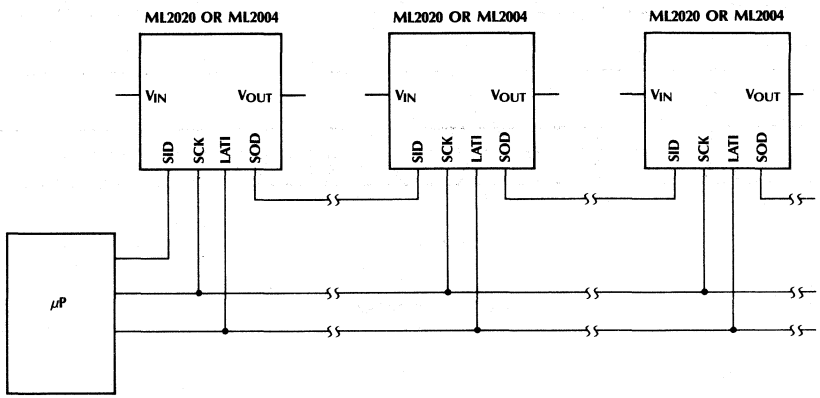


Figure 14. Controlling Multiple ML2020 and ML2004 With Only 3 Digital Lines Using One Long Data Word

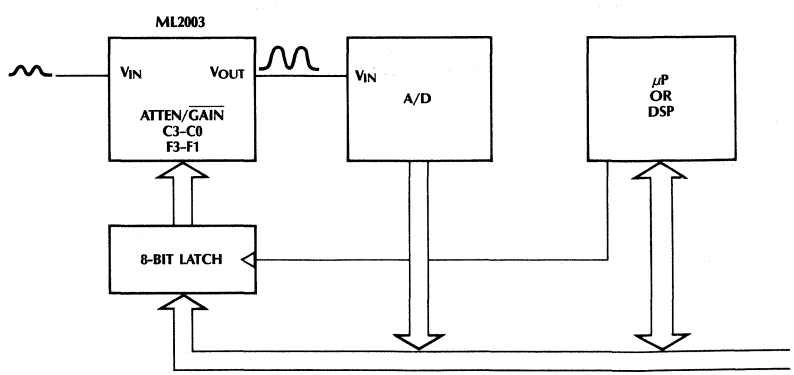


Figure 15. AGC For DSP Or Modem Front End

APPLICATIONS (Continued)

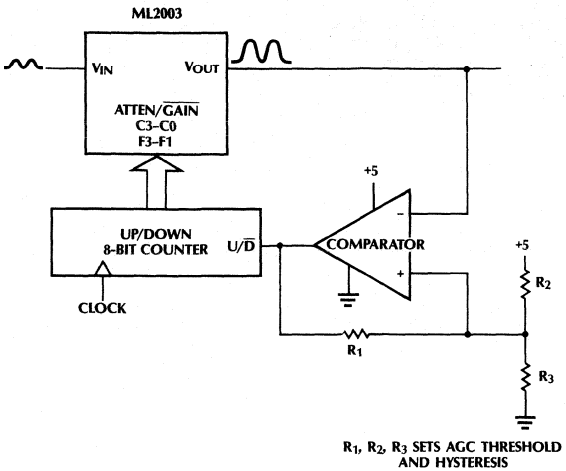


Figure 16. Analog AGC

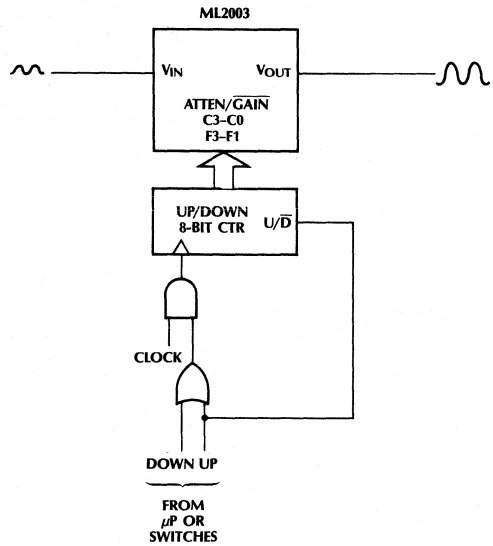


Figure 17. Digitally Controlled Volume Control

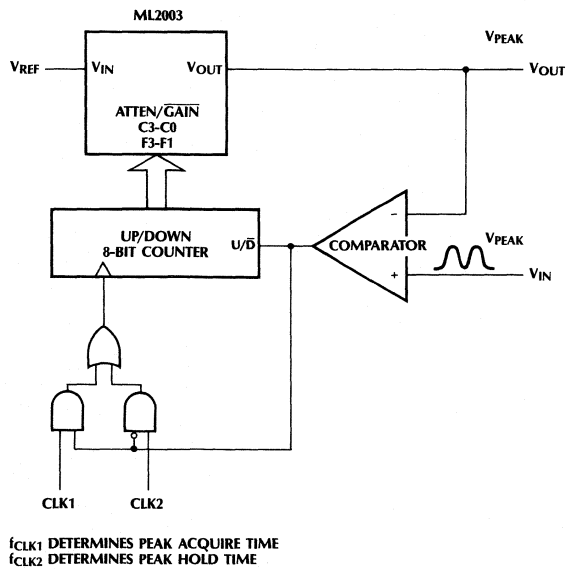


Figure 18. Precision Peak Detector (±1%) with Controllable Acquire and Hold Times

ORDERING INFORMATION

PART NUMBER	PACKAGE	TEMP. RANGE
ML2003IJ	HERMETIC DIP	-40°C to +85°C
ML2003CP	MOLDED DIP	0°C to +70°C
ML2003CQ	MOLDED PCC	0°C to +70°C
ML2004IJ	HERMETIC DIP	-40°C to +85°C
ML2004CP	MOLDED DIP	0°C to +70°C

μP Compatible Logarithmic Gain/Attenuator

GENERAL DESCRIPTION

The ML2008 and ML2009 are digitally controlled logarithmic gain/attenuators with a range of −24 to +24dB in 0.1dB steps.

Easy interface to microprocessors is provided by an input latch and control signals consisting of chip select and write.

The interface for gain setting of the ML2008 is by an 8-bit data word, while the ML2009 is designed to interface to a 16-bit data bus or with an 8-bit data bus with a single write operation by hard-wiring the gain/attenuation pin or LSB pin. The ML2008 can be power downed by the microprocessor utilizing a bit in the second write operation.

Absolute gain accuracy is 0.05dB max over supply tolerance of ±10% and temperature range.

These CMOS logarithmic gain/attenuators are designed for a wide variety of applications in telecom, audio, sonar, or general purpose function generation.

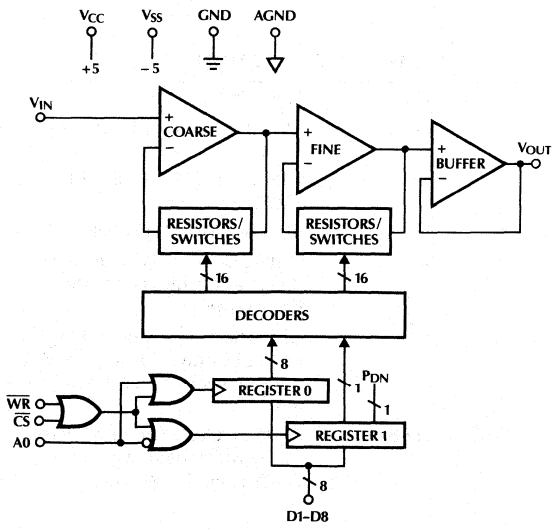
FEATURES

- Low noise 0dBrnc max with +24dB gain
- Low harmonic distortion −60dB max
- Gain range −24 to +24dB
- Resolution 0.1dB steps
- Flat frequency response ±0.05dB from 0.3-4kHz
  ±0.10dB from 0.1-20kHz
- Low supply current 4mA max from ±5V supplies
- TTL/CMOS compatible digital interface
- ML2008 is designed to interface to an 8-bit data bus; ML2009 to 16-bit data bus.
- Standard 18-pin 0.3″ center DIP or 20-pin molded chip carrier package

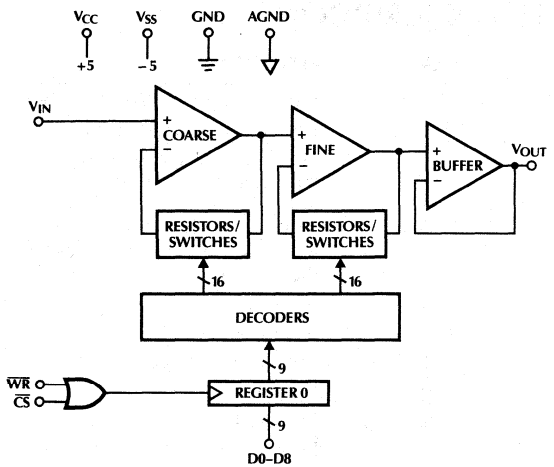
3

BLOCK DIAGRAMS

ML2008



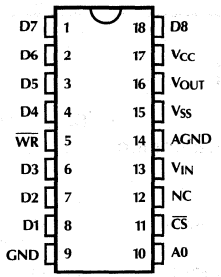
ML2009



PIN CONNECTIONS

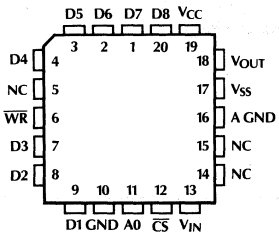
ML2008

18-PIN DIP



TOP VIEW

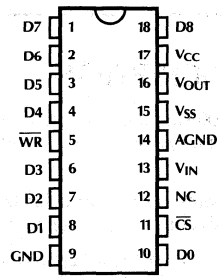
20-PIN PLCC



TOP VIEW

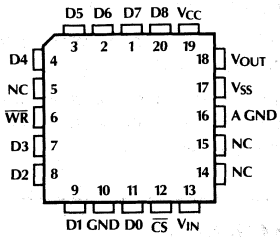
ML2009

18-PIN DIP



TOP VIEW

20-PIN PLCC



TOP VIEW

PIN DESCRIPTION

NAME	FUNCTION
V_{SS}	Negative supply. −5 volts ±10%
V_{CC}	Positive supply. 5 volts ±10%
GND	Digital ground. 0 volts. All digital inputs are referenced to this ground.
AGND	Analog ground. 0 volts. Analog input and output are referenced to this ground.
V_{IN}	Analog input
V_{OUT}	Analog output
D8	Data bit, ATTEN/$\overline{GAIN}$
D7	Data bit, C3
D6	Data bit, C2
D5	Data bit, C1
D4	Data bit, C0
D3	Data bit, F3
D2	Data bit, P_{DN}, F2 ML2008; F2 ML2009
D1	Data bit, F0, F1 ML2008; F1 ML2009
D0	Data bit, F0 ML2009 only
$\overline{WR}$	Write enable. This input latches the data bits into the registers on rising edges of $\overline{WR}$.
$\overline{CS}$	Chip select. This input selects the device by only allowing the $\overline{WR}$ signal to latch in data when $\overline{CS}$ is low.
A0 (ML2008 only)	Address select. This input determines which data word is being written into the registers.

ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage
- V_{CC} ..... +6.5V
- V_{SS} ..... −6.5V
- AGND with Respect to GND ..... V_{CC} to V_{SS}
- Analog Inputs and Outputs ..... V_{SS} −0.3V to V_{CC} +0.3V
- Digital Inputs and Outputs ..... GND −0.3V to V_{CC} +0.3V
- Input Current Per Pin ..... ±25mA
- Power Dissipation 750mW
- Storage Temperature Range ..... −65°C to +150°C
- Lead Temperature (Soldering 10 sec.) ..... 300°C

OPERATING CONDITIONS

Temperature Range (Note 2)
- ML2008CP, ML2009CP ..... 0°C to +70°C
- ML2008CQ, ML2009CQ ..... 0°C to +70°C
- ML2008IJ, ML2009IJ ..... −40°C to +85°C

Supply Voltage
- V_{CC} ..... 4V to 6V
- V_{SS} ..... −4V to −6V

ELECTRICAL CHARACTERISTICS

Unless otherwise specified $T_A = T_{MIN}$ to T_{MAX}, $V_{CC} = 5V \pm 10\%$, $V_{SS} = -5V \pm 10\%$, Data Word: D8 (ATTEN/$\overline{GAIN}$) = 1, Other Bits = 0, (0dB Ideal Gain), $C_L = 100pF$, $R_L = 600\Omega$, dBm measurements use 600Ω as reference load, digital timing measured at 1.4V.

SYMBOL	PARAMETER	NOTES	CONDITIONS	MIN	TYP NOTE 3	MAX	UNITS
ANALOG							
AG	Absolute Gain Accuracy	4	V_{IN} = 8dBm, 1kHz	−0.05		+0.05	dB
RG	Relative Gain Accuracy	4	100000001 000000000 000000001 All other gain settings All values referenced to 100000000 gain when D8 (ATTEN/$\overline{GAIN}$) = 1, V_{IN} = 8dBm when D8 (ATTEN/$\overline{GAIN}$) = 0, V_{IN} = (8dBm − Ideal Gain) in dB	−0.05 −0.05 −0.05 −0.1		+0.05 +0.05 +0.05 +0.1	dB dB dB dB
FR	Frequency Response	4	300-4000Hz 100-20,000Hz Relative to 1kHz	−0.05 −0.1		+0.05 +0.1	dB dB
V_{OS}	Output Offset Voltage	4	V_{IN} = 0, +24dB gain			±100	mV
I_{CN}	Idle Channel Noise	4 5	V_{IN} = 0, +24dB, C msg weighted V_{IN} = 0, +24dB, 1kHz		−6 450	0 900	dBrnc nv/ $\sqrt{Hz}$
HD	Harmonic Distortion	4	V_{IN} = 8dBm, 1kHz Measure 2nd, 3rd, harmonic relative to fundamental			−60	dB
SD	Signal to Distortion	4	V_{IN} = 8dBm, 1kHz C msg weighted	+60			dB
PSRR	Power Supply Rejection	4	200mV$_{p-p}$, 1kHz sine, V_{IN} = 0 on V_{CC} on V_{SS}		 −60 −60	 −40 −40	 dB dB
Z_{IN}	Input Impedance, V_{IN}	4		1			Meg
V_{INR}	Input Voltage Range	4		±3.0			V
V_{OSW}	Output Voltage Swing	4		±3.0			V

3

ELECTRICAL CHARACTERISTICS (Continued)

Unless otherwise specified $T_A = T_{MIN}$ to T_{MAX}, $V_{CC} = 5V \pm 10\%$, $V_{SS} = -5V \pm 10\%$, Data Word: D8 (ATTEN/GAIN) = 1, Other Bits = 0 (0dB Ideal Gain), $C_L = 100pF$, $R_L = 600\Omega$, dBm measurements use 600Ω as reference load, digital timing measured at 1.4V, $C_L = 100pF$.

SYMBOL	PARAMETER	NOTES	CONDITIONS	MIN	TYP NOTE 3	MAX	UNITS
DIGITAL AND DC							
V_{IL}	Digital Input Low Voltage	4				0.8	V
V_{IH}	Digital Input High Voltage	4		2.0			V
I_{IN}	Input Current, Low	4	$V_{IH} = GND$			−10	μA
I_{IN}	Input Current, High	4	$V_{IH} = V_{CC}$			10	μA
I_{CC}	V_{CC} Supply Current	4	No output load, $V_{IL} = GND$, $V_{IH} = V_{CC}$, $V_{IN} = 0$			4	mA
I_{SS}	V_{SS} Supply Current	4	No output load, $V_{IL} = GND$, $V_{IH} = V_{CC}$, $V_{IN} = 0$			−4	mA
I_{CCP}	V_{CC} Supply Current, ML2008 Powerdown Mode Only	4	No output load, $V_{IL} = GND$, $V_{IH} = V_{CC}$			0.5	mA
I_{SSP}	V_{SS} Supply Current, ML2008 Powerdown Mode Only	4	No output load, $V_{IL} = GND$, $V_{IH} = V_{CC}$			−0.1	mA
AC CHARACTERISTICS							
t_{SET}	V_{OUT} Settling Time	4	$V_{IN} = 0.185V$. Change gain from −24 to +24dB. Measure from $\overline{WR}$ rising edge to when V_{OUT} settles to within 0.05dB of final value.			20	μs
t_{STEP}	V_{OUT} Step Response	4	Gain = +24dB. $V_{IN} = -3V$ to +3V step. Measure from $V_{IN} = -3V$ to when V_{OUT} settles to within 0.05dB of final value.			20	μs
t_{DS}	Data Setup Time	4		50			ns
t_{DH}	Data Hold Time	4		50			ns
t_{AS}	A0 Setup Time	4		0			ns
t_{AH}	A0 Hold Time	4		0			ns
t_{CSS}	$\overline{CS}$* Setup Time	4		0			ns
t_{CSH}	$\overline{CS}$* Hold Time	4		0			ns
t_{PW}	$\overline{WR}$* Pulse Width	4		50			ns

Note 1: Absolute maximum ratings are limits beyond which the life of the integrated circuit may be impaired. All voltages unless otherwise specified are measured with respect to ground.

Note 2: 0°C to +70°C and −40°C to +85°C operating temperature range devices are 100% tested with temperature limits guaranteed by 100% testing, sampling, or by correlation with worst-case test conditions.

Note 3: Typicals are parametric norm at 25°C.

Note 4: Parameter guaranteed and 100% production tested.

Note 5: Parameter guaranteed. Parameters not 100% tested are not in outgoing quality level calculation.

TIMING DIAGRAM

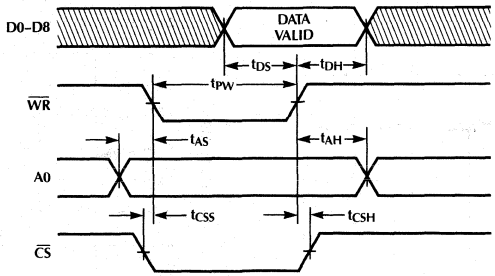


Figure 1. Timing Diagram

TYPICAL PERFORMANCE CURVES

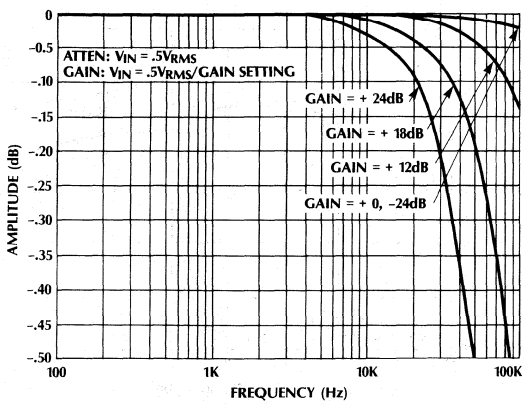


Figure 2. Amplitude vs Frequency ($V_{IN}/V_{OUT} = 0.5V_{RMS}$)

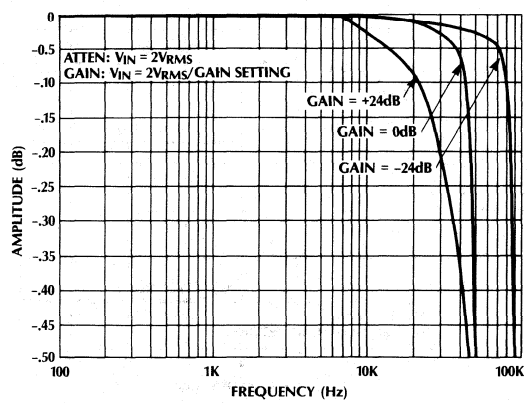


Figure 3. Amplitude vs Frequency ($V_{IN}/V_{OUT} = 2V_{RMS}$)

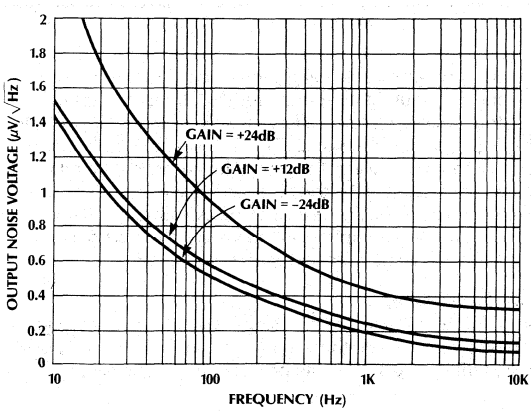


Figure 4. Output Noise Voltage vs Frequency

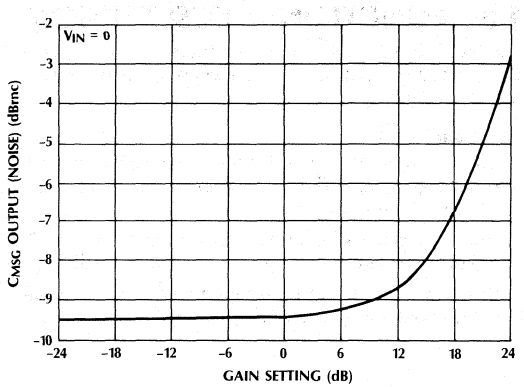


Figure 5. C_{MSG} Output Noise vs Gain Setting

TYPICAL PERFORMANCE CURVES (Continued)

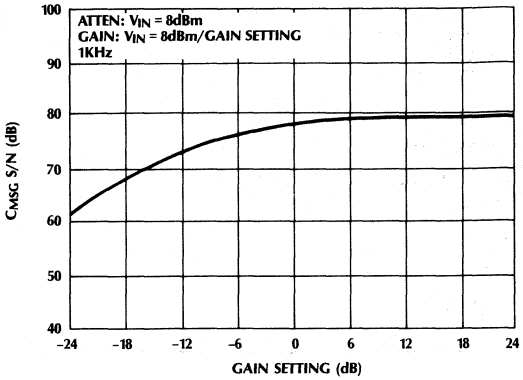


Figure 6. C_{MSG} S/N vs Gain Setting

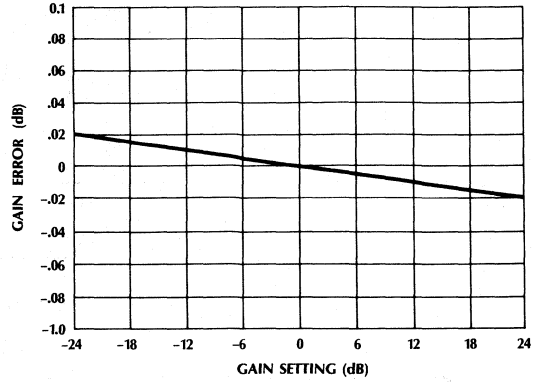


Figure 7. Gain Error vs Gain Setting

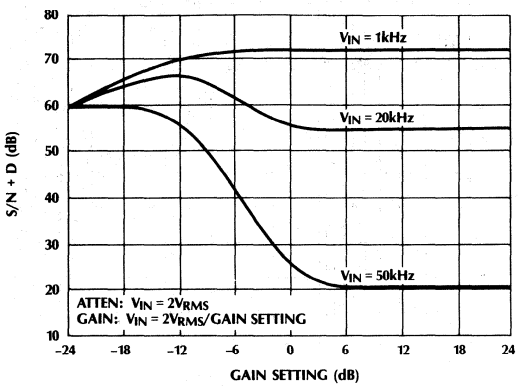


Figure 8. S/N +D vs Gain Setting ($V_{IN}/V_{OUT} = 2V_{RMS}$)

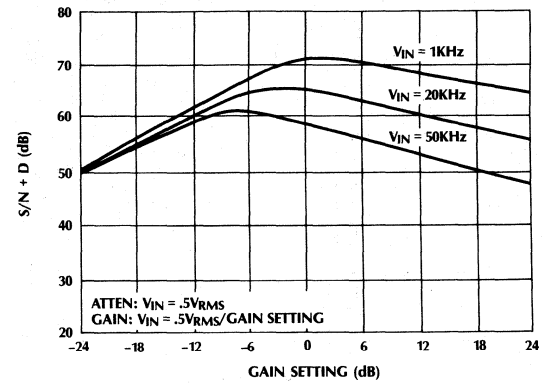


Figure 9. S/N +D vs Gain Setting ($V_{IN}/V_{OUT} = 0.5V_{RMS}$)

1.0 FUNCTIONAL DESCRIPTION

The ML2008, ML2009 consists of a coarse gain stage, a fine gain stage, an output buffer, and a µP compatible parallel digital interface.

1.1 Gain Stages

The analog input, V_{IN}, goes directly into the op amp input in the coarse gain stage. The coarse gain stage has a gain range of 0 to 22.5dB in 1.5dB steps.

The fine gain stage is cascaded onto the coarse section. The fine gain stage has a gain range of 0 to 1.5dB in 0.1dB steps.

Both stages can be programmed for either gain or attenuation, thus doubling the effective gain range.

The logarithmic steps in each gains stage are generated by placing the input signal across a resistor string of 16 series resistors. Analog switches allow the voltage to be tapped from the resistor string at 16 points. The resistors are sized such that each output voltage is at the proper logarithmic ratio relative to the input signal at the top of the string. Attenuation is implemented by using the resistor string as a simple voltage divider, and gain is implemented by using the resistor string as a feedback resistor around an internal op amp.

1.2 Gain Settings

Since the coarse and fine gain stages are cascaded, their gains can be summed logarithmically. Thus, any gain from −24dB to +24dB in 0.1dB steps can be obtained by combining

the coarse and fine gain settings to yield the desired gain setting. The relationship between the register 0 and 1 bits and the corresponding analog gain values is shown in Tables 1 and 2. Note that C3-C0 select the coarse gain, F3-F0 select the fine gain, and ATTEN/$\overline{\text{GAIN}}$ selects either gain or attenuation.

1.3 Output Buffer

The final analog stage is the output buffer. This amplifier has internal gain of 1 and is designed to drive 600Ω, 100pF loads. Thus, it is suitable for driving a telephone hybrid circuit directly without any external amplifier.

1.4 Power Supplies

The digital section is powered between V_{CC} and GND, or 5V. The analog section is powered between V_{CC} and V_{SS} and uses AGND as the reference point, or ±5V.

GND and AGND are totally isolated inside the device to minimize coupling from the digital section into the analog section. Typically this is less than 100μV. However, AGND and GND should be tied together physically near the device and ideally close to the common power supply ground connection.

Typically, the power supply rejection of V_{CC} and V_{SS} to the analog output is greater than −60dB at 1kHz. If decoupling of the power supplies is still necessary in a system, V_{CC} and V_{SS} should be decoupled with respect to AGND.

Table 1. Fine Gain Settings (C3 – C0 = 0)

F3	F2	F1	F0	Ideal Gain (dB) ATTEN/GAIN = 1	Ideal Gain (dB) ATTEN/GAIN = 0
0	0	0	0	0.0	0.0
0	0	0	1	−0.1	0.1
0	0	1	0	−0.2	0.2
0	0	1	1	−0.3	0.3
0	1	0	0	−0.4	0.4
0	1	0	1	−0.5	0.5
0	1	1	0	−0.6	0.6
0	1	1	1	−0.7	0.7
1	0	0	0	−0.8	0.8
1	0	0	1	−0.9	0.9
1	0	1	0	−1.0	1.0
1	0	1	1	−1.1	1.1
1	1	0	0	−1.2	1.2
1	1	0	1	−1.3	1.3
1	1	1	0	−1.4	1.4
1	1	1	1	−1.5	1.5

Table 2. Coarse Gain Settings (F3 – F0 = 0)

C3	C2	C1	C0	Ideal Gain (dB) ATTEN/GAIN = 1	Ideal Gain (dB) ATTEN/GAIN = 0
0	0	0	0	0.0	0.0
0	0	0	1	−1.5	1.5
0	0	1	0	−3.0	3.0
0	0	1	1	−4.5	4.5
0	1	0	0	−6.0	6.0
0	1	0	1	−7.5	7.5
0	1	1	0	−9.0	9.0
0	1	1	1	−10.5	10.5
1	0	0	0	−12.0	12.0
1	0	0	1	−13.5	13.5
1	0	1	0	−15.0	15.0
1	0	1	1	−16.5	16.5
1	1	0	0	−18.0	18.0
1	1	0	1	−19.5	19.5
1	1	1	0	−21.0	21.0
1	1	1	1	−22.5	22.5

3

2.0 DIGITAL INTERFACE

The architecture of the digital section is shown in the preceding block diagram.

The structure of the data registers or latches is shown in Figures 10 and 11 for the ML2008 and ML2009, respectively. The registers control the attenuation/gain setting bits and with the ML2008 the power down bit.

Tables 1 and 2 describe how the data word programs the gain.

The difference between the ML2008 and ML2009 is in the register structure. The ML2008 is a 8-bit data bus version. This device has one 8-bit register and one 2-bit register to store the 9 gain setting bits and 1 powerdown bit. Two write operations are necessary to program the full 10 data bits from eight external data pins. The address pin A0 controls which register is being written into. The powerdown bit, PDN, causes the device to be placed in powerdown. When PDN = 0, the device is powered down. In this state, the power consumption is reduced by removing power from the analog section and forcing the analog output, V_{OUT}, to a high impedance state. While the device is in powerdown, the digital section is still functional and the current data word remains stored in the registers. When PDN = 0, device is in normal operation.

The ML2009 is a 9-bit data bus version. This device has one 9-bit register to store the 9 gain setting bits. The full 9 data bits can be programmed with one write operation from nine external data pins.

The internal registers or latches are edge triggered. The data is transferred from the external pins to the register output on the rising edge of $\overline{\text{WR}}$. The address pin, A0, controls which register the data will be written into as shown in Figures 1 and 2. The $\overline{\text{CS}}$ control signal selects the device by allowing the $\overline{\text{WR}}$ signal to latch in the data only when $\overline{\text{CS}}$ is low. When $\overline{\text{CS}}$ is high, $\overline{\text{WR}}$ is inhibited from latching in new data into the registers.

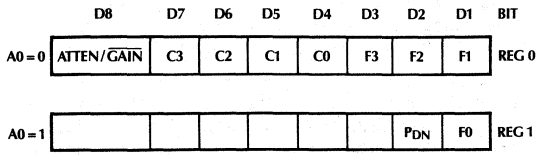


Figure 10. ML2008 Register Structure

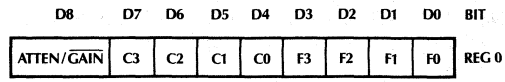


Figure 11. ML2009 Register Structure

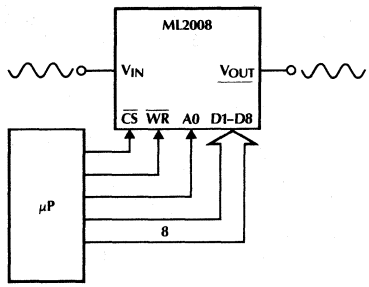


Figure 12. Typical 8-Bit μP Interface, Double Write

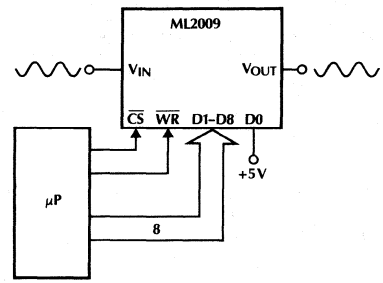


Figure 13. Typical 8-Bit μP Interface, Single Write

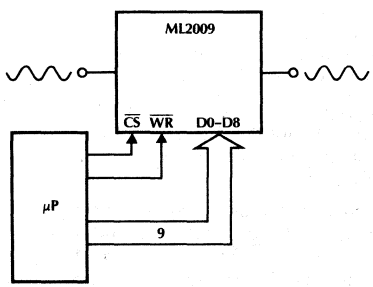


Figure 14. Typical 16-Bit μP Interface

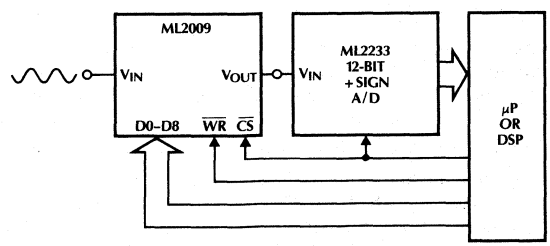


Figure 15. AGC for DSP or Modem Front End

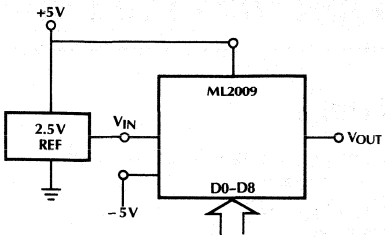


Figure 16. Operation as Logarithmic D/A Converter

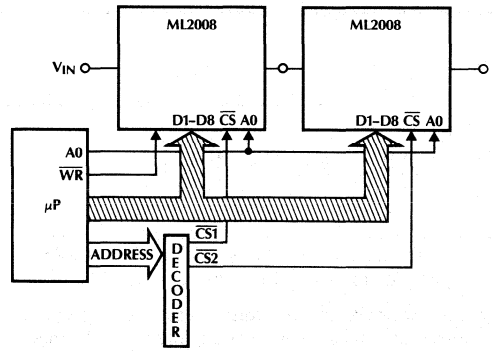


Figure 17. Controlling Multiple Gain/Attenuators

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ML2008IJ	–40°C to +85°C	HERMETIC DIP
ML2008CP	0°C to +70°C	MOLDED DIP
ML2008CQ	0°C to +70°C	MOLDED PCC
ML2009IJ	–40°C to +85°C	HERMETIC DIP
ML2009CP	0°C to +70°C	MOLDED DIP
ML2009CQ	0°C to +70°C	MOLDED PCC

Telephone Line Equalizer

GENERAL DESCRIPTION

The ML2020 is a monolithic analog line equalizer for telephone applications. The ML2020 consists of a switched capacitor filter that realizes a family of frequency response curves optimized for telephone line equalization.

The ML2020 consists of a continuous anti-aliasing filter, a 60 Hz rejection highpass filter section, three programmable switched capacitor equalization filters, an output smoothing filter, a 600Ω driver, and a digital section for the serial interface.

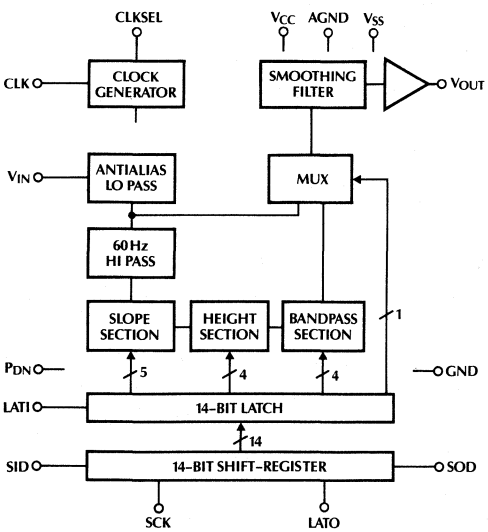
The equalization filters adjust the slope, height, and bandwidth of the frequency response. The desired frequency response is programmed by a digital 14-bit serial input data stream.

The ML2020 is implemented in a double polysilicon CMOS technology.

FEATURES

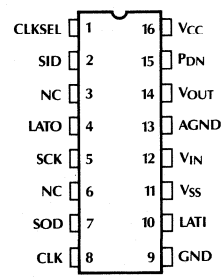
- Slope, height, and bandwidth adjustable
- 60 Hz rejection filter
- On chip anti-alias filter
- Bypass mode
- Low supply current 6 mA typical from ±5 V supplies
- TTL/CMOS compatible interface
- Double buffered data latch
- Selectable master clock 1.544 or 1.536 MHz
- Synchronous or asynchronous data loading capability
- Compatible with ML2003 and ML2004 logarithmic gain/attenuator
- Standard 16-pin 0.3" center molded or hermetic dip and 18-pin SOIC
- 0°C to +70°C and -40°C to +85°C operating temperature range

BLOCK DIAGRAM



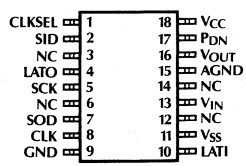
PIN CONNECTIONS

ML2020
16-PIN DIP



TOP VIEW

ML2020
18-PIN SOIC



TOP VIEW

PIN DESCRIPTION

NAME	FUNCTION
CLKSEL	Clock select input. This pin selects the frequency of the CLK input. If CLK is 1.536MHz, set CLKSEL = 1. If CLK is 1.544MHz, set CLKSEL = 0. Pin has an internal pullup resistor to V_{CC}.
SID	Serial input data. Digital input that contains serial data word which controls the filter frequency response setting.
LATO	Output latch clock. Digital input which loads the data word back into the shift register from the latch.
SCK	Shift clock. Digital input which shifts the serial data on SID into the shift register on rising edges and out onto SOD on falling edges.
SOD	Serial output data. Digital output of the shift register.
CLK	Master clock input. Digital input which generates clocks for the switched capacitor filters. Frequency can be either 1.544MHz or 1.536MHz.
GND	Digital ground. 0 volts. All digital inputs and output are referenced to this ground.
LATI	Input latch clock. Digital input which loads data from the shift register into the latch.
V_{SS}	Negative supply. −5 volts ±10%.
V_{IN}	Analog input.
AGND	Analog ground. 0 volts. Analog input and output are referenced to this ground.
V_{OUT}	Analog output.
P_{DN}	Powerdown input. When P_{DN} = 1, device is in powerdown mode. When P_{DN} = 0, device is in normal operation. This pin has an internal pulldown resistor to GND.
V_{CC}	Positive supply. 5 volts ±10%

3

ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage
- V_{CC} ..... +6.5V
- V_{SS} ..... −6.5V
- AGND with Respect to GND ..... ±0.5V
- Analog Input and Output ..... V_{SS} −0.3V to V_{CC} +0.3V
- Digital Input and Outputs ..... GND −0.3V to V_{CC} +0.3V
- Input Current Per Pin ..... ±25mA
- Power Dissipation 750mW
- Storage Temperature Range ..... −65°C to +150°C
- Lead Temperature (Soldering 10 sec.) ..... 300°C

OPERATING CONDITIONS

Temperature Range (Note 2)
- ML2020CP, ML2020CS ..... 0°C to +70°C
- ML2020IJ ..... −40°C to +85°C

Supply Voltage
- V_{CC} ..... 4V to 6V
- V_{SS} ..... −4V to −6V

ELECTRICAL CHARACTERISTICS

Unless otherwise specified $T_A = T_{MIN}$ to T_{MAX}, $V_{CC} = 5V \pm 10\%$, $V_{SS} = -5V \pm 10\%$, Data Word: $\overline{BP} = 1$, Other Bits = 0, $C_L = 100pF$, $R_L = 600\Omega$, dBm measurements use 600Ω as reference load, $V_{IN} = -7dBm$, 1kHz sinusoid CLK = 1.544MHz ±300Hz and digital time measured at 1.4V

SYMBOL	PARAMETER	NOTES	CONDITIONS	MIN	TYP NOTE 3	MAX	UNITS
ANALOG							
SR	Response, Slope Section	4	1kHz response NL/L S3 S2 S1 S0 0 0 0 0 1 0 0 0 1 0 0 0 1 0 0 0 1 0 0 0 0 1 1 1 1 1 0 0 0 0 1 0 0 0 1 1 0 0 1 0 1 0 1 0 0 1 1 0 0 0 1 1 1 1 1 Referenced to 0 0 0 0 0			 1.4±0.1 2.6±0.2 4.7±0.2 7.8±0.2 11.4±0.25 0±0.1 0.4±0.1 0.9±0.2 1.8±0.2 3.7±0.2 6.6±0.25	 dB dB dB dB dB dB dB dB dB dB dB
HR	Response, Height Section	4	3250Hz response referenced to 1kHz response with $\overline{BP} = 1$, other bits = 0 NL/L H3 H2 H1 H0 0 0 0 0 0 0 0 0 0 1 0 0 0 1 0 0 0 1 0 0 0 1 0 0 0 0 1 1 1 1			 0±0.1 0.6±0.2 1.2±0.2 2.4±0.2 5.8±0.3 11.2±0.3	 dB dB dB dB dB dB
BR	Response, Bandwidth Section (Q)	4	NL/L B3 B2 B1 B0 H3 H2 H1 H0 0 0 0 0 0 1 1 1 1 0 0 0 0 1 1 1 1 1 0 0 0 1 0 1 1 1 1 0 0 1 0 0 1 1 1 1 0 1 0 0 0 1 1 1 1 0 1 1 1 1 1 1 1 1			 16.1±2.0 14.2±1.5 12.6±1.5 9.1±1.0 3.6±0.5 1.2±0.35	
PK	BW Peak Frequency	4	H3 thru H0 = 1	3230	3250	3270	Hz
AG	Absolute Gain, Flat Response	4	1 to 4kHz	−0.1	+0.1	+0.3	dB
AGB	Absolute Gain, Bypass Mode	4	0.3 to 4kHz, $\overline{BP} = 0$	−0.1	+0.1	+0.3	dB
ICN	Idle Channel Noise	4	$V_{IN} = 0$		3	8	dBrnc
			V_{IN} = 0, All Data Bits = 1		9		dBrnc

ELECTRICAL CHARACTERISTICS (Continued)

Unless otherwise specified $T_A = T_{MIN}$ to T_{MAX}, $V_{CC} = 5V \pm 10\%$, $V_{SS} = -5V \pm 10\%$, Data Word: $\overline{BP} = 1$, Other Bits = 0, $C_L = 100pF$, $R_L = 600\Omega$, dBm measurements use 600Ω as reference load, $V_{IN} = -7$dBm, 1kHz sinusoid CLK = 1.544MHz ±300Hz and digital time measured at 1.4V

SYMBOL	PARAMETER	NOTES	CONDITIONS	MIN	TYP NOTE 4	MAX	LIMIT UNITS
ANALOG							
HD	Harmonic Distortion	4	V_{IN} = 5dBm, 1kHz Measure 2nd, 3rd, harmonic relative to fundamental			−48	dB
SD	Signal to Distortion	4	V_{IN} = −12dBm, 1kHz C msg weighted	+48			dB
SFN	Single Frequency Noise	5	V_{IN} = 0, 4kHz ≤ frequency ≤ 150kHz			−50	dBm
PSRR	Power Supply Rejection	4	200mV$_{p-p}$, 1kHz sine, V_{IN} = 0 on V_{CC} on V_{SS}			−40 −40	dB dB
Z_{IN}	Input Impedance, V_{IN}	4		100			kΩ
V_{OS}	Output Offset Voltage	4	V_{IN} = 0			±50	mV
V_{INR}	Input Voltage Range	4		±2.0			V
V_{OSW}	Output Voltage Swing	4	R_L = 600Ω	±2.0			V
DIGITAL AND DC							
V_{IL}	Digital Input Low Voltage	4				0.8	V
V_{IH}	Digital Input High Voltage	4		2.0			V
V_{OL}	Digital Output Low Voltage	4	I_{OL} = 2mA			0.4	V
V_{OH}	Digital Output High Voltage	4	I_{OH} = −1mA	4.0			V
I_{LCLK}	Input Current, CLK SEL	4	V_{IN} = 0	5		100	μA
I_{LPDN}	Input Current, PDN	4	$V_{IN} = V_{CC}$	−5		−100	μA
I_L	Input Current, All Other Inputs	4	$V_{IN} = 0 - V_{CC}$			±10	μA
I_{CC}	V_{CC} Supply Current	4	No output load, V_{IL} = GND, $V_{IH} = V_{CC}$, V_{IN} = 0			10	mA
I_{SS}	V_{SS} Supply Current	4	No output load, V_{IL} = GND, $V_{IH} = V_{CC}$, V_{IN} = 0			−10	mA
I_{CCP}	V_{CC} Supply Current, Powerdown Mode	4	No output load, V_{IL} = GND, $V_{IH} = V_{CC}$			1.2	mA
I_{SSP}	V_{SS} Supply Current, Powerdown Mode	4	No output load, V_{IL} = GND, $V_{IH} = V_{CC}$			−1.2	mA
AC CHARACTERISTICS							
t_{DC}	Clock Duty Cycle	5		40		60	%
t_{SCK}	SCK On/Off Period	4		250			ns
t_S	SID Data Setup Time	4		50			ns
t_H	SID Data Hold Time	4		50			ns
t_D	SOD Data Delay	4		0		125	ns
t_{IPW}	LATI Pulse Width	4		50			ns
t_{OPW}	LATO Pulse Width	4		50			ns
t_{IS},t_{OS}	LATI, LATO Setup Time	4		50			ns
t_{IH},t_{OH}	LATI, LATO Hold Time	5		50			ns
t_{PLD}	SOD Parallel Load Delay	4		0		125	ns

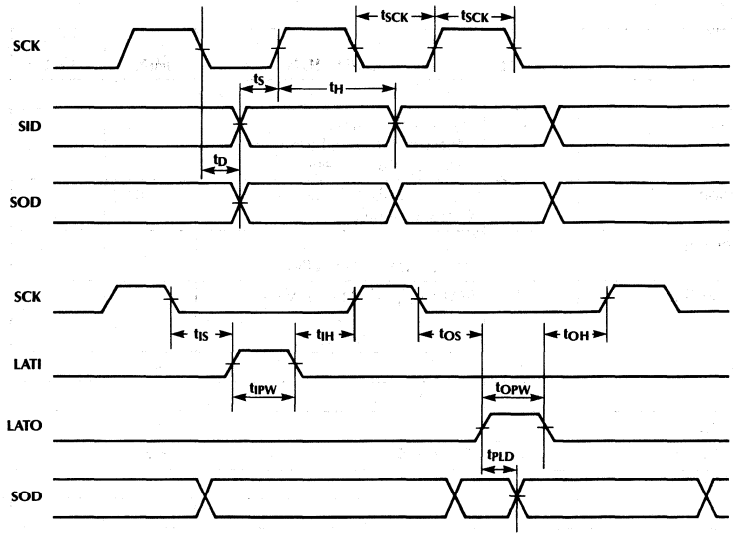
Note 1: Absolute maximum ratings are limits beyond which the life of the integrated circuit may be impaired. All voltages unless otherwise specified are measured with respect to ground.

Note 2: 0°C to +70°C and −40°C to +85°C operating temperature range devices are 100% tested with temperature limits guaranteed by 100% testing, sampling, or by correlation with worst-case test conditions.

Note 3: Typicals are parametric norm at 25°C.

Note 4: Parameter guaranteed and 100% production tested.

Note 5: Parameter guaranteed. Parameters not 100% tested are not in outgoing quality level calculation.



TIMING PARAMETERS ARE REFERENCED TO THE 1.4 VOLT MIDPOINT.

Figure 1. Serial Timing Diagram

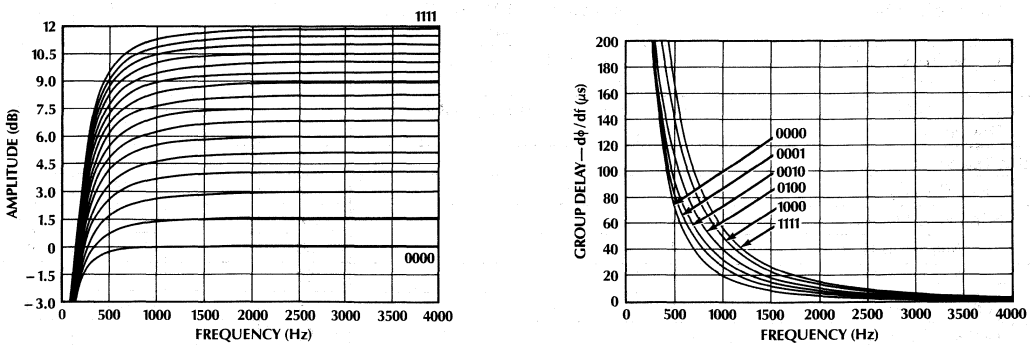


Figure 2. Typical Slope Filter Response — NL/L = 0

B3–B0, H3–H0 = 0000, S3–S0 = 0000 to 1111.

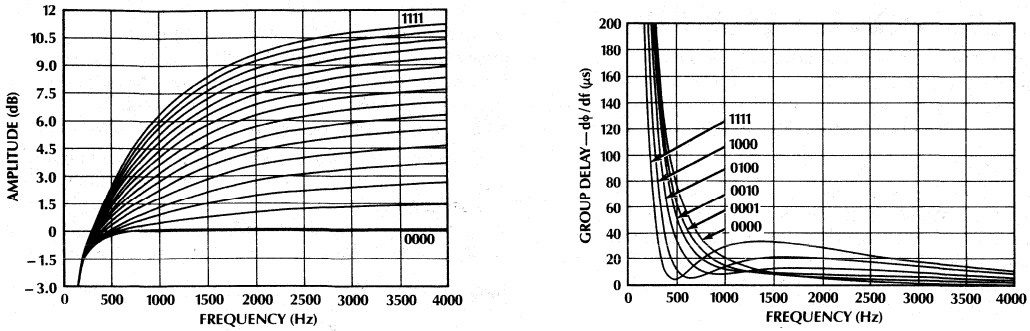


Figure 3. Typical Slope Filter Response — NL/L = 1
B3–B0, H3–H0 = 0000, S3–S0 = 0000 to 1111.

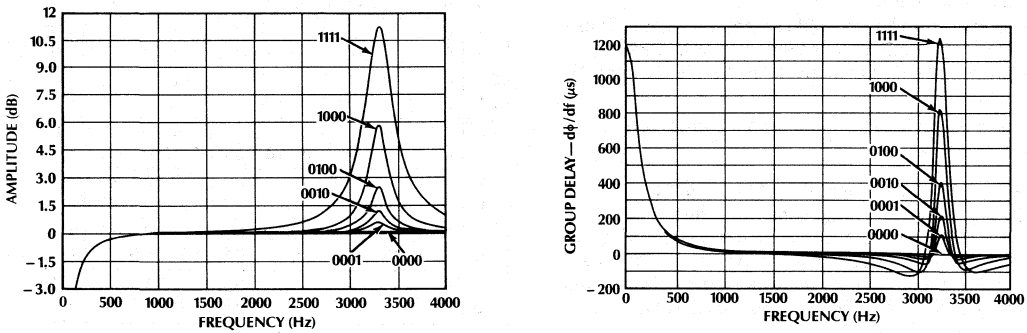


Figure 4. Typical Height Filter Response — NL/L = 0
B3–B0, S3–S0 = 0000; H3–H0 = 0000 to 1111.

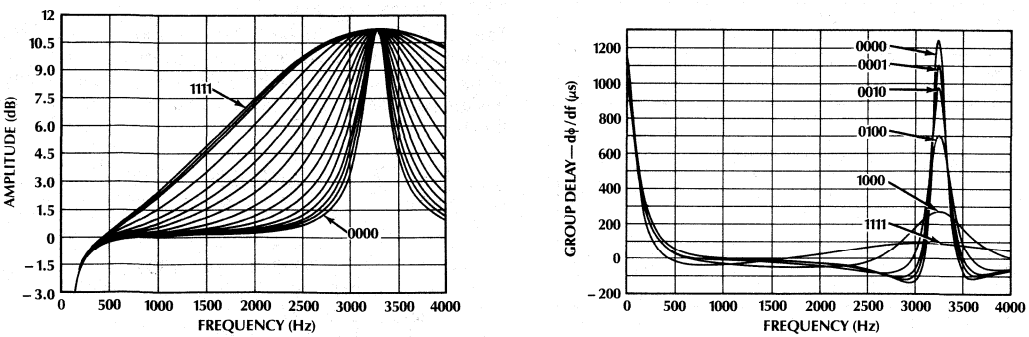


Figure 5. Typical Bandwidth Filter Response — NL/L = 0
H3–H0 = 1111; S3–S0 = 0000; B3–B0 = 0000 to 1111.

1.0 FUNCTIONAL DESCRIPTION

The ML2020 consists of a continuous anti-alias filter, a 60 Hz reject highpass filter section, three programmable switched capacitor equalization filters, an output smoothing filter, an output driver, and a digital section for the serial interface.

1.1 Anti-Alias Filter

The first section is a continuous anti-alias filter. This filter is needed to prevent aliasing of high frequency signals present on the input into the passband by the sampling action of the switched capacitor filters. This section is a continuous second order lowpass filter with a typical 3 dB frequency at 20 kHz and 30 dB of rejection at 124 kHz.

1.2 60 Hz Rejection Filter

The 60 Hz section is a highpass switched capacitor filter designed to reject DC offsets and low frequency signals present on the input. This filter is a first order section with a typical 3 dB frequency at 135 Hz.

1.3 Equalization Filters

The equalizer filters follow the 60 Hz highpass section. These programmable filters implement a family of frequency response curves intended to compensate for the response of telephone lines.

This filter is composed of three distinct sections: slope, height, and bandwidth.

1.3.1 Response of Slope, Height, and Bandwidth

The family of response curves generated by the slope section are shown in Figures 2 and 3. There are 4 slope select bits, S3-S0. These bits alter the slope of the highpass response under 1000 Hz, and as a result, the absolute gain above 1000 Hz will be unique for each setting. Table 1 gives typical 1 kHz gain values for all slope settings.

Table 1. Typ. 1 kHz Gain for Slope Settings

Slope Setting	Rel 1 kHz Gain (dB)	
	NL/L = 1	NL/L = 0
0	0.0	Rel
1	0.4	1.4
2	0.9	2.6
3	1.4	3.7
4	1.8	4.7
5	2.3	5.5
6	2.8	6.3
7	3.4	7.2
8	3.7	7.8
9	4.2	8.4
10	4.6	9.0
11	5.0	9.5
12	5.4	10.0
13	5.8	10.5
14	6.2	11.0
15	6.6	11.4

HT, BW Bits = 0

There is an additional bit, NL/L, that also affects the highpass response of the slope filter. The slope response curves in Figure 2 are with NL/L = 0. These same response curves are shown in Figure 3 with NL/L = 1. Notice that the NL/L bit adds more droop in the highpass response below 2500 Hz.

The family of response curves generated by the height section are shown in Figure 4. There are 4 height select bits, H3-H0. This section creates a peak in the response at 3250 Hz and this filter controls the amount of peaking. Table 2 gives typical 1 kHz gain values for all height and bandwidth settings.

Table 2. Typ. 1 kHz Gain for HT and BW Settings

	Relative 1 kHz Gain (dB)															
	HT Setting															
BW Setting	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	Rel	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
3	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0.1
5	0	0	0	0	0	0	0	0	0	0	0	0	0.1	0.1	0.1	0.1
6	0	0	0	0	0	0	0	0	0	0	0.1	0.1	0.1	0.1	0.1	0.1
7	0	0	0	0	0	0	0	0	0.1	0.1	0.1	0.1	0.1	0.2	0.2	0.2
8	0	0	0	0	0	0	0.1	0.1	0.1	0.1	0.1	0.2	0.2	0.3	0.3	0.4
9	0	0	0	0	0	0.1	0.1	0.1	0.1	0.2	0.2	0.3	0.3	0.4	0.5	0.6
10	0	0	0	0	0.1	0.1	0.1	0.1	0.2	0.3	0.3	0.4	0.5	0.6	0.7	0.8
11	0	0	0	0.1	0.1	0.1	0.2	0.2	0.3	0.4	0.4	0.5	0.7	0.8	0.9	1.1
12	0	0	0.1	0.1	0.1	0.2	0.2	0.3	0.4	0.5	0.7	0.8	1.0	1.1	1.4	1.6
13	0	0	0.1	0.1	0.2	0.3	0.4	0.5	0.6	0.8	0.9	1.1	1.4	1.6	1.9	2.3
14	0	0	0.1	0.1	0.2	0.3	0.4	0.5	0.7	0.8	1.0	1.2	1.5	1.7	2.0	2.4
15	0	0	0.1	0.1	0.2	0.3	0.4	0.5	0.7	0.9	1.1	1.3	1.6	1.8	2.1	2.5

Slope Bits = 0

The family of response curves generated by the bandwidth section is shown in Figure 5 There are 4 bandwidth select bits, B3-B0. This section causes the response of the 3250 Hz peak to be widened, and as a result, this filter controls the bandwidth of the 3250 Hz peaked region.

1.3.2 Transfer Function

The transfer function for the ML2020 is shown below. This transfer function is valid for magnitude response only. The actual magnitude response from an individual device may deviate from the computed response from the transfer function by typically 0–0.2 dB.

$$H(s) = \frac{-s}{s+a} \times \frac{c(s+b)}{b(s+c)} \times \frac{\left[s^2 + h(\omega_o/Q)s + \omega_o^2\right]}{\left[s^2 + (\omega_o/Q)s + \omega_o^2\right]} \times \frac{\left[\sin(\pi f/fc)\right]}{(\pi f/fc)}$$

$$s = j \times 256000 \times \tan(\pi f/128000)$$
$$a = 848.230$$
$$\omega_o = 20463.77$$
$$fc = 128000$$

b,c : See Table 3. (slope)
Q : See Table 4. (bandwidth)
h : See Table 5. (height)

Table 3. Slope Response Factors (b, c)

S3–0	b NL/L = 0	b NL/L = 1
0000	2.371759E+03	1.116280E+04
0001	1.985920E+03	9.345141E+03
0010	1.701779E+03	8.007156E+03
0011	1.493571E+03	7.026999E+03
0100	1.326721E+03	6.241681E+03
0101	1.196668E+03	5.629636E+03
0110	1.087277E+03	5.114881E+03
0111	9.983588E+02	4.696487E+03
1000	9.179889E+02	4.318339E+03
1001	8.537864E+02	4.016273E+03
1010	7.966049E+02	3.747249E+03
1011	7.478074E+02	3.517676E+03
1100	7.035099E+02	3.309279E+03
1101	6.651771E+02	3.128945E+03
1110	6.299477E+02	2.963214E+03
1111	5.990361E+02	2.817797E+03

S3–0	c NL/L = 0	c NL/L = 1
XXXX	2.371759E+03	1.116280E+04

Table 4. Slope Response Factors (b, c)

B3–0	Q
0000	17.444906
0001	15.386148
0010	13.652451
0011	11.593677
0100	9.859960
0101	8.017864
0110	6.392453
0111	5.092080
1000	3.900003
1001	3.141338
1010	2.599369
1011	2.165724
1100	1.731965
1101	1.406509
1110	1.352248
1111	1.297981

Table 5. Height Response Factors (h)

Code	h
0000	1.000000
0001	1.071519
0010	1.148154
0011	1.230269
0100	1.318257
0101	1.445438
0110	1.603245
0111	1.757924
1000	1.949845
1001	2.137962
1010	2.317395
1011	2.540973
1100	2.786121
1101	3.019951
1110	3.311311
1111	3.672823

1.4 Smoothing Filter

The equalizer filters are followed by a continuous second order smoothing filter that removes the high frequency sample information generated by the action of the switched capacitor filters. This filter provides a continuous analog signal at the output, V_{OUT} .

1.5 Output Buffer

The final stage in the ML2020 is the output buffer. This amplifier has internal gain of 1 and is capable of driving 600Ω, 100pF loads. Thus, it is suitable for driving telephone hybrids directly without any external amplifier.

1.6 Bypass Mode

The filter sections can be bypassed by setting the bypass data bit, $\overline{BP}$, to 0. Since the switched capacitor filters are bypassed in this mode, frequency response effects of the switched capacitor filters are eliminated. Thus, this mode offers very flat response and low noise over the 300–4000Hz frequency range.

1.7 Filter Clock

The master clock, CLK, is used to generate the internal clocks for the switched capacitor filters. The frequency of CLK can be either 1.544MHz or 1.536MHz. However, the internal clock frequency must be kept at 1.536MHz to guarantee accurate frequency response. The CLKSEL pin enables a bit swallower circuit to keep the internal clock frequency set to 1.536MHz. When 1.544MHz clock is used, CLKSEL should be set to logic level 0, and one bit out of every 193 bits is removed (swallowed) to reduce the internal frequency to 1.536MHz. When 1.536MHz clock is used, CLKSEL should be set to logic level 1, and the internal clock rate is the same as the external clock rate.

1.8 Serial Interface

The architecture of the digital section is shown in the preceding block diagram.

A timing diagram for the serial interface is shown in Figure 6. The serial input data, SID, is loaded into a shift register on rising edges of the shift clock, SCK. The data word is parallel loaded into a latch when the input latch signal, LATI, is high. The LATI pulse must occur when SCK is low. A new data word can be loaded into the shift register without disturbing the existing data word in the latch.

The parallel outputs of the latch control the filter response curves. The order of the data word bits in the latch is shown in Figure 7.

Note that bit 0 is the first bit of the data word clocked into the shift register.

The device has the capability to read out the data word stored in the latch. This is done by parallel loading the data from the latch back into the shift register when the latch signal, LATO, is high. The LATO pulse must occur when SCK is low. Then, the data word can be shifted out of the register serially to the output, SOD, on falling edges of the shift clock, SCK.

The loading and reading of the data word can be done continuously or in bursts. Since the shift register and latch

circuitry inside the device is static, there are no minimum frequency requirements on the clocks or data pulses. However, there is some coupling of the digital signals into the analog section. If this coupling is undesirable, the data can be clocked in bursts during non critical intervals, or the data rate can be done at a frequency outside the analog frequency range.

The clocks used to shift and latch data (SCK, LATI, LATO) are not related internally to the master clock and can occur asynchronous to CLK.

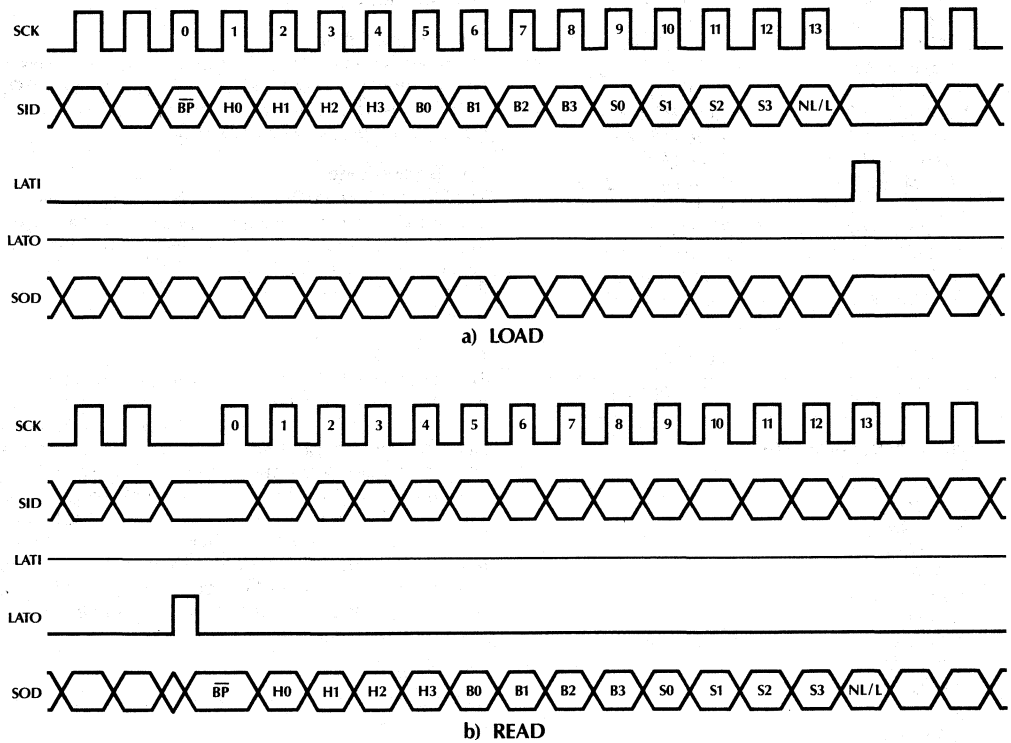


Figure 6. Serial Timing

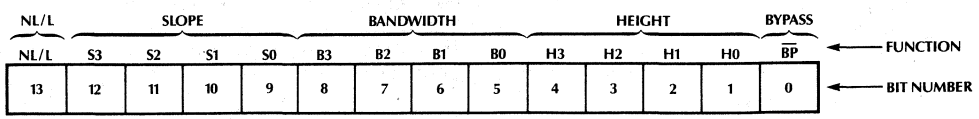


Figure 7. 14-Bit Latch

POWERDOWN MODE

A powerdown mode can be selected with pin P_{DN}. When $P_{DN}=1$, the device is powered down. In this state, the power consumption is reduced by removing power from the analog section and forcing the analog output, V_{OUT}, to a high impedance state. While the device is in power down mode, the digital section is still functional and the current data word remains stored in the latch. The master clock, CLK, can be left active or removed during powerdown mode. When $P_{DN}=0$, the device is in normal operation.

POWER SUPPLIES

The digital section inside the device is powered between V_{CC} and GND, or 5 volts. The analog section is powered between V_{CC} and V_{SS}, or ±5 volts. The analog section uses AGND as the reference point.

GND and AGND are totally isolated inside the device to minimize coupling from the digital section into the analog section. Typically this is less than 100µV. However, AGND and GND should be tied together physically near the device and close to the common power supply ground connection.

The power supply rejection of V_{CC} and V_{SS} to the analog output is greater than −60dB at 1kHz, typically. If decoupling of the power supplies is still necessary in a system, V_{CC} and V_{SS} should be decoupled with respect to AGND.

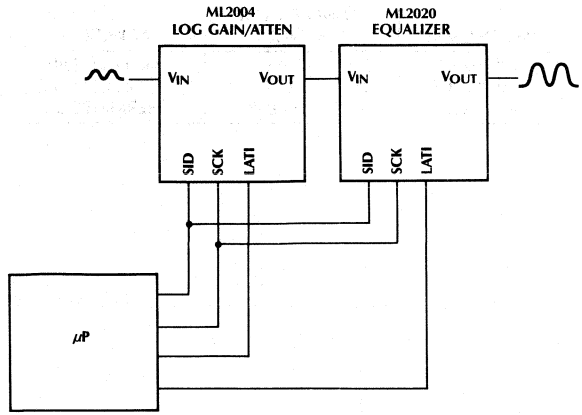


Figure 8. Typical Serial Interface

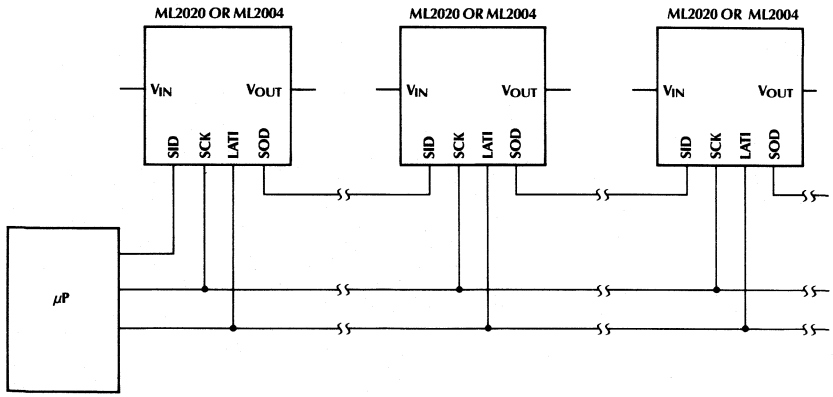


Figure 9. Controlling Multiple ML2020 and ML2004 With Only 3 Digital Lines Using One Long Data Word

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ML2020CP	0° C to +70° C	MOLDED DIP
ML2020CS	0° C to +70° C	MOLDED SOIC
ML2020IJ	−40° C to +85° C	HERMETIC DIP

Telephone Line Equalizer

GENERAL DESCRIPTION

The ML2021 is a monolithic analog line equalizer for telephone applications. The ML2021 consists of a switched capacitor filter that realizes a family of frequency response curves optimized for telephone line amplitude equalization while minimizing group delay. This ML2021 is the same function as the ML2020 telephone equalizer without the 60Hz rejection filter.

The ML2021 consists of a continuous anti-aliasing filter, three programmable switched capacitor equalization filters, an output smoothing filter, a 600Ω driver, and a digital section for the serial interface.

The equalization filters adjust the slope, height, and band-width of the frequency response. The desired frequency response is programmed by a digital 14-bit serial input data stream.

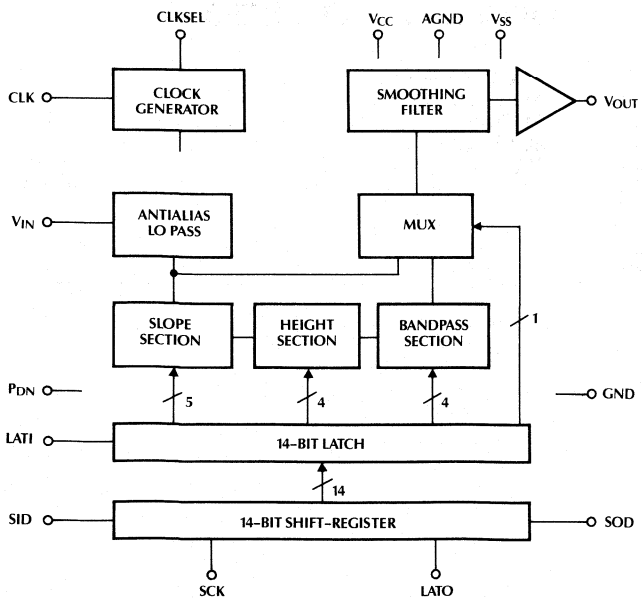
The ML2021 is implemented in a double polysilicon CMOS technology.

FEATURES

- Slope, height, and bandwidth adjustable
- Optimized group delays (500 Hz to 6.4 kHz)
- On chip anti-alias filter
- Bypass mode
- Low supply current 6mA typical from ±5V supplies
- TTL/CMOS compatible interface
- Double buffered data latch
- Selectable master clock 1.544 or 1.536 MHz
- Synchronous or asynchronous data loading capability
- Compatible with ML2003 and ML2004 logarithmic gain/attenuator
- Standard 16-pin 0.3" center molded or hermetic DIP and 18-pin SOIC
- 0°C to +70°C and –40°C to +85°C operating temperature range

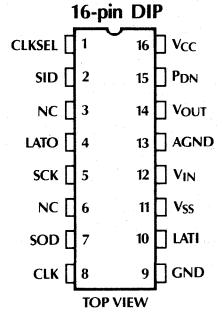
3

BLOCK DIAGRAM



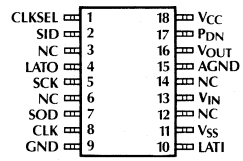
PIN CONNECTIONS

ML2021
16-pin DIP



TOP VIEW

ML2021
18-pin SOIC



TOP VIEW

PIN DESCRIPTION

NAME	FUNCTION
CLKSEL	Clock select input. This pin selects the frequency of the CLK input. If CLK is 1.536 MHz, set CLKSEL = 1. If CLK is 1.544 MHz, set CLKSEL = 0. Pin has an internal pullup resistor to V_{CC}.
SID	Serial input data. Digital input that contains serial data word which controls the filter frequency response setting.
LATO	Output latch clock. Digital input which loads the data word back into the shift register from the latch.
SCK	Shift clock. Digital input which shifts the serial data on SID into the shift register on rising edges and out onto SOD on falling edges.
SOD	Serial output data. Digital output of the shift register.
CLK	Master clock input. Digital input which generates clocks for the switched capacitor filters. Frequency can be either 1.544 MHz or 1.536 MHz.
GND	Digital ground. 0 volts. All digital inputs and output are referenced to this ground.
LATI	Input latch clock. Digital input which loads data from the shift register into the latch.
V_{SS}	Negative supply. −5 volts ±10%.
V_{IN}	Analog input.
AGND	Analog ground. 0 volts. Analog input and output are referenced to this ground.
V_{OUT}	Analog output.
P_{DN}	Powerdown input. When $P_{DN} = 1$, device is in powerdown mode. When $P_{DN} = 0$, device is in normal operation. This pin has an internal pulldown resistor to GND.
V_{CC}	Positive supply. 5 volts ±10%

ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage
- V_{CC} ..... +6.5 V
- V_{SS} ..... −6.5 V
- AGND with Respect to GND ..... ±0.5 V
- Analog Input and Output ..... V_{SS} −0.3 V to V_{CC} +0.3 V
- Digital Input and Outputs ..... GND −0.3 V to V_{CC} +0.3 V
- Input Current Per Pin ..... ±25 mA
- Power Dissipation ..... 750 mW
- Storage Temperature Range ..... −65° C to +150° C
- Lead Temperature (Soldering 10 sec.) ..... 300° C

OPERATING CONDITIONS

Temperature Range (Note 2)
- ML2021CP, ML2021CS ..... 0° C to +70° C
- ML2021IJ ..... −40° C to +85° C

Supply Voltage
- V_{CC} ..... 4 V to 6 V
- V_{SS} ..... −4 V to −6 V

ELECTRICAL CHARACTERISTICS

Unless otherwise specified $T_A = T_{MIN}$ to T_{MAX}, $V_{CC} = 5V \pm 10\%$, $V_{SS} = -5V \pm 10\%$, Data Word: $\overline{BP} = 1$, Other Bits = 0, $C_L = 100pF$, $R_L = 600\Omega$, dBm measurements use 600Ω as reference load, $V_{IN} = -7dBm$, 1kHz sinusoid CLK = 1.544MHz ±300Hz and digital time measured at 1.4V

SYMBOL	PARAMETER	NOTES	CONDITIONS	MIN	TYP NOTE 3	MAX	UNITS
ANALOG							
SR	Response, Slope Section	4	1kHz response				
			NL/L S3 S2 S1 S0				
			0 0 0 0 1			1.4 ±0.1	dB
			0 0 0 1 0			2.6 ±0.2	dB
			0 0 1 0 0			4.7 ±0.2	dB
			0 1 0 0 0			7.8 ±0.2	dB
			0 1 1 1 1			11.4 ±0.25	dB
			1 0 0 0 0			0 ±0.1	dB
			1 0 0 0 1			0.4 ±0.1	dB
			1 0 0 1 0			0.9 ±0.2	dB
			1 0 1 0 0			1.8 ±0.2	dB
			1 1 0 0 0			3.7 ±0.2	dB
			1 1 1 1 1			6.6 ±0.25	dB
			Referenced to				
			0 0 0 0 0				
HR	Response, Height Section	4	3250Hz response referenced to 1kHz response with $\overline{BP} = 1$, other bits = 0				
			NL/L H3 H2 H1 H0				
			0 0 0 0 0			0 ± 0.1	dB
			0 0 0 0 1			0.5 ± 0.2	dB
			0 0 0 1 0			1.1 ± 0.2	dB
			0 0 1 0 0			2.3 ± 0.2	dB
			0 1 0 0 0			5.7 ± 0.3	dB
			0 1 1 1 1			11.1 ± 0.3	dB
BR	Response, Bandwidth Section (Q)	4	NL/L B3 B2 B1 B0 H3 H2 H1 H0				
			0 0 0 0 0 1 1 1 1			16.1 ±2.0	
			0 0 0 0 1 1 1 1 1			14.2 ±1.5	
			0 0 0 1 0 1 1 1 1			12.6 ±1.5	
			0 0 1 0 0 1 1 1 1			9.1 ±1.0	
			0 1 0 0 0 1 1 1 1			3.6 ±0.5	
			0 1 1 1 1 1 1 1 1			1.2 ±0.35	
PK	BW Peak Frequency	4	H3 thru H0 = 1	3230	3250	3270	Hz
AG	Absolute Gain, Flat Response	4	.5 to 4kHz	−0.1	+0.1	+0.3	dB
AGB	Absolute Gain, Bypass Mode	4	0.3 to 4kHz, $\overline{BP} = 0$	−0.1	+0.1	+0.3	dB
ICN	Idle Channel Noise	4	$V_{IN} = 0$		3	8	dBrnc
			$V_{IN} = 0$, all data bits = 1		9		dBrnc

3

ELECTRICAL CHARACTERISTICS (Continued)

Unless otherwise specified $T_A = T_{MIN}$ to T_{MAX}, $V_{CC} = 5V \pm 10\%$, $V_{SS} = -5V \pm 10\%$, Data Word: $\overline{BP} = 1$, Other Bits = 0, $C_L = 100pF$, $R_L = 600\Omega$, dBm measurements use 600Ω as reference load, $V_{IN} = -7dBm$, 1kHz sinusoid CLK = 1.544MHz ±300Hz and digital time measured at 1.4V

SYMBOL	PARAMETER	NOTES	CONDITIONS	MIN	TYP NOTE 3	MAX	LIMIT UNITS
ANALOG							
HD	Harmonic Distortion	4	$V_{IN} = 5dBm$, 1kHz Measure 2nd, 3rd, harmonic relative to fundamental			−48	dB
SD	Signal to Distortion	4	$V_{IN} = -12dBm$, 1kHz C msg weighted	+48			dB
SFN	Single Frequency Noise	5	$V_{IN} = 0$, $4kHz \leq$ frequency $\leq 150kHz$			−50	dBm
PSRR	Power Supply Rejection	4	$200mV_{p-p}$, 1kHz sine, $V_{IN} = 0$ on V_{CC} on V_{SS}			−40 −40	dB dB
Z_{IN}	Input Impedance, V_{IN}	4		100			kΩ
V_{OS}	Output Offset Voltage	4	$V_{IN} = 0$			±50	mV
V_{INR}	Input Voltage Range	4		±2.0			V
V_{OSW}	Output Voltage Swing	4	$R_L = 600\Omega$	±2.0			V
DIGITAL AND DC							
V_{IL}	Digital Input Low Voltage	4				0.8	V
V_{IH}	Digital Input High Voltage	4		2.0			V
V_{OL}	Digital Output Low Voltage	4	$I_{OL} = 2mA$			0.4	V
V_{OH}	Digital Output High Voltage	4	$I_{OH} = -1mA$	4.0			V
I_{LCLK}	Input Current, CLK SEL	4	$V_{IN} = 0$	5		100	μA
I_{LPDN}	Input Current, PDN	4	$V_{IN} = V_{CC}$	−5		−100	μA
I_L	Input Current, All Other Inputs	4	V_{IN} = 0 to V_{CC}			±10	μA
I_{CC}	V_{CC} Supply Current	4	No output load, V_{IL} = GND, $V_{IH} = V_{CC}$, $V_{IN} = 0$			10	mA
I_{SS}	V_{SS} Supply Current	4	No output load, V_{IL} = GND, $V_{IH} = V_{CC}$, $V_{IN} = 0$			−10	mA
I_{CCP}	V_{CC} Supply Current, Powerdown Mode	4	No output load, V_{IL} = GND, $V_{IH} = V_{CC}$			1.2	mA
I_{SSP}	V_{SS} Supply Current, Powerdown Mode	4	No output load, V_{IL} = GND, $V_{IH} = V_{CC}$			−1.2	mA
AC CHARACTERISTICS							
t_{DC}	Clock Duty Cycle	5		40		60	%
t_{SCK}	SCK On/Off Period	4		250			ns
t_S	SID Data Setup Time	4		50			ns
t_H	SID Data Hold Time	4		50			ns
t_D	SOD Data Delay	4		0		125	ns
t_{IPW}	LATI Pulse Width	4		50			ns
t_{OPW}	LATO Pulse Width	4		50			ns
t_{IS}, t_{OS}	LATI, LATO Setup Time	4		50			ns
t_{IH}, t_{OH}	LATI, LATO Hold Time	5		50			ns
t_{PLD}	SOD Parallel Load Delay	4		0		125	ns

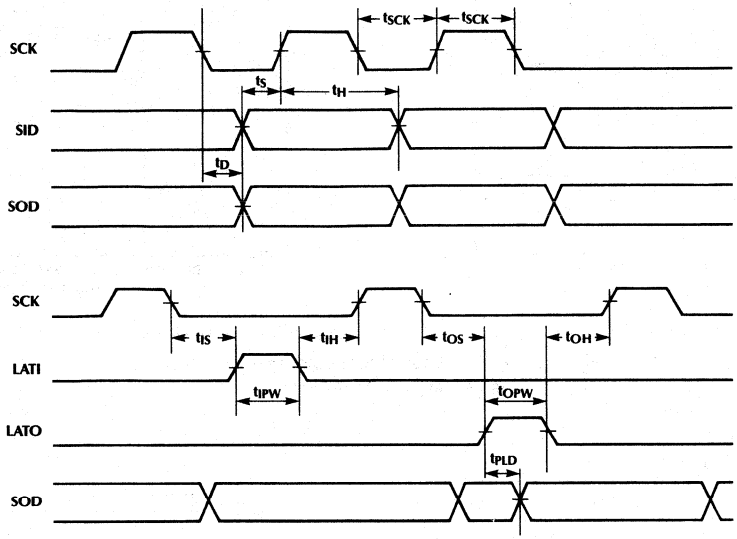
Note 1: Absolute maximum ratings are limits beyond which the life of the integrated circuit may be impaired. All voltages unless otherwise specified are measured with respect to ground.

Note 2: 0°C to +70°C and −40°C to +85°C operating temperature range devices are 100% tested with temperature limits guaranteed by 100% testing, sampling, or by correlation with worst-case test conditions.

Note 3: Typicals are parametric norm at 25°C.

Note 4: Parameter guaranteed and 100% production tested.

Note 5: Parameter guaranteed. Parameters not 100% tested are not in outgoing quality level calculation.



TIMING PARAMETERS ARE REFERENCED TO THE 1.4 VOLT MIDPOINT.

Figure 1. Serial Timing Diagram

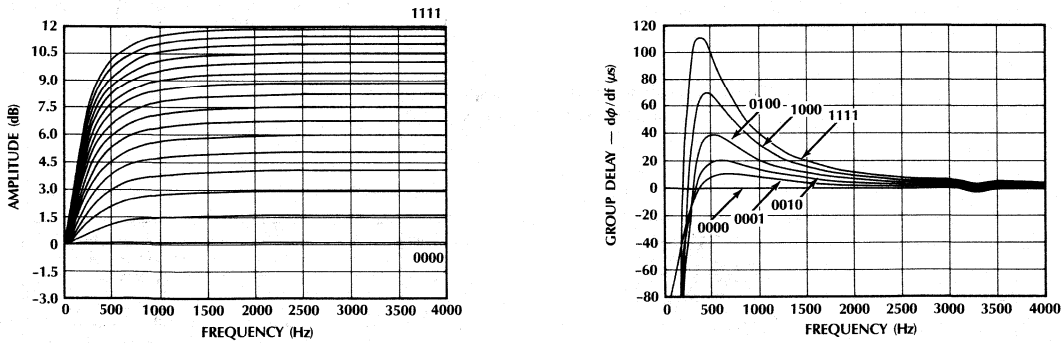


Figure 2. Typical Slope Filter Response — NL/L = 0

B3–B0, H3–H0 = 0000, S3–S0 = 0000 to 1111.

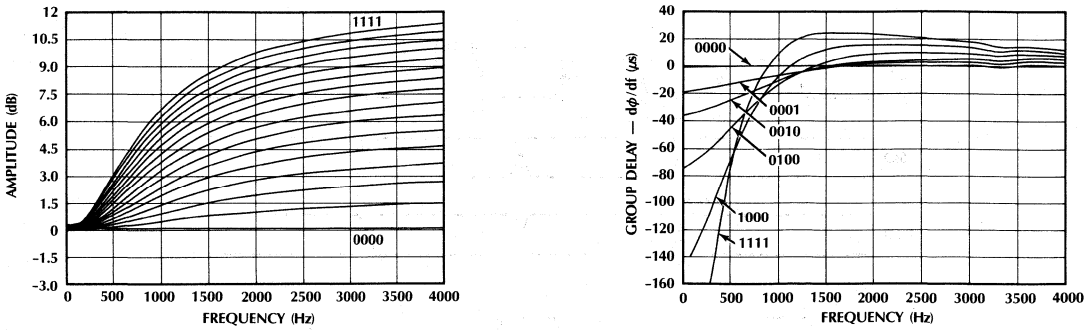


Figure 3. Typical Slope Filter Response — NL/L = 1

B3–B0, H3–H0 = 0000, S3–S0 = 0000 to 1111.

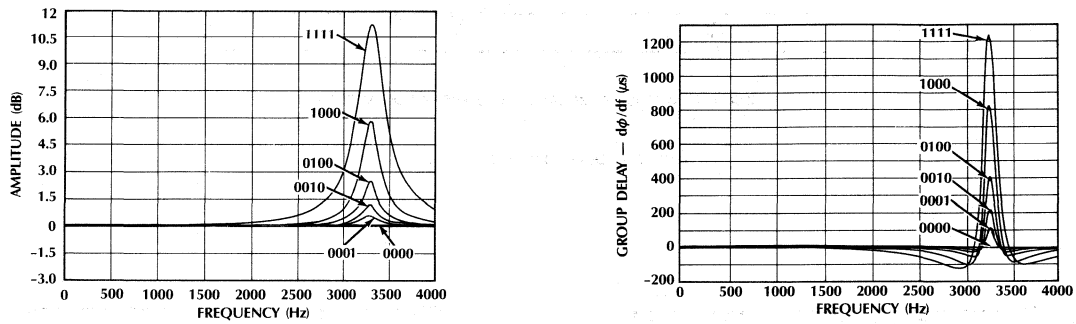


Figure 4. Typical Height Filter Response — NL/L = 0

B3–B0, S3–S0 = 0000; H3–H0 = 0000 to 1111.

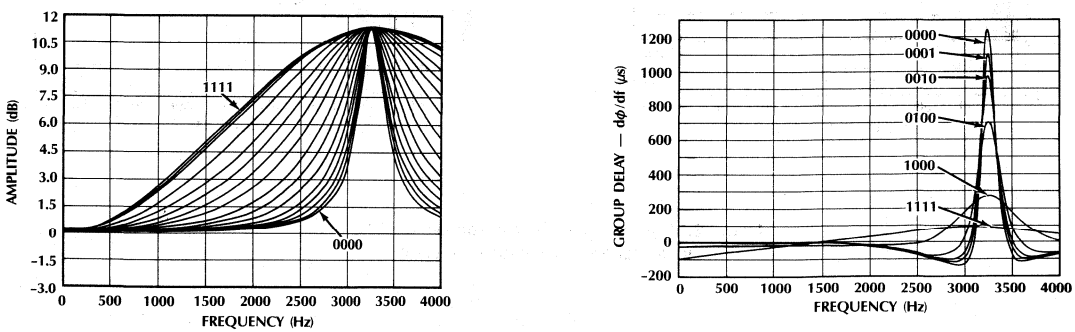


Figure 5. Typical Bandwidth Filter Response — NL/L = 0

H3–H0 = 1111; S3–S0 = 0000; B3–B0 = 0000 to 1111.

1.0 FUNCTIONAL DESCRIPTION

The ML2021 consists of a continuous anti-alias filter, three programmable switched capacitor equalization filters, an output smoothing filter, an output driver, and a digital section for the serial interface.

1.1 ANTI-ALIAS FILTER

The first section is a continuous anti-alias filter. This filter is needed to prevent aliasing of high frequency signals present on the input into the passband by the sampling action of the switched capacitor filters. This section is a continuous second order lowpass filter with a typical 3dB frequency at 20kHz and 30dB of rejection at 124kHz.

1.2 EQUALIZATION FILTERS

The programmable filters implement a family of frequency response curves intended to compensate for the response of telephone lines.

This filter is composed of three distinct sections: slope, height, and bandwidth.

1.2.1 RESPONSE OF SLOPE, HEIGHT, AND BANDWIDTH

The family of response curves generated by the slope section are shown in Figures 2 and 3. There are 4 slope select bits, S3-S0. These bits alter the slope of the highpass response under 1000Hz, and as a result, the absolute gain above 1000Hz will be unique for each setting. Table 1 gives typical 1kHz gain values for all slope settings.

Table 1. Typ. 1kHz Gain for Slope Settings

Slope Setting	Rel 1kHz Gain (dB)	
	NL/L=1	NL/L=0
0	0.0	Rel
1	0.4	1.4
2	0.9	2.6
3	1.4	3.7
4	1.8	4.7
5	2.3	5.5
6	2.8	6.3
7	3.4	7.2
8	3.7	7.8
9	4.2	8.4
10	4.6	9.0
11	5.0	9.5
12	5.4	10.0
13	5.8	10.5
14	6.2	11.0
15	6.6	11.4

HT, BW Bits=0

There is an additional bit, NL/L, that also affects the highpass response of the slope filter. The slope response curves in Figure 2 are with NL/L=0. These same response curves are shown in Figure 3 with NL/L=1. Notice that the NL/L bit adds more droop in the highpass response below 2500Hz.

The family of response curves generated by the height section are shown in Figure 4. There are 4 height select bits, H3-H0. This section creates a peak in the response at 3250Hz and this filter controls the amount of peaking. Table 2 gives typical 1kHz gain values for all height and bandwidth settings.

Table 2. Typ. 1kHz Gain for HT and BW Settings

	Relative 1kHz Gain (dB)															
	HT Setting															
BW Setting	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	Rel	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
3	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0.1
5	0	0	0	0	0	0	0	0	0	0	0	0	0.1	0.1	0.1	0.1
6	0	0	0	0	0	0	0	0	0	0	0.1	0.1	0.1	0.1	0.1	0.1
7	0	0	0	0	0	0	0	0	0.1	0.1	0.1	0.1	0.1	0.2	0.2	0.2
8	0	0	0	0	0	0	0.1	0.1	0.1	0.1	0.1	0.2	0.2	0.3	0.3	0.4
9	0	0	0	0	0	0.1	0.1	0.1	0.1	0.2	0.2	0.3	0.3	0.4	0.5	0.6
10	0	0	0	0	0.1	0.1	0.1	0.1	0.2	0.3	0.3	0.4	0.5	0.6	0.7	0.8
11	0	0	0	0.1	0.1	0.1	0.2	0.2	0.3	0.4	0.4	0.5	0.7	0.8	0.9	1.1
12	0	0	0.1	0.1	0.1	0.2	0.2	0.3	0.4	0.5	0.7	0.8	1.0	1.1	1.4	1.6
13	0	0	0.1	0.1	0.2	0.3	0.4	0.5	0.6	0.8	0.9	1.1	1.4	1.6	1.9	2.3
14	0	0	0.1	0.1	0.2	0.3	0.4	0.5	0.7	0.8	1.0	1.2	1.5	1.7	2.0	2.4
15	0	0	0.1	0.1	0.2	0.3	0.4	0.5	0.7	0.9	1.1	1.3	1.6	1.8	2.1	2.5

Slope Bits=0

The family of response curves generated by the bandwidth section is shown in Figure 5 There are 4 bandwidth select bits, B3-B0. This section causes the response of the 3250Hz peak to be widened, and as a result, this filter controls the bandwidth of the 3250Hz peaked region.

1.2.2 TRANSFER FUNCTION

The transfer function for the ML2021 is shown below. This transfer function is valid for magnitude response only. The actual magnitude response from an individual device may deviate from the computed response from the transfer function by typically 0–0.2dB.

$$H(s) = \frac{c(s+b)}{b(s+c)} \times \frac{\left[s^2 + h(\omega_o/Q)s + \omega_o^2\right]}{\left[s^2 + (\omega_o/Q)s + \omega_o^2\right]} \times \frac{\left[\sin(\pi f/fc)\right]}{(\pi f/fc)}$$

$s = j \times 256000 \times \tan(\pi f/128000)$

$\omega_o = 20463.77$

$fc = 128000$

b,c : See Table 3. (slope)

Q : See Table 4. (bandwidth)

h : See Table 5. (height)

Table 3. Slope Response Factors (b, c)

S3–0	b NL/L = 0	b NL/L = 1
0000	2.371759E+03	1.116280E+04
0001	1.985920E+03	9.345141E+03
0010	1.701779E+03	8.007156E+03
0011	1.493571E+03	7.026999E+03
0100	1.326721E+03	6.241681E+03
0101	1.196668E+03	5.629636E+03
0110	1.087277E+03	5.114881E+03
0111	9.983588E+02	4.696487E+03
1000	9.179889E+02	4.318339E+03
1001	8.537864E+02	4.016273E+03
1010	7.966049E+02	3.747249E+03
1011	7.478074E+02	3.517676E+03
1100	7.035099E+02	3.309279E+03
1101	6.651771E+02	3.128945E+03
1110	6.299477E+02	2.963214E+03
1111	5.990361E+02	2.817797E+03

S3–0	c NL/L = 0	c NL/L = 1
XXXX	2.371759E+03	1.116280E+04

Table 4. Slope Response Factors (b, c)

B3–0	Q
0000	17.444906
0001	15.386148
0010	13.652451
0011	11.593677
0100	9.859960
0101	8.017864
0110	6.392453
0111	5.092080
1000	3.900003
1001	3.141338
1010	2.599369
1011	2.165724
1100	1.731965
1101	1.406509
1110	1.352248
1111	1.297981

Table 5. Height Response Factors (h)

Code	h
0000	1.000000
0001	1.071519
0010	1.148154
0011	1.230269
0100	1.318257
0101	1.445438
0110	1.603245
0111	1.757924
1000	1.949845
1001	2.137962
1010	2.317395
1011	2.540973
1100	2.786121
1101	3.019951
1110	3.311311
1111	3.672823

1.2.3 GROUP DELAY

The difference between the ML2020 and ML2021 is the elimination of a 60Hz highpass filter in order to eliminate positive group delay at low frequency.

The group delay through the ML2021 can be minimized such that less than 50μs of group delay can be achieved in both unloaded and cable loaded conditions relative to 1804Hz in the frequency range of 504 to 3004Hz. Minimum group delays are dependent upon using the proper setting for slope, height, and bandwidth for a give equalization requirement.

1.3 SMOOTHING FILTER

The equalizer filters are followed by a continuous second order smoothing filter that removes the high frequency sample information generated by the action of the switched capacitor filters. This filter provides a continuous analog signal at the output, V_{OUT} .

1.4 OUTPUT BUFFER

The final stage in the ML2020 is the output buffer. This amplifier has internal gain of 1 and is capable of driving 600Ω, 100pF loads. Thus, it is suitable for driving telephone hybrids directly without any external amplifier.

1.5 BYPASS MODE

The filter sections can be bypassed by setting the bypass data bit, $\overline{BP}$, to 0. Since the switched capacitor filters are bypassed in this mode, frequency response effects of the switched capacitor filters are eliminated. Thus, this mode offers very flat response and low noise over the 300–4000Hz frequency range.

1.6 FILTER CLOCK

The master clock, CLK, is used to generate the internal clocks for the switched capacitor filters. The frequency of CLK can be either 1.544MHz or 1.536MHz. However, the internal clock frequency must be kept at 1.536MHz to guarantee accurate frequency response. The CLKSEL pin enables a bit swallower circuit to keep the internal clock frequency set to 1.536MHz. When 1.544MHz clock is used, CLKSEL should be set to logic level 0, and one bit out of every 193 bits is removed (swallowed) to reduce the internal frequency to 1.536MHz. When 1.536MHz clock is used, CLKSEL should be set to logic level 1, and the internal clock rate is the same as the external clock rate.

1.7 SERIAL INTERFACE

The architecture of the digital section is shown in the preceding block diagram.

A timing diagram for the serial interface is shown in Figure 6. The serial input data, SID, is loaded into a shift register on rising edges of the shift clock, SCK. The data word is parallel loaded into a latch when the input latch signal, LATI, is high. The LATI pulse must occur when SCK is low. A new data word can be loaded into the shift register without disturbing the existing data word in the latch.

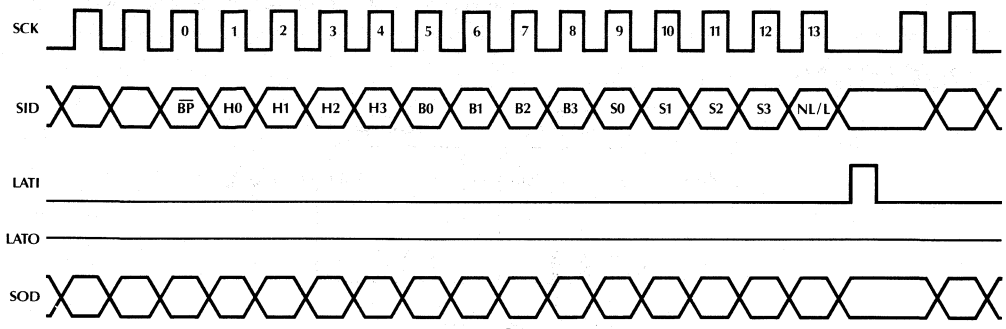
The parallel outputs of the latch control the filter response curves. The order of the data word bits in the latch is shown in Figure 7.

Note that bit 0 is the first bit of the data word clocked into the shift register.

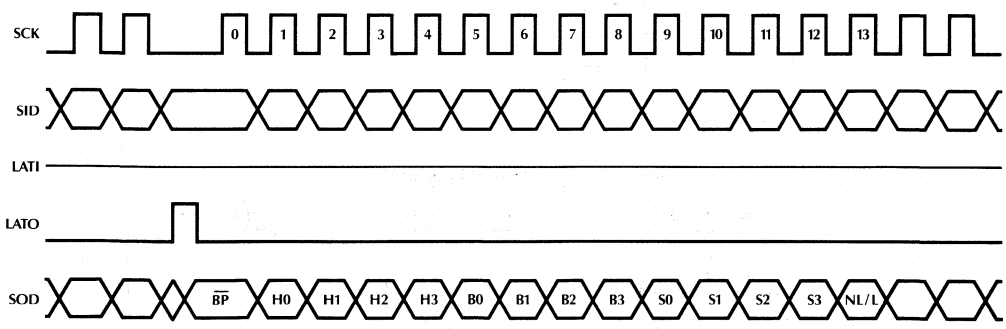
The device has the capability to read out the data word stored in the latch. This is done by parallel loading the data from the latch back into the shift register when the latch signal, LATO, is high. The LATO pulse must occur when SCK is low. Then, the data word can be shifted out of the register serially to the output, SOD, on falling edges of the shift clock, SCK.

The loading and reading of the data word can be done continuously or in bursts. Since the shift register and latch circuitry inside the device is static, there are no minimum frequency requirements on the clocks or data pulses. However, there is some coupling of the digital signals into the analog section. If this coupling is undesirable, the data can be clocked in bursts during non critical intervals, or the data rate can be done at a frequency outside the analog frequency range.

The clocks used to shift and latch data (SCK, LATI, LATO) are not related internally to the master clock and can occur asynchronous to CLK.



a) LOAD



b) READ

Figure 6. Serial Timing

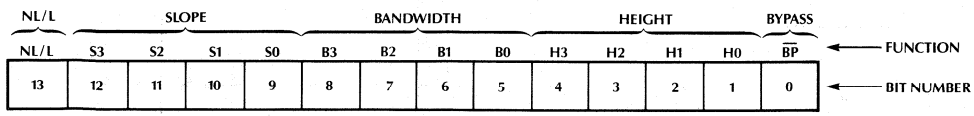


Figure 7. 14-Bit Latch

1.8 POWERDOWN MODE

A powerdown mode can be selected with pin P_{DN}. When $P_{DN} = 1$, the device is powered down. In this state, the power consumption is reduced by removing power from the analog section and forcing the analog output, V_{OUT}, to a high impedance state. While the device is in power down mode, the digital section is still functional and the current data word remains stored in the latch. The master clock, CLK, can be left active or removed during powerdown mode. When $P_{DN} = 0$, the device is in normal operation.

1.9 POWER SUPPLIES

The digital section inside the device is powered between V_{CC} and GND, or 5 volts. The analog section is powered between V_{CC} and V_{SS}, or ±5 volts. The analog section uses AGND as the reference point.

GND and AGND are totally isolated inside the device to minimize coupling from the digital section into the analog section. Typically this is less than 100μV. However, AGND and GND should be tied together physically near the device and close to the common power supply ground connection.

The power supply rejection of V_{CC} and V_{SS} to the analog output is greater than −60dB at 1kHz, typically. If decoupling of the power supplies is still necessary in a system, V_{CC} and V_{SS} should be decoupled with respect to AGND.

2.0 APPLICATIONS

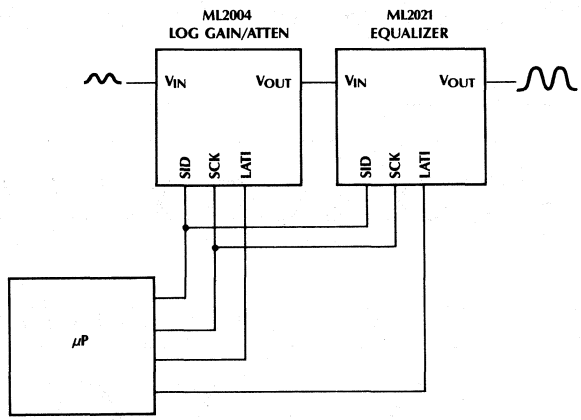


Figure 8. Typical Serial Interface

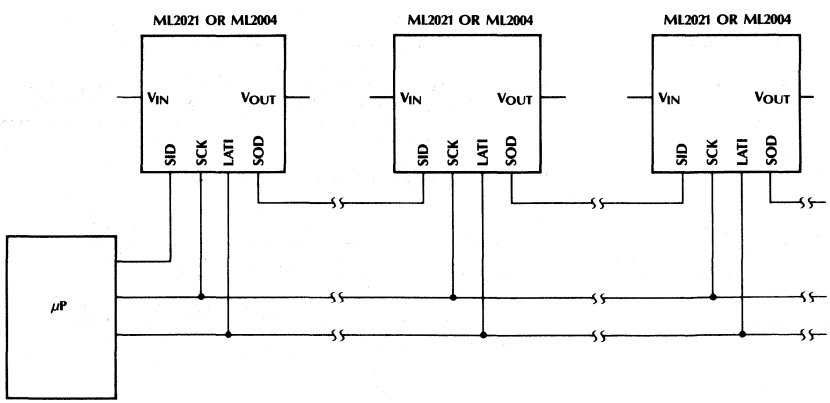


Figure 9. Controlling Multiple ML2021 and ML2004 With Only 3 Digital Lines Using One Long Data Word

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ML2021CP	0°C to +70°C	MOLDED DIP
ML2021CS	0°C to +70°	MOLDED SOIC
ML2021IJ	-40°C to +85°C	HERMETIC DIP

ML2031, ML2032

Tone Detector

GENERAL DESCRIPTION

The ML2031 and ML2032 are monolithic tone detectors intended for telecommunication applications utilizing 4-wire loopback capability. The device meets or exceeds the 4-wire Maintenance Terminating Unit (MTU) requirements outlined in BELL PUB 43004.

These devices incorporate a 2713 Hz tone detector, clock oscillator, and uncommitted op amp in an 8-pin DIP. No external components are required.

The ML2031 or ML2032 can be used to detect frequencies of 1004 Hz or 2600 Hz, as the tone detector frequency template from 1000 Hz to 4000 Hz is proportional to the frequency of the external clock.

The ML2031 has two clock outputs. $CLK_{OUT}1$ is one half the frequency of CLK_{IN}, while $CLK_{OUT}2$ is one eighth of the frequency of CLK_{IN}. The ML2032 has an uncommitted op amp instead of the clock outputs.

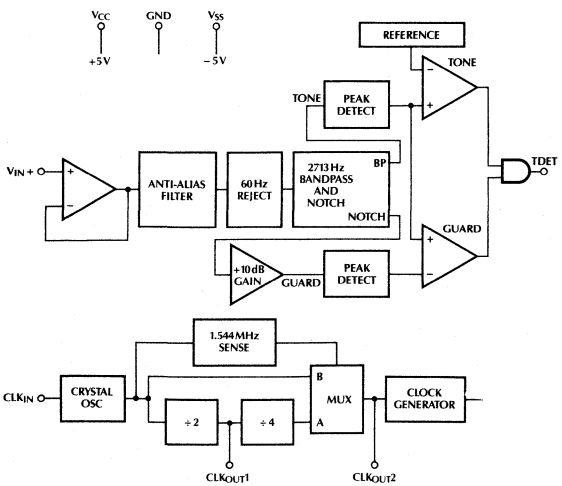
The ML2031 and ML2032 are implemented in a double polysilicon CMOS technology.

FEATURES

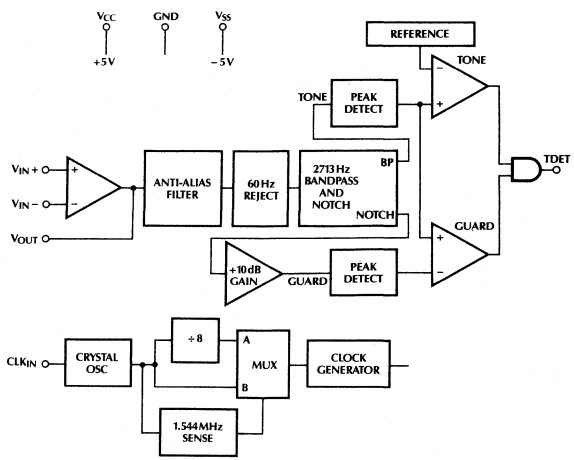
- Meets or exceeds BELL PUB 43004 requirements
- Extended dynamic range detect −34 dBm to +6 dBm
  no detect ⩽ −40 dBm
- Frequency template ($f_{CLK\ IN}$ = 12MHz)
  detect 2713 ± 10Hz
  no detect 2713 ± 36Hz
- General purpose tone detect range of 1000Hz to 4000Hz
- Signal-to-guard ratio 8 dB to 13 dB
- No external components required
- Continuous anti-alias filter
- 60 Hz reject filter
- ±5 V supplies
- Clock input 12.352 MHz, 1.544 MHz, or a 12.352 MHz crystal
- ML2031 has clock outputs of 1.544 MHz and 6.176 MHz
- Tone detection of 1000 Hz to 4000 Hz proportional to external clock
- ML2032 has uncommitted op amp
- 8-pin dual-in-line package

BLOCK DIAGRAMS

ML2031

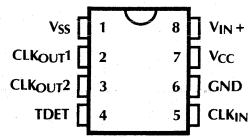


ML2032



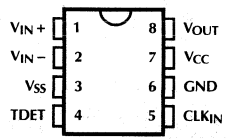
PIN CONNECTIONS

ML2031



TOP VIEW

ML2032



TOP VIEW

PIN DESCRIPTIONS

ML2031

PIN NO.	NAME	FUNCTION
1	V_{SS}	Negative supply. −5V ± 10%
2	$CLK_{OUT}1$	Clock output. Digital output from oscillator divided by 2.
3	$CLK_{OUT}2$	Clock output. Digital output from oscillator divided by 8.
4	TDET	Tone detect output. Digital output which indicates when valid 2713 Hz tone is present on analog input.
5	CLK_{IN}	Clock input. Internal clock can be generated by tying a 12.352 MHz crystal between this pin and GND, or by applying a 12.352 MHz or 1.544 MHz clock to this pin.
6	GND	Ground. Analog and digital inputs and outputs are referenced to this point.
7	V_{CC}	Positive supply. +5V ± 10%
8	$V_{IN}+$	Analog input.

ML2032

PIN NO.	NAME	FUNCTION
1	$V_{IN}+$	Positive Analog input. Positive input to the uncommitted op amp.
2	$V_{IN}-$	Negative Analog input. Negative input to the uncommitted op amp.
3	V_{SS}	Negative supply. −5V ± 10%
4	TDET	Tone detect output. Digital output which indicates when valid 2713 Hz tone is present on analog input.
5	CLK_{IN}	Clock input. Internal clock can be generated by tying a 12.352 MHz crystal between this pin and GND, or by applying a 12.352 MHz or 1.544 MHz clock to this pin.
6	GND	Ground. Analog and digital inputs and outputs are referenced to this point.
7	V_{CC}	Positive supply. +5V ± 10%
8	V_{OUT}	Analog output. Output of the uncommitted op amp.

ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage
- V_{CC} ..... +6.5V
- V_{SS} ..... −6.5V
- Analog Input and Output ..... V_{SS} −0.3V to V_{CC} +0.3V
- Digital Input and Outputs ..... −0.3V to V_{CC} +0.3V
- Input Current Per Pin ..... ±25mA
- Power Dissipation 750mW
- Storage Temperature Range ..... −65°C to +150°C
- Lead Temperature (Soldering 10 sec.) ..... 300°C

OPERATING CONDITIONS

Temperature Range (Note 2)
- ML2031CP, ML2032CP ..... 0°C to +70°C
- ML2031IJ, ML2032IJ ..... −40°C to +85°C

Supply Voltage
- V_{CC} ..... 4V to 6V
- V_{SS} ..... −4V to −6V

ELECTRICAL CHARACTERISTICS

Unless otherwise specified $T_A = T_{MIN}$ to T_{MAX}, $V_{CC} = 5V \pm 10\%$, $V_{SS} = -5V \pm 10\%$, $CLK_{IN} = 12.352MHz \pm 1200Hz$, or $CLK_{IN} = 1.544MHz \pm 150Hz$, $C_L = 100pF$, dBm measurements use 600Ω as reference load, uncommitted op amp in unity gain configuration.

SYMBOL	PARAMETER	NOTES	CONDITIONS	MIN	TYP NOTE 3	MAX	UNITS
TONE DETECT							
f_{TD}	Tone Detection Frequency	4	V_{IN} = +6dBm to −34dBm	2703		2723	Hz
f_{TR}	Tone Rejection Frequency	4		2679		2747	Hz
A_{TD}	Tone Detection Amplitude	4	V_{IN} = 2703 Hz to 2723 Hz	−34		+6	dBm
A_{TR}	Tone Rejection Amplitude	4		−40			dBm
SGM	Signal to Guard Margin	4	800 Hz 1400 Hz 2000 Hz 2450 Hz Signal = −13 dBm, 2713 Hz. See BELL PUB 43004 sec. 2.4 for test method	8 8 8 8		13 13 13 13	dB dB dB dB
SFI	SF Tone Immunity	5	V_{IN} + = 2600 Hz No tone detect			+6	dBm
t_{TD}	Tone Detect Delay	4	V_{IN}+ = −8dBm, 2713 Hz Figure 1	0	10	30	ms
t_{TR}	Tone Removal Delay	4	V_{IN}+ = −8dBm, 2713 Hz Figure 1	0	4	30	ms
OP AMP							
V_{INR}	Input Voltage Range	5		±3			V
V_{OSW}	Output Voltage Swing	4	ML2032 Only	±3			V
V_{OS}	Input Offset Voltage	4	ML2032 Only			±20	mV
Z_{IN}	Input Impedance	4		1			MΩ
A_{VOL}	DC Open Loop Gain	4		1k	5k		V/V
f_{UG}	Unity Gain Frequency	5		0.5	1		MHz
I_{CN}	Noise- Input Referred	5	C msg weighted 1kHz		−9	−3 375	dBrnc nv/√Hz

ELECTRICAL CHARACTERISTICS (Continued)

Unless otherwise specified $T_A = T_{MIN}$ to T_{MAX}, $V_{CC} = 5V \pm 10\%$, $V_{SS} = -5V \pm 10\%$, $CLK_{IN} = 12.352MHz \pm 1200Hz$, or $CLK_{IN} = 1.544MHz \pm 150Hz$, $C_L = 100pF$, dBm measurements use 600Ω as reference load, uncommitted op amp in unity gain configuration.

SYMBOL	PARAMETER	NOTES	CONDITIONS	MIN	TYP NOTE 3	MAX	UNITS
DIGITAL AND DC							
V_{IL}	Input Low Voltage, CLK_{IN}	4				1.5	V
V_{IH}	Input High Voltage, CLK_{IN}	4		3.5			V
I_{IN}	Input Current, CLK_{IN}	4	CLK_{IN} = 1.5V to 3.5V		10	60	μA
			CLK_{IN} = 0 to 1.5V; 3.5V to V_{CC}		150	500	μA
C_{IN}	Input Capacitance, CLK_{IN}	5			11		pF
V_{OL}	Output Low Voltage	4	I_{OL} = -2mA			0.4	V
V_{OH}	Output High Voltage	4	I_{OH} = 2mA	4.0			V
I_{CC}	V_{CC} Supply Current	4	No output load			7.5	mA
I_{SS}	V_{SS} Supply Current	4	No output load			-4.5	mA
CLOCK OUTPUT							
$f_{CLK}1$	$CLK_{OUT}1$ Output Frequency	4	Figure 2	½		½	$f_{CLK}1$
$f_{CLK}2$	$CLK_{OUT}2$ Output Frequency	4	Figure 2	⅛		⅛	$f_{CLK}1$
t_{1R}	$CLK_{OUT}1$ Output Rise Time	4	Figure 2, C_L = 50pF	0		20	ns
t_{1F}	$CLK_{OUT}1$ Output Fall Time	4	Figure 2, C_L = 50pF	0		20	ns
t_{2R}	$CLK_{OUT}2$ Output Rise Time	4	Figure 2, C_L = 50pF	0		20	ns
t_{2F}	$CLK_{OUT}2$ Output Fall Time	4	Figure 2, C_L = 50pF	0		20	ns

Note 1: Absolute maximum ratings are limits beyond which the life of the integrated circuit may be impaired. All voltages unless otherwise specified are measured with respect to ground.

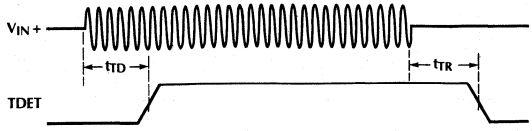
Note 2: 0°C to +70°C and -40°C to +85°C operating temperature range devices are 100% tested with temperature limits guaranteed by 100% testing, sampling, or by correlation with worst-case test conditions.

Note 3: Typicals are parametric norm at 25°C.

Note 4: Parameter guaranteed and 100% production tested.

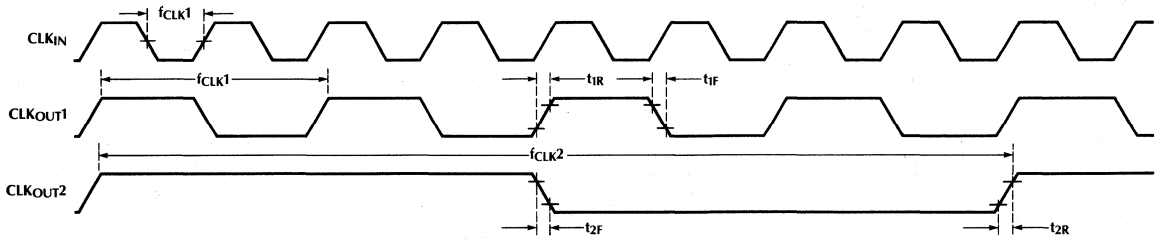
Note 5: Parameter guaranteed. Parameters not 100% tested are not in outgoing quality level calculation.

TIMING DIAGRAMS



t_{TD} MEASURED FROM V_{IN} + ZERO CROSSING TO 1.4 V MIDPOINT ON TDET
t_{TR} MEASURED FROM 1.4 V MIDPOINT ON TDET TO ZERO CROSSING ON V_{IN} +

Figure 1. Tone Detect Timing



t_{1F}, t_{1R}, t_{2F}, t_{2R} MEASURED BETWEEN 0.8 and 2.0 VOLT TRANSITION POINTS
ALL OTHER PARAMETERS REFERRED TO 1.4 V MIDPOINT

Figure 2. Digital Clock Output Timing

TYPICAL PERFORMANCE CURVE

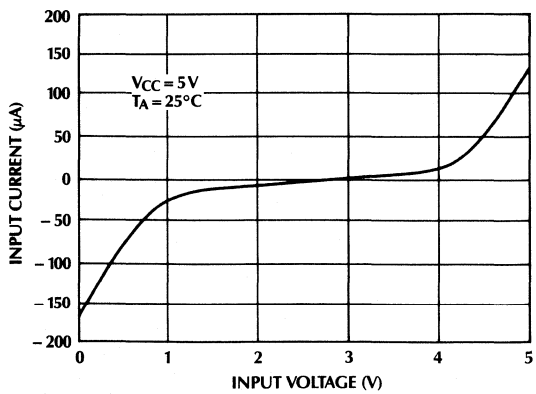


Figure 3. CLK_{IN} Input Current vs. Input Voltage

1.0 FUNCTIONAL DESCRIPTION

The ML2031 has a divide by 2 and divide by 8 clock output to drive external devices. The ML2032 has an uncommitted op amp. Refer to the block diagram.

1.1 Uncommitted Op Amp

The ML2032 features an uncommitted op amp. The ML2031 has the op amp connected in the unity gain configuration ($V_{IN}-$ internally tied to V_{OUT}).

The uncommitted op amp is a general purpose amplifier that can be used to interface the device with the analog telephone line. It has a high impedance input, a 0.5 MHz unity gain bandwidth, will drive a 1k, 100 pF load, and the input and output can swing within 1.5 V of the supplies.

1.2 Anti-Alias Filter

The anti-alias filter is a continuous second order low pass designed to prevent high frequency signals at the input from being aliased into the passband by the sampling action of the switched capacitor filters. The typical 3 dB corner frequency is 25 kHz and the typical rejection at 124 kHz is −30 dB.

1.3 60 Hz Reject Filter

The 60 Hz reject filter is a switched capacitor second order high pass designed to reject 60 Hz line interference on the analog input. The typical 3 dB corner frequency is 300 Hz and the typical rejection at 60 Hz is −24 dB.

1.4 Tone Detector

The tone detector is a monolithic block designed to indicate when a valid 2713 Hz tone is present on the analog input. A tone is valid if the following criteria are met:

1. 2713 Hz tone satisfies amplitude vs. frequency tone detector template shown in *Figure 4*.
2. The non-2713 Hz out of band energy present on the input is sufficiently small enough compared to the 2713 Hz tone (signal to guard margin).

The tone detector consists of 2713 Hz bandpass and notch filters, tone and guard peak detectors, tone and guard comparators, reference, and digital output buffer.

The analog signal first goes through the 2713 Hz bandpass and notch switched capacitor filters. The bandpass filter outputs any 2713 Hz signal (tone), and the notch filter outputs any non-2713 Hz signals (guard) in the range of 300–4500 Hz, respectively.

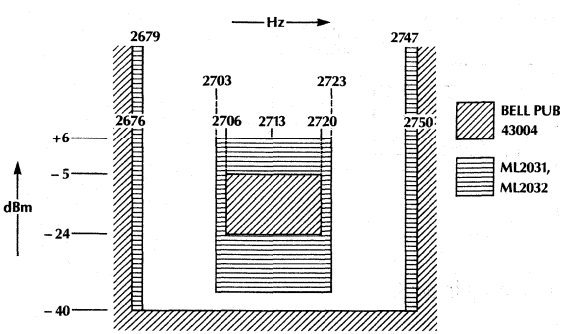


Figure 4. Tone Detector Template

The tone and guard signals then go to peak detectors which output a DC voltage proportional to the 2713 Hz and non-2713 Hz energy present on the analog input.

The tone comparator compares the tone energy to a fixed reference value to determine if it meets the amplitude requirements for tone detection shown in *Figure 4*.

The guard comparator compares the tone energy to the guard energy to determine if the signal to guard margin is met.

If both comparators indicate that a 2713 Hz tone and no out of band energy exists, the TDET output goes high indicating valid tone detection. If the signal comparator indicates insufficient signal energy or the guard comparator indicates too much out of band energy, then the TDET output stays low indicating invalid tone output.

1.5 Crystal Oscillator/Clock Generator

The crystal oscillator/clock generator generates the necessary internal clocks from either an external clock or an external crystal.

If an external clock input is used to drive CLK_{IN}, the input frequency can either be 12.352 MHz or 1.544 MHz in order to meet the frequency template. The device has an internal frequency sense circuit that can sense the difference between 12.352 MHz and 1.544 MHz and makes the necessary changes in the clock generator to accomodate either frequency at the input.

If a crystal is used, a 12.352 MHz crystal must be connected between CLK_{IN} and GND. This unique 1-pin crystal oscillator does not generally require any external capacitors or other external components to meet the frequency template. The crystal should be physically placed as close as possible to the CLK_{IN} pin to minimize stray inductances and capacitances.

The crystal must have the following characteristics:

1. Parallel resonant type
2. Frequency: 12.352000 MHz
3. Tolerance: ±0.005% @ 25°C
4. Less than 0.005% variation over desired temperature range
5. Maximum equivalent series resistance of 15 Ω at a drive level of 1 μW to 200 μW
6. Maximum equivalent series resistance of 30 Ω at drive levels of 10 nW to 1 μW
7. Typical load capacitance: 18 pF
8. Maximum case capacitance: 5 pF

The frequency of oscillation will be a function of the crystal parameters and board capacitance. If the final oscillation frequency is different than the ideal 12.352 MHz, the template frequencies will change according to the formulas outlined in section 1.6. If the crystal meets the above recommended parameters and typical PC board capacitance from CLK_{IN} to GND is 2 pF, then the device will meet the template specifications. Crystals that meet these requirements are M-tron 3709-010 12.352 for 0°C to +70°C and 3709-020 12.352 for −40°C to +85°C operation.

3

1.0 FUNCTIONAL DESCRIPTION (Continued)

The ML2031 has two clock outputs that can be used to drive other external devices. The $CLK_{OUT}1$ output is a buffered output from the oscillator divided by 2. The $CLK_{OUT}2$ output is a buffered output from the oscillator divided by 8. If a 12.352 MHz clock or crystal is used, $CLK_{OUT}1 = 6.176$ MHz and $CLK_{OUT}2 = 1.544$ MHz.

1.6 Detecting Tones from 1000 Hz to 4000 Hz

The tone detector frequency template shown in *Figure 5* is proportional to the frequency of CLK_{IN}. Thus, the device can be set to a center frequency (other than 2713 Hz) by adjusting CLK_{IN} frequency.

The external clock frequency, $fCLK_{IN}$, needed to produce a given center frequency, can be calculated by:

$$fCLK_{IN} = f_C \times 4552.893$$

once $fCLK_{IN}$ has been determined, the other template frequency points shown in *Figure 5* can be calculated by:

$$f_{DL} = fCLK_{IN} \times 2.18831 \times 10^{-4}$$

$$f_{DU} = fCLK_{IN} \times 2.20450 \times 10^{-4}$$

$$f_{RL} = fCLK_{IN} \times 2.16888 \times 10^{-4}$$

$$f_{RU} = fCLK_{IN} \times 2.22393 \times 10^{-4}$$

The above formulas are valid for center frequencies with the range of 1000 Hz to 4000 Hz. The internal divide by 8 circuitry may be bypassed by applying a clock that is one eighth of the above calculated values.

When the required CLK_{IN} frequency calculated above is less than 6 MHz, the internal frequency sense circuit may become enabled causing the detection of an erroneous center frequency. In this case, the divide by 8 function cannot be used and only the lower clock frequency may be used. For example, for a 1004 Hz tone detector, the clock frequency applied must be 571 kHz.

1.7 Power Supplies

The analog circuits in the device run from +5 to −5 (V_{CC} to V_{SS}) and are referenced to GND.

The digital circuits in the device run from +5 to 0 (V_{CC} to GND).

It is recommended that the power supplies to the device be bypassed by placing decoupling capacitors from V_{CC} to GND and V_{SS} to GND as physically close to the device as possible.

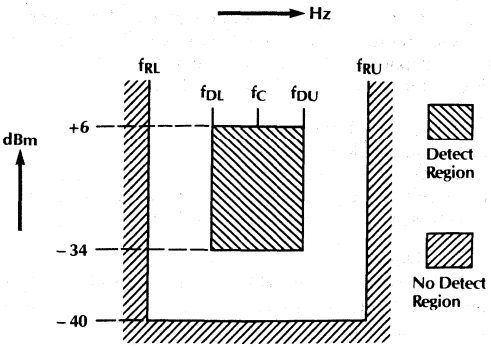


Figure 5. Tone Detector Template

2.0 APPLICATIONS

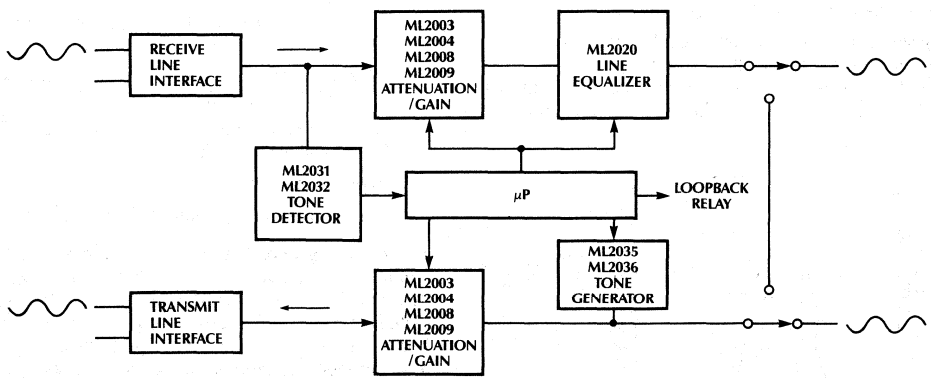


Figure 6. 4-Wire Termination Equipment

ORDERING INFORMATION

PART NUMBER	PACKAGE	TEMPERATURE RANGE
ML2031IJ	Hermetic DIP	−40°C to +85°C
ML2031CP	Molded DIP	0°C to +70°C
ML2032IJ	Hermetic DIP	−40°C to +85°C
ML2032CP	Molded DIP	0°C to +70°C

Micro Linear

ML2035, ML2036

Programmable Sinewave Generator

GENERAL DESCRIPTION

The frequency of these monolithic sinewave generators is programmable for the ML2035 from DC to 25kHz and for the ML2036 from DC to 50kHz. No external components are required.

The frequency of the sinewave output is derived from either an external crystal or clock input, thus providing a stable and accurate frequency reference. The frequency is programmed by a 16-bit serial data word.

The ML2035 is packaged in an 8-pin DIP and has a V_{OUT} amplitude of $\pm V_{CC}/2$.

The ML2036 provides for a V_{OUT} amplitude of either $\pm V_{REF}$ or $\pm V_{REF}/2$. Also included with the ML2036 is an inhibit input which allows the sinewave output to be held at zero volts after completing the last half cycle of the sinewave preventing steps in voltage. Two pins of the ML2036 are clock outputs designed to drive other devices with one half or one eighth of the clock input frequency.

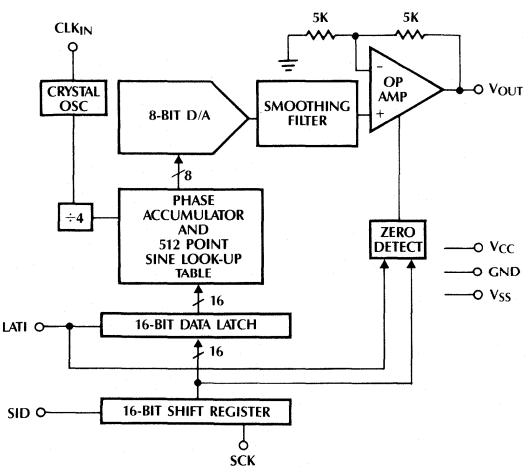
The ML2035 and ML2036 are intended for telecommunications and modem applications that need low cost and accurate generation of precise test tones, call progress tones, and signaling tones.

FEATURES

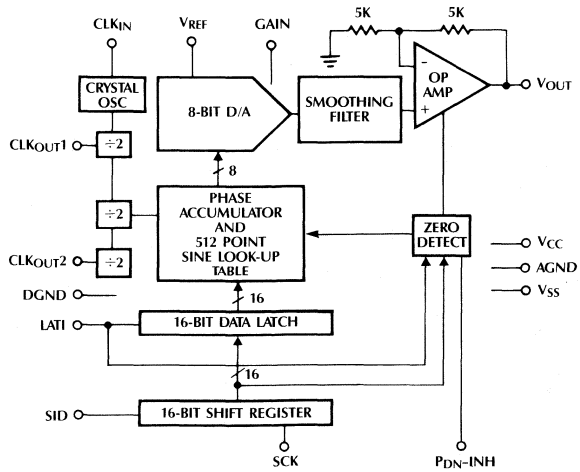
- Programmable frequency DC to 50kHz
- Frequency resolution with f_{CLKIN} = 12MHz (±.75 Hz) 1.5Hz
- Absolute gain error ±.1dB max
- Harmonic distortion –45dB max
- Output voltage amplitude of $\pm V_{REF}$ or $\pm V_{REF}/2$
- On chip crystal oscillator 3 to 12MHz
- ML2036 has clock outputs of 1/2 or 1/8 of the input clock frequency
- No external components required
- µP compatible serial interface
- Double buffered data latch
- Synchronous or asynchronous data loading capability
- Power dissipation 50mW max from ±5V supplies
- Compatible with ML2031 and ML2032 tone detector, and ML2004 logarithmic gain/attenuator
- TTL/CMOS compatible inputs
- ML2035 package 8-pin DIP; ML2036 14-pin DIP or 16-pin SOIC
- 0°C to +70°C or –40°C to +85°C operating temperature range

BLOCK DIAGRAMS

ML2035

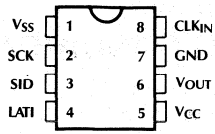


ML2036



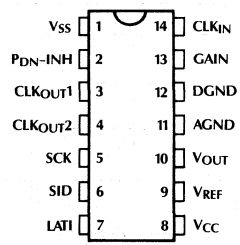
PIN CONNECTIONS

ML2035
8-Pin DIP



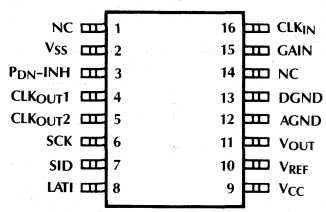
TOP VIEW

ML2036
14-Pin DIP



TOP VIEW

ML2036
16-Pin SOIC



TOP VIEW

PIN DESCRIPTIONS

ML2035

PIN NO.	NAME	FUNCTION
1	V_{SS}	Negative supply. –5V ± 10%.
2	SCK	Serial clock. Digital input which clocks in serial data on rising edges.
3	SID	Serial data. Serial input data which programs the frequency of V_{OUT}.
4	LATI	Serial latch. Digital input which latches serial data into the internal data latch on falling edges.
5	V_{CC}	Positive supply. +5V ± 10%.
6	V_{OUT}	Analog output. V_{OUT} swing is $\pm V_{CC}/2$.
7	GND	Ground. 0 volts. All inputs and outputs referenced to this point.
8	CLK_{IN}	Clock input. Internal clock can be generated by tying a 3 to 12MHz crystal from this pin to GND or applying a clock directly to the pin.

ML2036

PIN NO. DIP	PIN NO. SOIC	NAME	FUNCTION
1	2	V_{SS}	Negative supply. –5V ± 10%.
2	3	P_{DN}–INH	Three level input. Controls inhibit mode and power down mode. Current source pull up to V_{CC}.
3	4	CLK_{OUT1}	Clock output. Digital output from internal clock generator that can drive other devices. $f_{CLKOUT1} = f_{CLKIN/2}$.
4	5	CLK_{OUT2}	Clock output. Digital output from internal clock generator that can drive other devices. $f_{CLKOUT2} = f_{CLKIN/8}$.
5	6	SCK	Serial clock. Digital input which clocks in serial data on rising edges.
6	7	SID	Serial data. Serial input data which programs the frequency of V_{OUT}.
7	8	LATI	Serial latch. Digital input which latches serial data into the internal data latch on falling edges.
8	9	V_{CC}	Positive supply. +5V ± 10%.
9	10	V_{REF}	Reference input. The voltage on this pin determines the peak-peak swing on V_{OUT}. V_{REF} can be tied to V_{CC}.
10	11	V_{OUT}	Analog output.
11	12	AGND	Analog ground. 0 volts. Analog inputs and outputs referenced to this point.
12	13	DGND	Digital ground. 0 volts. Digital inputs and outputs referenced to this point.
13	15	GAIN	Sets V_{OUT} peak amplitude to V_{REF} or $V_{REF}/2$. Current source pull down to DGND.
14	16	CLK_{IN}	Clock input. Internal clock can be generated by tying a 3 to 12MHz crystal from this pin to DGND or applying a clock directly to the pin.

3

ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage
- V_{CC} ..... +6.5V
- V_{SS} ..... -6.5V
- Analog Input and Output ..... V_{SS} - 0.3V to V_{CC} + 0.3V
- AGND Voltage ..... V_{SS} to V_{CC}
- Digital Inputs and Outputs ..... -0.3V to V_{CC} + 0.3V
- Input Current per Pin ..... ±25mA
- Power Dissipation 750mW
- Storage Temperature Range ..... -65°C to +150°C

Lead Temperature (Soldering 10 sec)
- Dual-In-Line Package (Molded) ..... 260°C
- Dual-In-Line Package (Ceramic) ..... 300°C
- Molded Small Outline IC Package
  - Vapor Phase (60 sec) ..... 215°C
  - Infrared (15 sec) ..... 220°C

OPERATING CONDITIONS

Temperature Range (Note 2)
- ML2035CP, ML2036CP, ML2036CS ..... 0°C to +70°C
- ML2035IJ, ML2036IJ ..... -40°C to +85°C

ML2035 ELECTRICAL CHARACTERISTICS

Unless otherwise specified, $T_A = T_{MIN}$ to T_{MAX}, V_{CC} = 5V ± 10%, V_{SS} = -5V ± 10%, CLK_{IN} = 12.352MHz, V_{OUT} load C_L = 100pF and R_L = 1k, all digital timing measured at 1.4V midpoint, and input control signals from 10% to 90% of V_{CC} with $t_R = t_F$ = 20ns.

SYMBOL	PARAMETER	NOTES	CONDITIONS		MIN	TYP (Note 3)	MAX	UNITS
Sinewave Generator								
HD	Harmonic Distortion	4	2nd or 3rd Harmonic Relative to Fundamental	f_{OUT} = 20Hz to 10kHz			-45	dB
				f_{OUT} = 10kHz to 25kHz			-40	dB
SND	Signal to Noise + Distortion	4	200Hz ≤ f_{OUT} ≤ 3400Hz, noise measured 200Hz to 4kHz				-45	dB
			20Hz ≤ f_{OUT} ≤ 25kHz, noise measured 20Hz to 75kHz				-40	dB
ICN	Output Idle Channel Noise	4	Power Down Mode, Cmsg weighted			-20	0	dBrnc
			Power Down Mode, 1kHz			50		$nV/\sqrt{Hz}$
PSRR	Power Supply Rejection Ratio	5	200mV_{P-P}, 0-10kHz sine, measured on V_{OUT}	V_{CC}			-40	dB
				V_{SS}			-40	dB
V_{OS}	V_{OUT} Offset Voltage	4					±75	mV
V_{PK}	V_{OUT} Peak Voltage					±V_{CC}/2		V
V_{GN}	V_{OUT} Gain Error	4	Relative to V_{CC}	f_{OUT} = 20Hz to 10kHz			±.1	dB
				f_{OUT} = 10kHz to 25kHz			±.3	dB
Digital and DC								
V_{IL}, CLK	Input Low Voltage, CLK_{IN}	4					1.5	V
V_{IH}, CLK	Input High Voltage, CLK_{IN}	4			3.5			V
I_{IN}, CLK	Input Current, CLK_{IN}	4	CLK_{IN} = 1.5V to 3.5V			10	60	μA
			CLK_{IN} = 0 to 1.5V; 3.5V to V_{CC}				250	μA
C_{IN}, CLK	Input Capacitance, CLK_{IN}	5				12		pF
V_{IL}	Input Low Voltage	4					.8	V
V_{IH}	Input High Voltage	4			2.0			V
I_{IL}	Input Low Current	4	V_{IN} = 0V		-1			μA
I_{IH}	Input High Current	4	V_{IN} = V_{CC}				1	μA
C_{IN}	Digital Input Capacitance					5		pF
V_{OL}	Output Low Voltage	4	I_{OL} = -2mA				0.4	V
V_{OH}	Output High Voltage	4	I_{OH} = 2mA		4.0			V

ML2035 ELECTRICAL CHARACTERISTICS (Continued)

Unless otherwise specified, $T_A = T_{MIN}$ to T_{MAX}, $V_{CC} = 5V \pm 10\%$, $V_{SS} = -5V \pm 10\%$, $CLK_{IN} = 12.352MHz$, V_{OUT} load $C_L = 100pF$ and $R_L = 1k$, all digital timing measured at 1.4V midpoint, and input control signals from 10% to 90% of V_{CC} with $t_R = t_F = 20ns$.

SYMBOL	PARAMETER	NOTES	CONDITIONS	MIN	TYP (Note 3)	MAX	UNITS
Digital and DC (Continued)							
I_{CC}	V_{CC} Supply Current	4	No output load, $V_{CC} = 5.5V$			5.5	mA
I_{SS}	V_{SS} Supply Current	4	No output load, $V_{SS} = -5.5V$, $V_{CC} = 5.5V$			-3.5	mA
I_{CCI}	V_{CC} Supply Current, Power Down Mode	4	No Output Load, Power Down Mode			2.0	mA
I_{SSI}	V_{SS} Supply Current, Power Down Mode	4	No Output Load, Power Down Mode			-100	μA
Digital Timing							
t_{CKI}	CLK_{IN} On/Off Period	4	$t_R = t_F = 10ns$, 2.5V midpoint	30			ns
t_{SCK}	SCK On/Off Period	4		100			ns
t_{DS}	SID DATA Setup Time	4		50			ns
t_{DH}	SID DATA Hold Time	4		50			ns
t_{LPW}	LATI Pulse Width	4		50			ns
t_{LH}	LATI Hold Time	4		50			ns
t_{LS}	LATI Setup Time	5		50			ns

3

ML2036 ELECTRICAL CHARACTERISTICS

Unless otherwise specified, $T_A = T_{MIN}$ to T_{MAX}, V_{CC} = 5V ± 10%, V_{SS} = –5V ± 10%, AGND = DGND = 0V, V_{REF} = 2.5V to V_{CC}, and CLK_{IN} = 12.352MHz, V_{OUT} load C_L = 100pF and R_L = 1k, all digital timing measured at 1.4V midpoint, and input control signals from 10% to 90% of V_{CC} with $t_R = t_F$ = 20ns.

SYMBOL	PARAMETER	NOTES	CONDITIONS	MIN	TYP (Note 3)	MAX	UNITS
Sinewave Generator							
HD	Harmonic Distortion	4, 6	2nd or 3rd harmonic relative to fundamental; f_{OUT} = 20Hz to 10kHz			–45	dB
			2nd or 3rd harmonic relative to fundamental; f_{OUT} = 10kHz to 50kHz			–40	dB
SND	Signal to Noise + Distortion	4, 6	200Hz ≤ f_{OUT} ≤ 3400Hz, noise measured 200Hz to 4kHz			–45	dB
			20Hz ≤ f_{OUT} ≤ 50kHz, noise measured 20Hz to 150kHz			–40	dB
ICN	Output Idle Channel Noise	4	Power down mode, Cmsg weighted		–20	0	dBrnc
			Power down mode, 1kHz		50		$nV/\sqrt{Hz}$
			Inhibit mode, 1kHz		500		$nV/\sqrt{Hz}$
PSRR	Power Supply Rejection Ratio	5	200mV$_{P-P}$, 0 to 10kHz sine, measured on V_{OUT}; V_{CC}			–40	dB
			200mV$_{P-P}$, 0 to 10kHz sine, measured on V_{OUT}; V_{SS}			–40	dB
V_{OS}	V_{OUT} Offset Voltage	4, 7				±25 + (±10 × V_{OUTP-P})	mV
V_{PK}	V_{OUT} Peak Voltage	6	GAIN = V_{CC}		±V_{REF}		V
			GAIN = DGND		±V_{REF}/2		V
V_{SW}	V_{OUT} Swing	5	GAIN = V_{CC}	V_{SS}+1.5V		V_{CC}–1.5V	V
V_{GN}	V_{OUT} Gain Error	4, 6	f_{OUT} = 20Hz to 10kHz			±.1	dB
			f_{OUT} = 10kHz to 50kHz			±.3	dB
R_{REF}	Reference Input Resistance	4		2.5	12		MΩ
Digital and DC							
V_{IL}, CLK	Input Low Voltage, CLK_{IN}	4				1.5	V
V_{IH}, CLK	Input High Voltage, CLK_{IN}	4		3.5			V
I_{IN}, CLK	Input Current, CLK_{IN}	4	CLK_{IN} = 1.5V to 3.5V		10	60	µA
			CLK_{IN} = 0 to 1.5V; 3.5V to V_{CC}			250	µA
C_{IN}, CLK	Input Capacitance, CLK_{IN}	5			12		pF
V_{IL}	Input Low Voltage	4	LATI, SID, GAIN, SCK			.8	V
V_{IH}	Input High Voltage	4	LATI, SID, GAIN, SCL	2.0			V
I_{IL}	Input Low Current	4	V_{IN} = 0V, LATI, SID, GAIN, SCK	–1			µA
I_{IH}	Input High Current	4	V_{IN} = V_{CC}, LATI, SID, P_{DN}–INH, SCK			1	µA
I_{IL}, P_{DN}	Input Low Current	4	P_{DN}–INH, V_{IN} = 0V	–70	–20	–5	µA
I_{IH}, G	Input High Current	4	GAIN, V_{IN} = V_{CC}	5	20	70	µA
V_{I1}	Input Logic Low P_{DN}–INH	4		DGND–.5		.8	V
V_{I2}	Inhibit State Voltage P_{DN}–INH	4				V_{SS}+.5	V
V_{I3}	Input Logic High P_{DN}–INH	4		2.0			V
C_{IN}	Digital Input Capacitance				5		pF
V_{OL}	Output Low Voltage	4	I_{OL} = –2mA			0.4	V
V_{OH}	Output High Voltage	4	I_{OH} = 2mA	4.0			V

ML2036 ELECTRICAL CHARACTERISTICS (Continued)

Unless otherwise specified, $T_A = T_{MIN}$ to T_{MAX}, V_{CC} = 5V ± 10%, V_{SS} = –5V ± 10%, AGND = DGND = 0V, V_{REF} = 2.5V to V_{CC}, and CLK_{IN} = 12.352MHz, V_{OUT} load C_L = 100pF and R_L = 1k, all digital timing measured at 1.4V midpoint, and input control signals from 10% to 90% of V_{CC} with $t_R = t_F$ = 20ns.

SYMBOL	PARAMETER	NOTES	CONDITIONS	MIN	TYP (Note 3)	MAX	UNITS
Digital and DC (Continued)							
I_{CC}	V_{CC} Supply Current	4	No output load, $V_{CC} = V_{REF}$ = 5.5V			5.5	mA
I_{SS}	V_{SS} Supply Current	4	No output load, V_{SS} = –5.5V, $V_{CC} = V_{REF}$ =5.5V			–3.5	mA
I_{CCI}	V_{CC} Supply Current, Power Down Mode		No output load, power down mode			2.0	mA
I_{SSI}	V_{SS} Supply Current, Power Down Mode		No output load, power down mode			–100	µA
Digital Timing							
t_{CKI}	CLK_{IN} On/Off Period	4	$t_R = t_F$ = 10ns, 2.5V midpoint	30			ns
t_{SCK}	SCK On/Off Period	4		100			ns
t_{DS}	SID DATA Setup Time	4		50			ns
t_{DH}	SID DATA Hold Time	4		50			ns
t_{LPW}	LATI Pulse Width	4		50			ns
t_{LH}	LATI Hold Time	4		50			ns
t_{LS}	LATI Setup Time	5		50			ns
Clock Output							
$f_{CLK}1$	$CLK_{OUT}1$ Output Frequency	4	Figure 2	½		½	f_{CLKIN}
$f_{CLK}2$	$CLK_{OUT}2$ Output Frequency	4	Figure 2	⅛		⅛	f_{CLKIN}
t_{1R}, t_{2R}	CLK_{OUT1}, CLK_{OUT2}, Output Rise Time	5	C_L=40pF, 10% and 90% transition point	0		20	ns
		4	C_L=100pF, 0.8V and 2.0V transition point	0		20	ns
t_{1F}, t_{2F}	CLK_{OUT1}, CLK_{OUT2}, Output Fall Time	5	C_L=40pF, 10% and 90% transition point	0		20	ns
		4	C_L=100pF, 0.8V and 2.0V transition point	0		20	ns

Note 1: Absolute maximum ratings are limits beyond which the life of the integrated circuit may be impaired. All voltages unless otherwise specified are measured with respect to ground.

Note 2: 0°C to +70°C and –40°C to +85°C operating temperature range devices are 100% tested with temperature limits guaranteed by 100% testing, sampling, or by correlation with worst-case test conditions.

Note 3: Typicals are parametric norm at 25°C.

Note 4: Parameter guaranteed and 100% production tested.

Note 5: Parameter guaranteed. Parameters not 100% tested are not in outgoing quality level calculation.

Note 6: Maximum peak-to-peak voltage for output sinewave is $V_{OUTP-P} \leq (125kV \times Hz)/f_{OUT}$. For example at 50kHz output the maximum guaranteed voltage swing is $2.5V_{P-P}$.

Note 7: Offset voltage is a function of the peak-to-peak output voltage, for example if V_{OUTP-P} = 2.5V, V_{OS} = ±50mV max.

TIMING DIAGRAMS

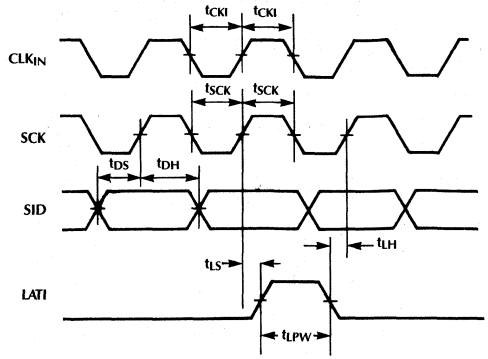
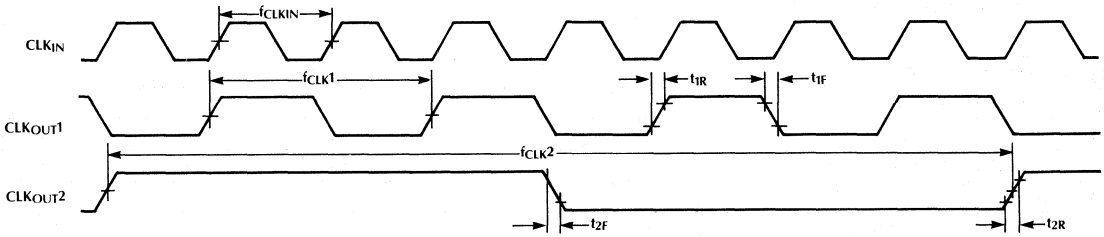


Figure 1. Serial Interface Timing



fCLK PARAMETERS REFERRED TO 1.4V MIDPOINT

Figure 2. ML2036 Digital Clock Output Timing

TYPICAL PERFORMANCE

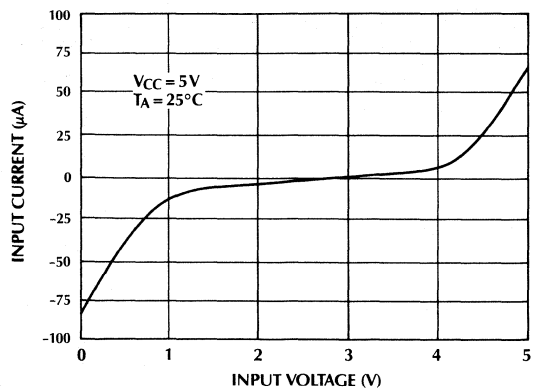


Figure 3. CLK_{IN} Input Current vs. Input Voltage

1.0 FUNCTIONAL DESCRIPTION

The ML2035 and ML2036 are composed of a programmable frequency generator, sinewave generator, crystal oscillator, and serial digital interface. The ML2035 and ML2036 frequency and sinewave generator functional block diagram is shown in figure 4.

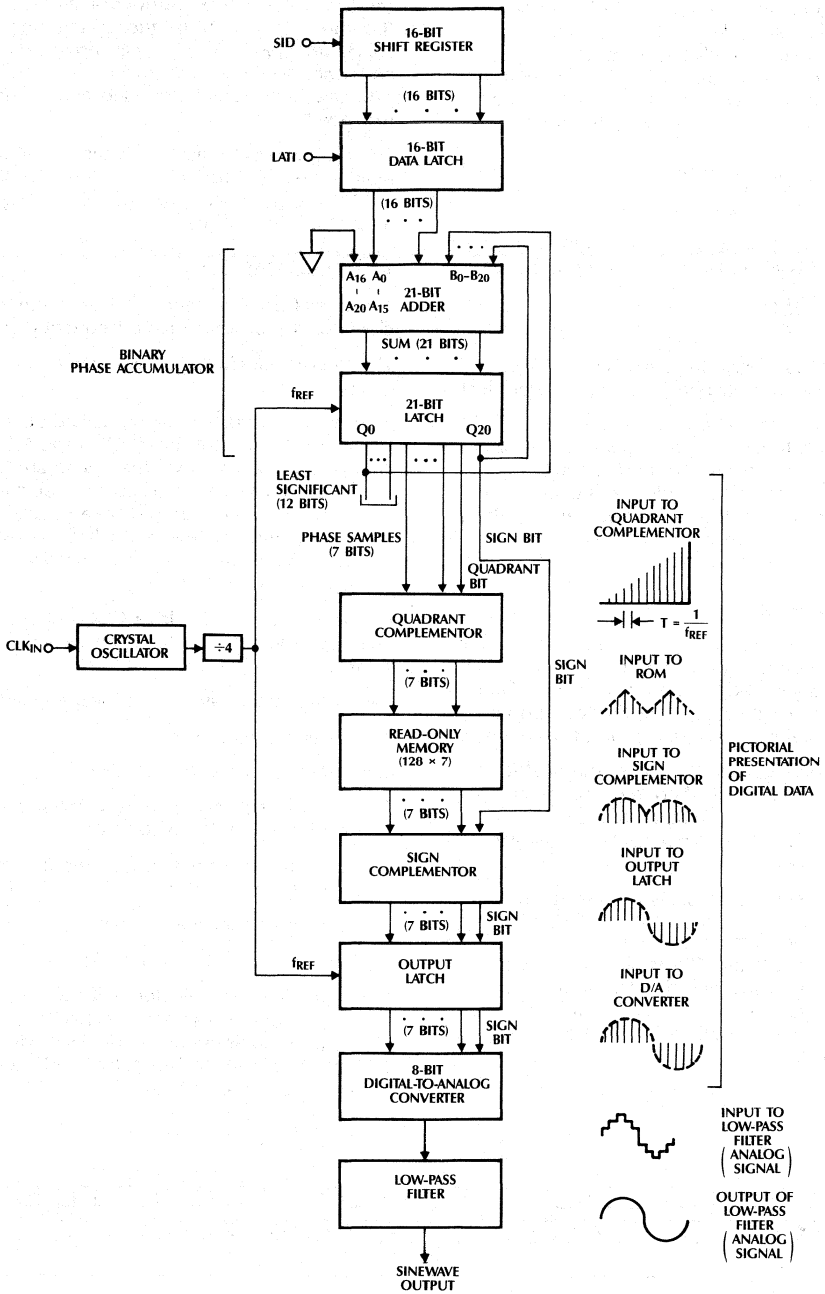


Figure 4. Frequency and Sinewave Generator Functional Block Diagram

1.1 Programmable Frequency Generator

The programmable frequency generator produces a digital output whose frequency is determined by a 16-bit digital word.

The frequency generator is composed of a phase accumulator which is clocked at $f_{CLKIN/4}$. The value stored in the data latch is added to the phase accumulator every 4 cycles of CLK_{IN}. The frequency of the analog output is equal to the rate at which the accumulator overflows and is given by the following equation:

$$f_{OUT} = \frac{f_{CLKIN} \times (D15\text{–}D0)_{DEC}}{2^{23}}$$

The frequency resolution and the minimum frequency are the same and is given by the following equation:

$$\Delta f_{MIN} = \frac{f_{CLKIN}}{2^{23}}$$

When f_{CLKIN} = 12.352MHz, Δf_{MIN} = 1.5Hz (±.75Hz). Lower frequencies are obtained by using a lower clock.

Due to the phase quantization nature of the frequency generator spurious tones can be present in the output in the range of –55dB relative to fundamental. The energy from these tones is included in the signal to noise + distortion specification. The frequency of these tones can be very close to the fundamental, therefore it is not practical to filter them out.

1.2 Sinewave Generator

The sinewave generator is composed of a sine look-up table, a DAC, and an output smoothing filter. The sine look-up table is addressed by the phase accumulator. The DAC is driven by the output of the look-up table and generates a staircase representation of a sinewave.

The output smoothing filter "smooths" the analog output by removing the high frequency sampling components. The resultant voltage on V_{OUT} is a sinusoid with all distortion components at least 45dB below the fundamental.

The ML2035 provides a peak sinewave voltage of $\pm V_{CC}/2$. The ML2036 has a V_{REF} input that can be tied to V_{CC} or generated from an external voltage. With the gain input equal to a logic "1" the sinewave peak voltage is equal to $\pm V_{REF}$; with the gain input equal to a logic "0" the peak voltage is $\pm V_{REF}/2$. The sinewave output is referenced to AGND for the ML2036 and GND for the ML2035.

The analog section is designed to operate over a range from DC to 50kHz. Due to slew rate limitations, the peak-to-peak output voltage must be limited to $V_{OUTP\text{-}P} \leq (125kV \times Hz)/f_{OUT}$. For example on the ML2036 an output at 50kHz must be limited to $2.5V_{P\text{-}P}$. Since the ML2035 peak-to-peak output voltage is equal to V_{CC}, the maximum output frequency must be limited to 25kHz for V_{CC} = 5V. V_{OUT} can drive 1kΩ, 100pF loads and swing to within 1.5V of V_{CC} and V_{SS}, provided the slew rate limitations mentioned above are not exceeded.

The output offset voltage, V_{OS}, is a function of the peak-to-peak output voltage and is specified as 25mV + (±10 × $V_{OUTP\text{-}P}$) max. For example if $V_{OUTP\text{-}P}$ = 2.5V, then V_{OS} = 50mV max.

1.3 Crystal Oscillator

The crystal oscillator generates an accurate reference clock for the programmable frequency generator.

The internal clock can be generated with a crystal or external clock.

If a crystal is used, it must be placed between CLK_{IN} and DGND of the ML2036 or GND of the ML2035. An on chip crystal oscillator will then generate the internal clock. No other external capacitors or components are required. The crystal should be a parallel resonant type with a frequency between 3MHz to 12.4MHz. It should be placed physically as close as possible to the CLK_{IN} and DGND (GND).

An external clock can drive CLK_{IN} directly if desired. The frequency of this clock can be anything from 0 to 12MHz.

The crystal must have the following characteristics:

1. Parallel resonant type
2. Frequency: 3MHz to 12.4MHz
3. Maximum equivalent series resistance of 15Ω at a drive level of 1μW to 200μW
4. Maximum equivalent series resistance of 30Ω at drive levels of 10nW to 1μW
5. Typical load capacitance: 18pF
6. Maximum case capacitance: 7pF

The frequency of oscillation will be a function of the crystal parameters and board capacitance. Crystals that meet these requirements at 12.352000MHz are M-tron 3709-010 12.352 for 0°C to +70°C and 3709-020 12.352 for –40°C to +85°C operation.

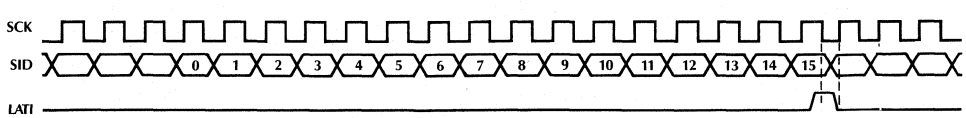


Figure 5. Serial Interface Timing

The ML2036 has two clock outputs that can be used to drive other external devices. The $CLK_{OUT}1$ output is a buffered output from the oscillator divided by 2. The $CLK_{OUT}2$ output is a buffered output from the oscillator divided by 8.

1.4 Serial Digital Interface

The digital interface consists of a shift register and data latch. The serial 16-bit data word on SID is clocked into a 16-bit shift register on rising edges of the serial shift clock, SCK. The LSB should be shifted in first and the MSB last as shown in figure 5. The data that has been shifted into the shift register is loaded into a 16-bit data latch on the falling edge of LATI. To insure that true data is loaded into the data latch from the shift register, LATI falling edge should occur when SCK is low, as shown in figure 1. LATI should be low while shifting data into the shift register to avoid inadvertantly entering the power down mode as described in paragraph 1.5. Note that all data is entered and latched on edges, not levels, of SCK and LATI.

1.5 Inhibit and Power Down Modes

1.5.1 ML2035 Power Down Mode

The power down mode of the ML2035 can be selected by entering all zeros in the shift register and applying a logic "1" to LATI. A zero data detect circuit detects when all bits in the shift register are zero's. In this state, the power consumption is reduced to 11.5mW max, and V_{OUT} goes to 0V as shown in figure 6 and appears as 10k to analog ground. The master clock, CLK_{IN}, can be left active or removed during power down mode.

1.5.2 ML2036 Inhibit and Power Down Modes

The ML2036 has an inhibit mode and a power down mode which are controlled by the three-level P_{DN}–INH input as described in table 1. When a logic "1", V_{I3}, is applied to the P_{DN}–INH pin, the power down mode is entered in the same way as described for the ML2035. Also, the ML2036 will be placed in the power down mode by applying a logic "0" to the P_{DN}–INH pin.

If V_{SS} to V_{SS} + .5V, V_{I2}, is applied to the P_{DN}–INH pin, the inhibit mode is entered by shifting all zero's into the shift register and applying a logic "1" to the LATI pin. Once the inhibit mode is entered V_{OUT} will complete the last half cycle of the sinewave and then be held at approximately V_{OS}, such that no voltage step occurs, as shown in figure 6.

P_{DN}–INH MODE	P_{DN}–INH PIN	DATA IN SHIFT REG.	LATI	SINEWAVE OUTPUT
P_{DN} (1)	V_{I1}, Logic "0"	X	X	V_{OUT} = 0V (10K to AGND)
Inhibit	V_{I2}, Inhibit State Voltage, V_{SS} to V_{SS} + .5V	All 0's	Logic "1"	V_{OUT} goes to approximately V_{OS} at the next V_{OS} crossing. See figure 6.
P_{DN} (1)	V_{I3}, Logic "1"	All 0's	Logic "1"	V_{OUT} = 0V (10K to AGND)

Note 1: In the power down mode, the oscillator, CLK_{OUT1} and CLK_{OUT2}, shift register, and data latch are all functional.

Table 1. Three Level P_{DN}–INH Function

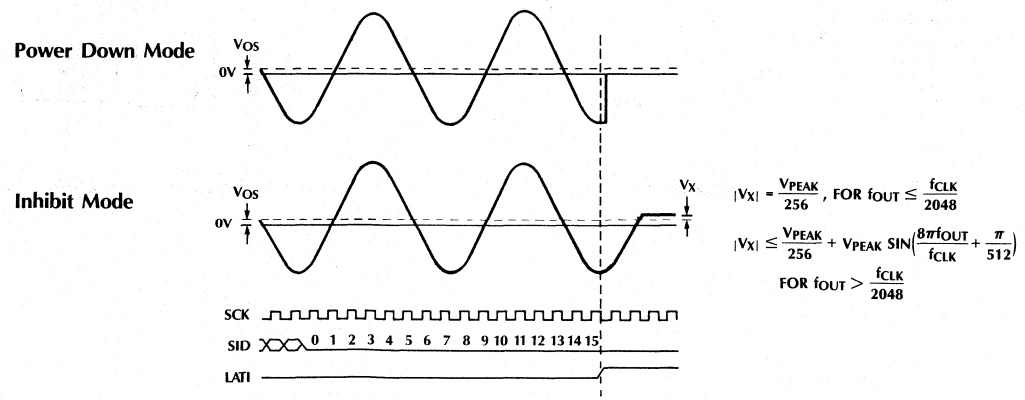


Figure 6. Power Down and Inhibit Mode

1.6 Power Supplies

The analog circuitry in the device are powered from +5V to –5V (V_{CC} to V_{SS}) and are referenced to AGND.

The digital circuits in the device are powered from +5V to 0V (V_{CC} to DGND).

For the ML2036, it is recommended that AGND and DGND be connected together close to the device and have a good connection back to the power source.

It is recommended that the power supplies to the device should be bypassed by placing decoupling capacitors from V_{CC} to AGND (GND for ML2035) and V_{SS} to AGND (GND for ML2035) as physically close to the device as possible.

2.0 TYPICAL APPLICATIONS

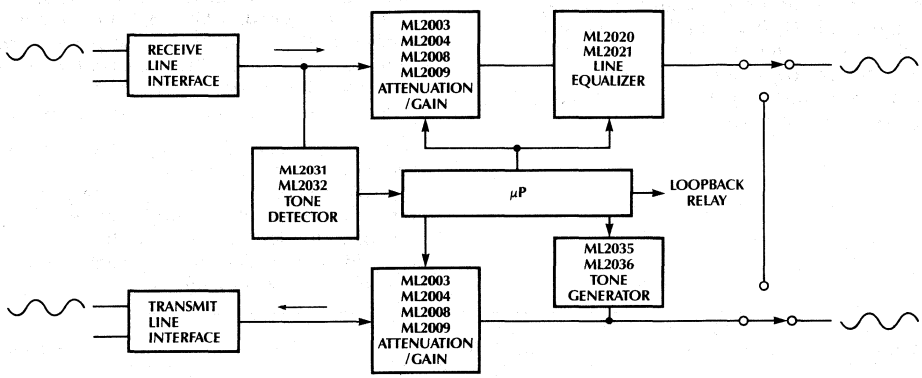


Figure 7. 4-Wire Termination Equipment

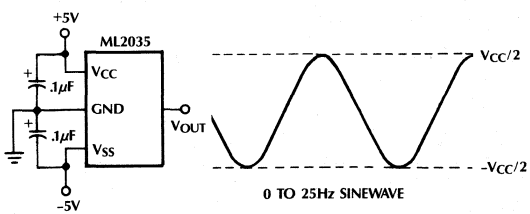


Figure 8. Sinewave Ratiometric to $\pm V_{CC}/2$

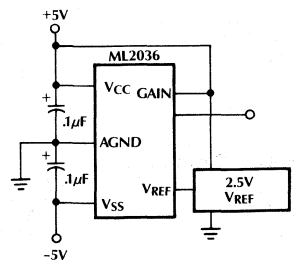


Figure 9. Sinewave with $\pm 2.5V_{P-P}$ ($5V_{P-P}$)

ORDERING INFORMATION

PART NUMBER	PACKAGE	TEMPERATURE RANGE
ML2035IJ	8-Pin Hermetic DIP	–40°C to +85°C
ML2035CP	8-Pin Molded DIP	0°C to +70°C
ML2036IJ	14-Pin Hermetic DIP	–40°C to +85°C
ML2036CP	14-Pin Molded DIP	0°C to +70°C
ML2036CS	16-Pin Molded SOIC	0°C to +70°C

ML2110

Universal Dual Filter

GENERAL DESCRIPTION

The ML2110 consists of two independent switched capacitor filters that perform second order filter functions such as lowpass, bandpass, highpass, notch and allpass. All filter configurations including Butterworth, Bessel, Cauer, and Chebyshev can be formed.

The center frequency of these filters is tuned by an external clock or the external clock and resistor ratio.

The ML2110 frequency range is specified to 30kHz with ±2.25V (single 5V operation) to ±5.5V power supplies.

For higher frequency operation the ML2111 is specified up to 150kHz operation.

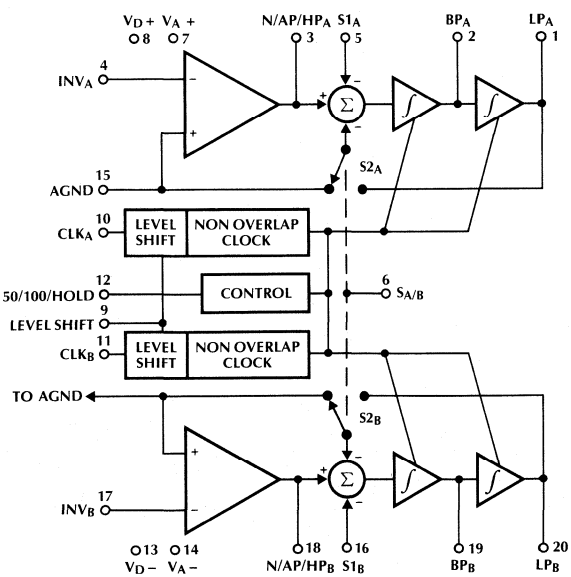
These filters are ideal where center frequency accuracy and high Qs are needed.

The ML2110 is a pin compatible superior replacement for MF10, LMF100, and LTC1060 filters.

FEATURES

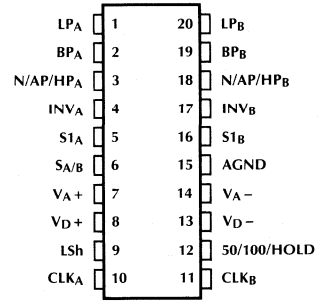
- Specified to 30kHz
- Center frequency × Q product ≤2MHz
- Separate highpass, notch, allpass, bandpass, and lowpass outputs
- Center frequency accuracy ±0.3% or ±0.8% max
- Q accuracy ±3% or ±6% max
- Clock inputs TTL or CMOS compatible with duty cycle 40% to 60%
- Single 5V (±2.25V) or ±5V supply operation
- 0°C to 70°C, −40°C to +85°C, −55°C to +125°C operating temperature range
- Standard 0.3″ 20-pin DIP or 20-pin small outline (SOIC) package

BLOCK DIAGRAM



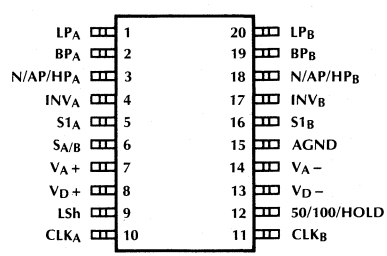
PIN CONNECTIONS

ML2110
20-PIN DIP



TOP VIEW

ML2110
20-PIN SOIC



TOP VIEW

PIN DESCRIPTION

PIN NO.	NAME	FUNCTION
1	LP_A	Lowpass output for biquad A.
2	BP_A	Bandpass output for biquad A.
3	$N/AP/HP_A$	Notch/allpass/highpass output for biquad A.
4	INV_A	Inverting input of the summing op amp for biquad A.
5	$S1_A$	Auxiliary signal input pin used in modes 1a, 1d, 4, 5, and 6b.
6	$S_{A/B}$	Controls S2 input function.
7	V_A+	Positive analog supply.
8	V_D+	Positive digital supply.
9	LSh	Reference point for clock input levels. Logic threshold typically 1.4V above LSh voltage.
10	CLK_A	Clock input for biquad A.
11	CLK_B	Clock input for biquad B.
12	50/100/HOLD	Input pin to control the clock to center frequency ratio of 50:1 or 100:1, or stops the clock to hold the last sample of the bandpass or lowpass outputs.
13	V_D-	Negative digital supply.
14	V_A-	Negative analog supply.
15	AGND	Analog ground.
16	$S1_B$	Auxiliary signal input used in modes 1a, 1d, 4, 5, and 6b.
17	INV_B	Inverting input of the summing op amp for biquad B.
18	$N/AP/HP_B$	Notch/allpass/highpass output for biquad B.
19	BP_B	Bandpass output for biquad B.
20	LP_B	Lowpass output for biquad B.

3

ABSOLUTE MAXIMUM RATINGS
(Note 1)

Supply Voltage
- $|V_A+|, |V_D+| - |V_A-|, |V_D-|$ 13V
- V_A+, V_D+ to LSh 13V

Inputs ..... $|V_A+, V_D+|+0.3V$ to $|V_A-, V_D-|-0.3V$
Outputs ..... $|V_A+, V_D+|+0.3V$ to $|V_A-, V_D-|-0.3V$
$|V_A+|$ to $|V_D+|$ ..... ±0.3V
Power Dissipation 750mW
Storage Temperature Range ..... −65°C to 150°C
Lead Temperature (soldering, 10 sec) ..... 300°C

OPERATING CONDITIONS

Temperature Range (Note 2)
- ML2110BCP, ML2110CCP, ML2110BCS, ML2110CCS ..... 0°C to 70°C
- ML2110BIJ, ML2110CIJ ..... −40°C to +85°C
- ML2110BMJ, ML2110CMJ ..... −55°C to +125°C

Supply Voltage Range ..... ±2.25V to ±6.0V

ELECTRICAL CHARACTERISTICS

Unless otherwise specified $T_A = T_{MIN}$ to T_{MAX}, $V_A+ = V_D+ = 5V \pm 10\%$, $V_A- = V_D- = -5V \pm 10\%$, $C_L = 25pF$, $V_{IN} = 2.5V_{PK}$ (1.767 V_{RMS}) Clock Duty Cycle 40% to 60%.

			ML2110B			ML2110C			
PARAMETER	NOTES	CONDITIONS	MIN	TYP NOTE 3	MAX	MIN	TYP NOTE 3	MAX	UNITS
Filter									
f_o, Center Frequency Maximum	5, 6	Figure 16 (Mode 1)							
		$Q \leq 50$, Q Accuracy $\leq \pm 20\%$			20			20	kHz
		$Q \leq 20$, Q Accuracy $\leq \pm 10\%$			30			30	kHz
f_o, Center Frequency Minimum	5, 6	Figure 16 (Mode 1)							
		$Q \leq 50$, Q Accuracy $\leq \pm 30\%$	25			25			Hz
		$Q \leq 20$, Q Accuracy $\leq \pm 15\%$	25			25			Hz
f_o, Temperature Coefficient		$f_{CLK} < 1MHz$		−10			−10		ppm/°C
Clock to Center Frequency Ratio		Q = 10							
		Figure 16 (Mode 1)							
	4	50:1, $f_{CLK} = 250kHz$	49.85	50.0	50.15	49.60	50.0	50.40	
	4	100:1, $f_{CLK} = 500kHz$	100.0	100.3	100.6	99.50	100.3	101.1	

ELECTRICAL CHARACTERISTICS (Continued)

Unless otherwise specified $T_A = T_{MIN}$ to T_{MAX}, $V_A+ = V_D+ = 5V \pm 10\%$, $V_A- = V_D- = -5V \pm 10\%$, $C_L = 25pF$, $V_{IN} = 2.5V_{PK}$ (1.767 V_{RMS}) Clock Duty Cycle 40% to 60%.

PARAMETER	NOTES	CONDITIONS	ML2110B MIN	ML2110B TYP NOTE 3	ML2110B MAX	ML2110C MIN	ML2110C TYP NOTE 3	ML2110C MAX	UNITS
Filter (Continued)									
Clock Frequency	5	Q ≤ 20, Q Accuracy ≤ ±15%	2.5k		1.5M	2.5k		1.5M	Hz
Clock Feedthrough	5	$f_{CLK} \leq 1MHz$		10	20		10	20	mV(p-p)
Q Accuracy	4	f_o = 5kHz, Q = 10, Figure 16 (Mode 1) 50:1			±3			±6	%
		f_o = 5kHz, Q = 10, Figure 16 (Mode 1) 100:1			±4			±8	%
Q Temperature Coefficient		$f_{CLK} < 500kHz$, Q = 10		20			20		ppm/°C
DC Offset		50:1, $f_{CLK} = 250kHz$							
$V_{OS\,2,3}$	4	$S_{A/B}$ High		7	40		7	60	mV
$V_{OS\,2,3}$	4	$S_{A/B}$ Low		7	40		7	60	mV
DC Offset		100:1, $f_{CLK} = 500kHz$							
$V_{OS\,2,3}$	4	$S_{A/B}$ High		14	60		14	100	mV
$V_{OS\,2,3}$	4	$S_{A/B}$ Low		14	60		14	100	mV
Gain Accuracy									
DC Lowpass	4	R1 = 20k, R2 = 2k, R3 = 20k		0.01	2		0.01	2	%
Bandpass at f_o	4	100:1, f_o = 5kHz, Q = 10		1	4		1	8	%
DC Notch Output	5			0.02	2		0.02	2	%
Noise	7	Figure 16 (Mode 1) Q = 1, R1 = R2 = R3 = 2k							
		Bandpass, 5kHz, 50:1		80			80		μV_{RMS}
		5kHz, 100:1		100			100		μV_{RMS}
		Lowpass, 5kHz, 50:1		105			105		μV_{RMS}
		5kHz, 100:1		130			130		μV_{RMS}
		Notch, 5kHz, 50:1		80			80		μV_{RMS}
		5kHz, 100:1		100			100		μV_{RMS}
		Figure 16 (Mode 1) Q = 10, R1 = R3 = 20k, R2 = 2k							
		Bandpass, 5kHz, 50:1		256			256		μV_{RMS}
		5kHz, 100:1		315			315		μV_{RMS}
		Lowpass, 5kHz, 50:1		262			262		μV_{RMS}
		(R1 = 2k) 5kHz, 100:1		320			320		μV_{RMS}
		Notch, 5kHz, 50:1		33			33		μV_{RMS}
		(R1 = 2k) 5kHz, 100:1		38			38		μV_{RMS}
Crosstalk		f_{CLK} = 250kHz, f_o = 5kHz		−70			−70		dB
Filter, $V_A+ = V_D+ = 2.25V$, $V_A- = V_D- = -2.25V$, $V_{IN} = 0.707\ V_{PK}$ (0.5 V_{RMS})									
f_o, Center Frequency Maximum	5	Figure 16 (Mode 1)							
		Q ≤ 50, Q Accuracy ≤ ±25%			20			20	kHz
		Q ≤ 20, Q Accuracy ≤ ±12%			30			30	kHz
f_o, Center Frequency Minimum	5	Figure 16 (Mode 1)							
		Q ≤ 50, Q Accuracy ≤ ±30%	25			25			Hz
		Q ≤ 20, Q Accuracy ≤ ±15%	25			25			Hz
Clock to Center Frequency Ratio		Q = 10, Figure 16 (Mode 1)							
	4	50:1, f_{CLK} = 250kHz	49.85	50.0	50.15	49.60	50.0	50.40	
	5	100:1, f_{CLK} = 500kHz	100.0	100.3	100.6	99.50	100.3	101.1	
Clock Frequency	5	Q ≤ 20, Q Accuracy ≤ ±15%	2.5k		1.5M	2.5k		1.5M	Hz
Q Accuracy	4	f_{CLK} = 250kHz, Q = 10, 50:1			±4			±8	%
		Figure 16 (Mode 1) 100:1		±3			±6		%

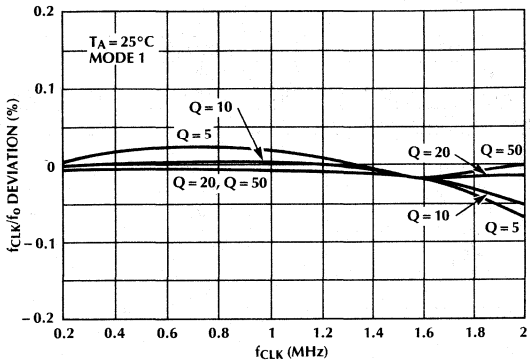
ELECTRICAL CHARACTERISTICS (Continued)

Unless otherwise specified $T_A = T_{MIN}$ to T_{MAX}, $V_A+ = V_D+ = 5V \pm 10\%$, $V_A- = V_D- = -5V \pm 10\%$, $C_L = 25pF$, $V_{IN} = 2.5V_{PK}$ (1.767 V_{RMS}) Clock Duty Cycle 40% to 60%.

PARAMETER	NOTES	CONDITIONS	ML2110B MIN	ML2110B TYP NOTE 3	ML2110B MAX	ML2110C MIN	ML2110C TYP NOTE 3	ML2110C MAX	UNITS
Filter, $V_A+ = V_D+ = 2.25V$, $V_A- = V_D- = -2.25V$, $V_{IN} = 0.707\ V_{PK}$ (0.5 V_{RMS}) (Continued)									
Noise	7	Figure 16 (Mode 1)							
		Q = 1, R1 = R2 = R3 = 2k							
		Bandpass, 5kHz, 50:1		80			80		μV_{RMS}
		5kHz, 100:1		100			100		μV_{RMS}
		Lowpass, 5kHz, 50:1		105			105		μV_{RMS}
		5kHz, 100:1		130			130		μV_{RMS}
		Notch, 5kHz, 50:1		80			80		μV_{RMS}
		5kHz, 100:1		100			100		μV_{RMS}
		Figure 16 (Mode 1)							
		Q = 10, R1 = R3 = 20k, R2 = 2k							
		Bandpass, 5kHz, 50:1		256			256		μV_{RMS}
		5kHz, 100:1		315			315		μV_{RMS}
		Lowpass, 5kHz, 50:1		262			262		μV_{RMS}
		(R1 = 2k) 5kHz, 100:1		320			320		μV_{RMS}
		Notch, 5kHz, 50:1		33			33		μV_{RMS}
		(R1 = 2k) 5kHz, 100:1		38			38		μV_{RMS}
Operational Amplifiers and Power Supply									
V_{OS} DC Offset	4			2	15		2	15	mV
DC Open Loop Gain		$R_L = 1k$		95			95		dB
Gain Bandwidth Product				2.4			2.4		MHz
Slew Rate				2.0			2.0		V/μs
Output Voltage Swing (Clipping Level)	5	$R_L = 2k$, $\|V\|$ from V_{A+} or V_{A-}		.5	1.2		.5	1.2	V
Output Short Circuit Current		Source		50			50		mA
		Sink		25			25		mA
Power Supply And Clock									
Supply Current	4	$f_{CLK} = 250kHz$							
$(I_A+) + (I_D+)$				13	22		13	22	mA
$(I_A-) + (I_D-)$				12	21		12	21	mA
I_{LSH}				0.5	1		0.5	1	mA
V_{CLK} Input Threshold	4	Low			0.8			0.8	V
		High	2.0			2.0			V
CLKA, CLKB Pulse Width	5	CLK High or CLK Low	250			250			ns

Note 1: Absolute maximum ratings are limits beyond which the life of the integrated circuit may be impaired. All voltages unless otherwise specified are measured with respect to ground.
Note 2: −55°C to +125°C operating temperature range devices are 100% tested at temperature extremes with worst-case test conditions. 0°C to 70°C and −40°C to +85°C operating temperature range devices are 100% tested with temperature limits guaranteed by 100% testing, sampling, or by correlation with worst-case test conditions.
Note 3: Typicals are parametric norm at 25°C.
Note 4: Parameter guaranteed and 100% production tested.
Note 5: Parameter guaranteed. Parameters not 100% tested are not in outgoing quality level calculation.
Note 6: Center frequency is defined as the peak of the bandpass output.
Note 7: The noise is measured with the HP8903A audio analyzer with a bandwidth of 30kHz which is 6 times the f_o at 50:1 or at 100:1.

TYPICAL PERFORMANCE CURVES



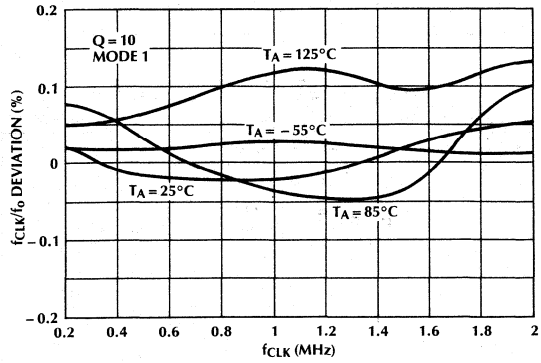


Figure 1. f_{CLK}/f_o vs. f_{CLK} (100:1, 50:1 at $V_S = \pm 2.5V$ or $V_S = \pm 5V$)

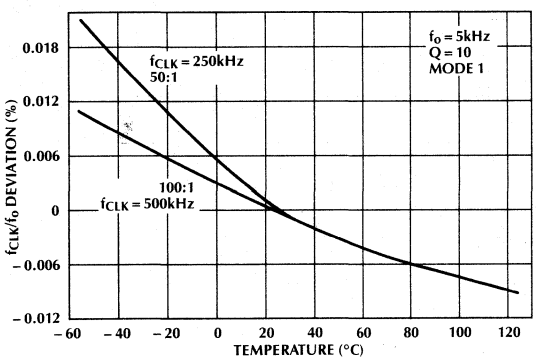


Figure 2A. f_{CLK}/f_o Deviation vs. Temperature ($V_S = \pm 5V$)

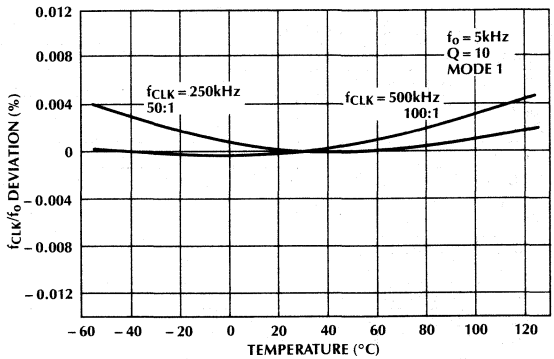
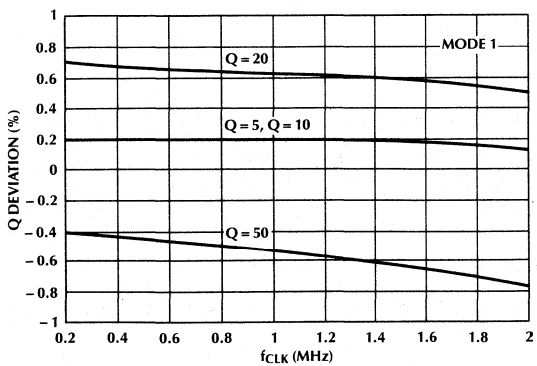


Figure 2B. f_{CLK}/f_o Deviation vs. Temperature ($V_S = \pm 2.5V$)



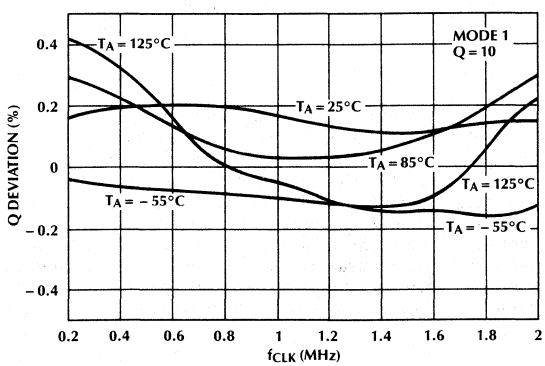


Figure 3. Q Error vs. f_{CLK} (100:1, 50:1 at $V_S = \pm 2.5V$ or $V_S = \pm 5V$)

TYPICAL PERFORMANCE CURVES (Continued)

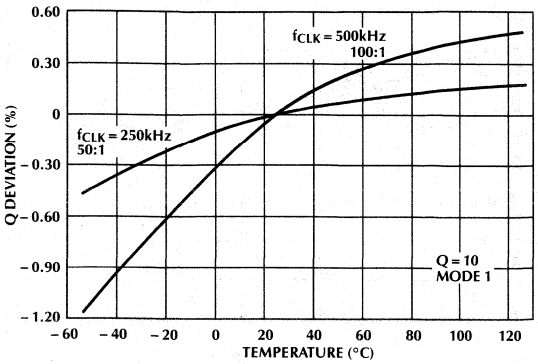


Figure 4A. Q Deviation vs. Temperature ($V_S = \pm 5V$)

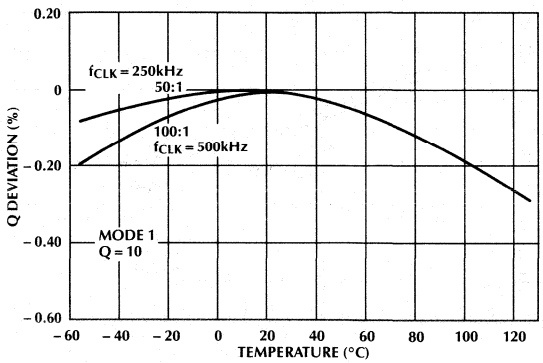


Figure 4B. Q Deviation vs. Temperature ($V_S = \pm 2.5V$)

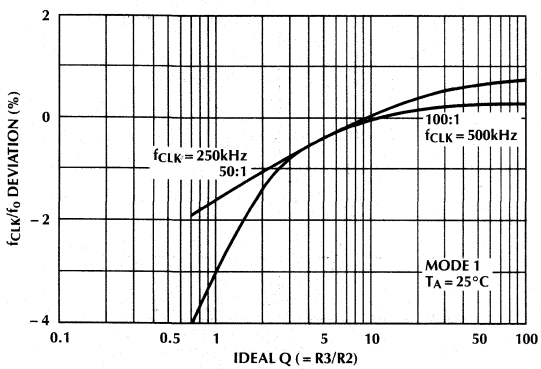


Figure 5A. f_{CLK}/f_o Deviation vs. Q ($V_S = \pm 5V$)

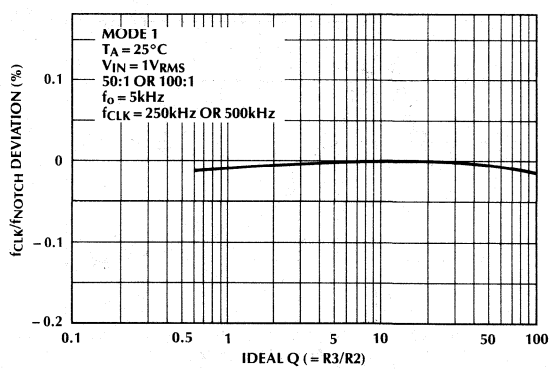


Figure 5B. f_{CLK}/f_{NOTCH} Deviation vs. Q ($V_S = \pm 5V$)

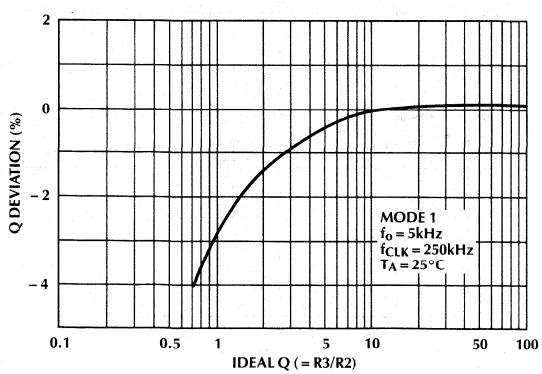


Figure 6A. Q Deviation vs. Q (50:1, $V_S = \pm 5V$)

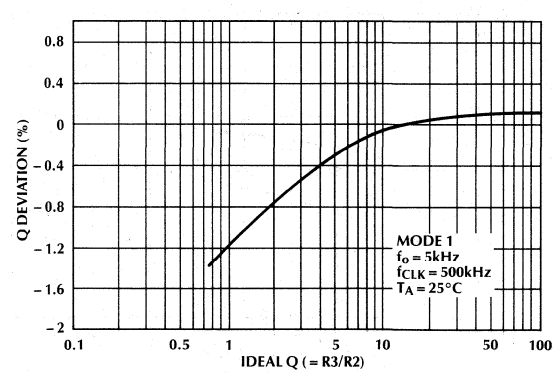


Figure 6B. Q Deviation vs. Q (100:1, $V_S = \pm 5V$)

TYPICAL PERFORMANCE CURVES (Continued)

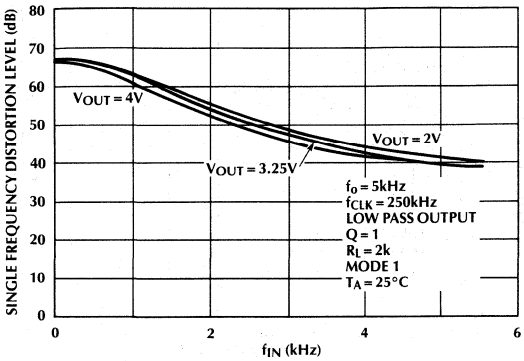


Figure 7A. Distortion vs. f_{IN} (50:1, $V_S = \pm 5V$)

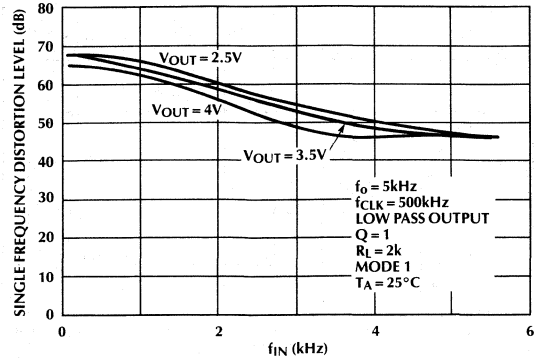


Figure 7B. Distortion vs. f_{IN} (100:1, $V_S = \pm 5V$)

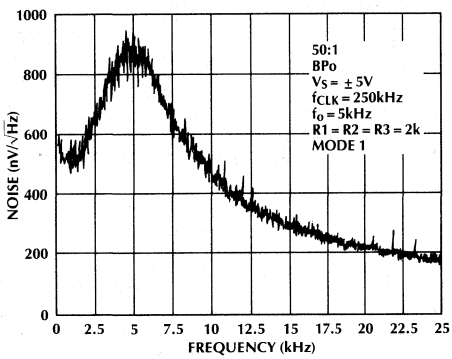


Figure 8A. Noise Spectrum Density (Q = 1)

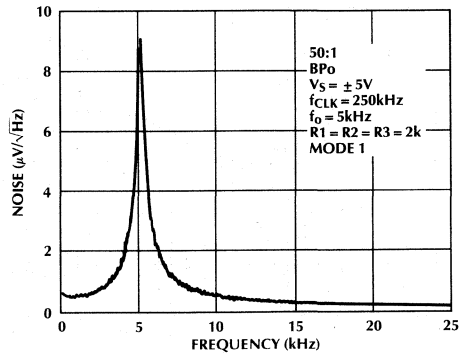


Figure 8B. Noise Spectrum Density (Q = 10)

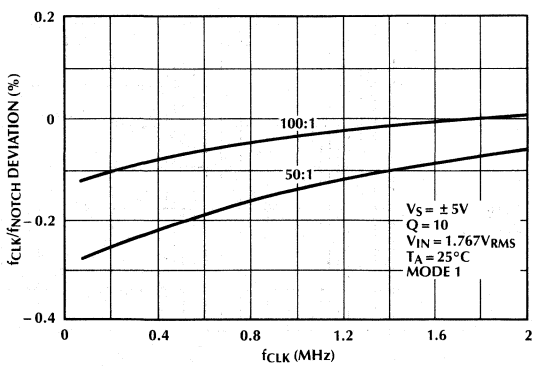


Figure 9. f_{CLK}/f_{NOTCH} vs. f_{CLK}

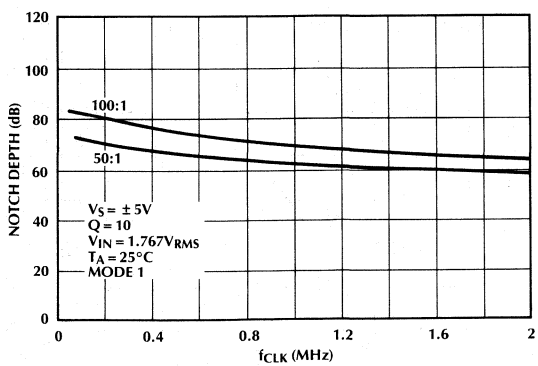


Figure 10. Notch Depth vs f_{CLK}

TYPICAL PERFORMANCE CURVES (Continued)

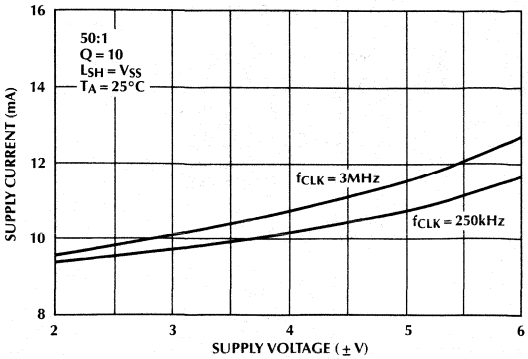


Figure 11. Supply Current vs. Supply Voltage

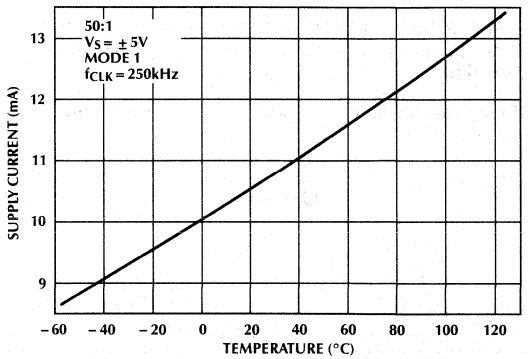


Figure 12. Supply Current vs. Temperature

FUNCTIONAL DESCRIPTION

POWER SUPPLIES

The analog (V_A+) and digital (V_D+) supply voltage pins, in most cases, are tied together and bypassed to AGND with a 0.1μF and a 0.01μF disc ceramic capacitor. If high digital noise exists, the supply pins can be bypassed separately. The ML2110 positive analog and positive digital supply pins are internally connected by the IC substrate and should be biased from the same DC source.

The ML2110 operates with a single supply from 5V±10% and with split supplies from ±4.5V to ±6V supplies.

CLOCK INPUT PINS AND LEVEL SHIFT

With dual supplies equal to or higher than ±4.0V, the level shift (LSh) pin 9 can be connected to the same potential as the AGND or V_A- pin. With single supply operation, the negative supply pins and the LSh pin should be tied to the system ground. The AGND, pin 15, should be biased at 1/2 supplies. Under these conditions, the clock levels are TTL or CMOS. The input clock pins (10, 11) share the same level shift pin.

50/100/HOLD (Pin 12)

By tying pin 12 to (V_A+, V_D+) the filter operates in the 50:1 mode. By tying pin 12 to 1/2 of the voltage supplies (AGND potential), the ML2110 operates in the 100:1 mode. The range of pin 12 with total supply voltage of +5V is 2.5±0.5V; +10V is 5V±0.5V. When pin 12 is tied to the negative supply pin, the filter operation is stopped and the bandpass and lowpass outputs act as an S/H circuit holding the last sample.

$S1_A$, $S1_B$, (Pins 5 and 16)

These are voltage signal input pins and should be driven with a source impedance below 5k. The $S1_A$, $S1_B$ pins can be used to alter the clock to center frequency ratio (f_{CLK}/f_o) of the filter (see modes 1b, 1c, 2a, 2b) or to feedforward the input signal for allpass filter configurations (see modes 4 and 5). When these pins are not used, they should be tied to the AGND pin.

$S_{A/B}$ (Pin 6)

When $S_{A/B}$ is high, the S2 negative input of the voltage summer is tied to the lowpass output. When the $S_{A/B}$ pin is connected to the negative supply, the S2 input switches to ground.

AGND (Pin 15)

AGND is connected to the system ground for dual supply operation. When operating with a single positive supply, the analog ground pin should be tied to 1/2 of the supply and bypassed with a 0.1μF capacitor. The positive inputs of the internal op amps and the reference point of the internal switches are connected to the AGND pin.

f_{CLK}/f_o RATIO

The ML2110 is a sampled data filter and approximates continuous time filters. The filter deviates from its ideal continuous filter model when the (f_{CLK}/f_o) ratio decreases and when the Qs are low.

$f_o \times Q$ PRODUCT RATIO

The $f_o \times Q$ product of the ML2110 depends on the clock frequency and the mode of operation. For clock frequencies below 1MHz, in mode 1 and its derivatives, the $f_o \times Q$ product is mainly limited by the desired f_o and Q accuracy. For the same clock frequency and for the same Q value the $f_o \times Q$ product can be further increased if the clock to center frequency ratio is lowered below 50:1.

Mode 3, Figure 24, and the modes of operation where R4 is finite, are "slower" than the basic mode 1. The resistor R4 places the input op amp inside the resonant loop. The finite GBW of this op amp creates an additional phase shift and enhances the Q value at high clock frequencies.

OUTPUT NOISE

The wideband RMS noise of the ML2110 outputs is nearly independent from the clock frequency provided that the clock itself does not become part of the noise. The noise at the BP and LP outputs increases for high Qs.

FILTER FUNCTION DEFINITIONS

Each filter of the ML2110 with an external clock and resistors approximates 2nd order filter functions. These are tabulated below in the frequency domain.

1. **Bandpass function:** available at the bandpass output pins (2, 19), Figure 13.

$$G(s) = H_{OBP}\frac{s\omega_o/Q}{s^2 + (s\omega_o/Q) + \omega_o^2}$$

H_{OBP} = Gain at $\omega = \omega_o$

$f_o = \omega_o/2\pi$; f_o is the center frequency of the complex pole pair. f_o is measured as the peak frequency of the bandpass output.

Q = Quality factor of the complex pole pair. It is the ratio of f_o to the −3dB bandwidth of the 2nd order bandpass function. The Q is always measured at the filter BP output.

2. **Lowpass function:** available at the LP output pins (1, 20), Figure 14.

$$G(s) = H_{OLP}\frac{\omega_o^2}{s^2 + s(\omega_o/Q) + \omega_o^2}$$

H_{OLP} = DC gain of the LP output.

3. **Highpass function:** available only in mode 3 at the output pins (3, 18), Figure 15.

$$G(s) = H_{OHP}\frac{s^2}{s^2 + s(\omega_o/Q) + \omega_o^2}$$

H_{OHP} = gain of the HP output for $f \rightarrow \frac{f_{CLK}}{2}$

4. **Notch function:** available at pins 3 (18) for several modes of operation.

$$G(s) = (H_{ON2})\frac{(s^2 + \omega^2_n)}{s^2 + s(\omega_o/Q) + \omega_o^2}$$

H_{ON2} = gain of the notch output for $f \rightarrow \frac{f_{CLK}}{2}$

H_{ON1} = gain of the notch output for $f \rightarrow 0$

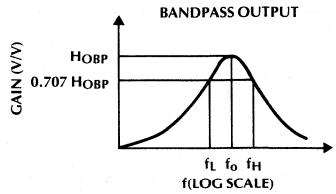
$f_n = \omega_n/2\pi$; f_n is the frequency of the notch occurrence.

5. **Allpass function:** available at pins 3(18) for mode 4, 4a.

$$G(s) = H_{OAP}\frac{[s^2 - s(\omega_o/Q) + \omega_o^2]}{s^2 + s(\omega_o/Q) + \omega_o^2}$$

H_{OAP} = gain of the allpass output for $0 < f < \frac{f_{CLK}}{2}$

For allpass functions, the center frequency and the Q of the numerator complex zero pair is the same as the denominator. Under these conditions, the magnitude response is a straight line. In mode 5, the center frequency f_Z, of the numerator complex zero pair, is different than f_o. For high numerator Q's, the magnitude response will have a notch at f_Z.

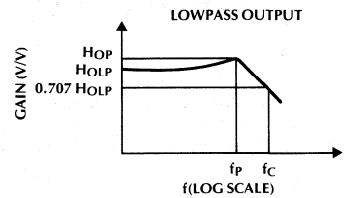


$$Q = \frac{f_o}{f_H - f_L};\ f_o = \sqrt{f_L f_H}$$

$$f_L = f_o\left(\frac{-1}{2Q} + \sqrt{\left(\frac{1}{2Q}\right)^2 + 1}\right)$$

$$f_H = f_o\left(\frac{1}{2Q} + \sqrt{\left(\frac{1}{2Q}\right)^2 + 1}\right)$$

Figure 13

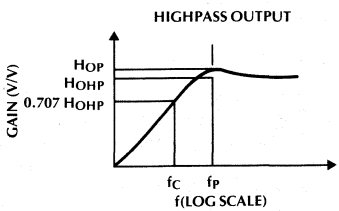


$$f_C = f_o \times \sqrt{\left(1 - \frac{1}{2Q^2}\right) + \sqrt{\left(1 - \frac{1}{2Q^2}\right)^2 + 1}}$$

$$f_P = f_o\sqrt{1 - \frac{1}{2Q^2}}$$

$$H_{OP} = H_{OLP} \times \frac{1}{\frac{1}{Q}\sqrt{1 - \frac{1}{4Q^2}}}$$

Figure 14



$$f_C = f_o \times \left[\sqrt{\left(1 - \frac{1}{2Q^2}\right) + \sqrt{\left(1 - \frac{1}{2Q^2}\right)^2 + 1}}\right]^{-1}$$

$$f_P = f_o \times \left[\sqrt{1 - \frac{1}{2Q^2}}\right]^{-1}$$

$$H_{OP} = H_{OHP} \times \frac{1}{\frac{1}{Q}\sqrt{1 - \frac{1}{4Q^2}}}$$

Figure 15

OPERATION MODES

Table 1. 1st Order Functions

MODE	PIN 2 (19)	PIN 3 (18)	f_C	f_Z
6a	LP	HP	$\frac{f_{CLK}}{100(50)} \times \frac{R2}{R3}$	
6b	LP	LP	$\frac{f_{CLK}}{100(50)} \times \frac{R2}{R3}$	
7	LP	AP	$\frac{f_{CLK}}{100(50)} \times \frac{R2}{R3}$	$\frac{f_{CLK}}{100(50)} \times \frac{R2}{R3}$

Table 2. 2nd Order Functions

MODE	PIN 1 (20)	PIN 2 (19)	PIN 3 (18)	f_o	f_N
1	LP	BP	Notch	$\frac{f_{CLK}}{100(50)}$	f_o
1a	LP	BP	BP	$\frac{f_{CLK}}{100(50)}$	
1b	LP	BP	Notch	$\frac{f_{CLK}}{100(50)} \times \sqrt{1 + \frac{R6}{R5+R6}}$	$\frac{f_{CLK}}{100(50)} \times \sqrt{1 + \frac{R6}{R5+R6}}$
1c	LP	BP	Notch	$\frac{f_{CLK}}{100(50)} \times \sqrt{\frac{R6}{R5+R6}}$	$\frac{f_{CLK}}{100(50)} \times \sqrt{\frac{R6}{R5+R6}}$
1d	LP	BP		$\frac{f_{CLK}}{100(50)}$	
2	LP	BP	Notch	$\frac{f_{CLK}}{100(50)} \times \sqrt{1 + \frac{R2}{R4}}$	$\frac{f_{CLK}}{100(50)}$
2a	LP	BP	Notch	$\frac{f_{CLK}}{100(50)} \times \sqrt{1 + \frac{R2}{R4} + \frac{R6}{R5+R6}}$	$\frac{f_{CLK}}{100(50)} \times \sqrt{1 + \frac{R6}{R5+R6}}$
2b	LP	BP	Notch	$\frac{f_{CLK}}{100(50)} \times \sqrt{\frac{R2}{R4} + \frac{R6}{R5+R6}}$	$\frac{f_{CLK}}{100(50)} \times \sqrt{\frac{R6}{R5+R6}}$
3	LP	BP	HP	$\frac{f_{CLK}}{100(50)} \times \sqrt{\frac{R2}{R4}}$	
3a	LP	BP	Notch	$\frac{f_{CLK}}{100(50)} \times \sqrt{\frac{R2}{R4}}$	$\frac{f_{CLK}}{100(50)} \times \sqrt{\frac{R_h}{R_l}}$
4	LP	BP	AP	$\frac{f_{CLK}}{100(50)}$	
4a	LP	BP	AP	$\frac{f_{CLK}}{100(50)} \times \sqrt{\frac{R2}{R4}}$	
5	LP	BP	C.Z	$\frac{f_{CLK}}{100(50)} \times \sqrt{1 + \frac{R2}{R4}}$	$\frac{f_{CLK}}{100(50)} \times \sqrt{1 - \frac{R1}{R4}}$

OPERATION MODES (Continued)

There are basically three modes of operation: mode 1, mode 2, mode 3. In the mode 1, Figure 16, the input amplifier is outside the resonant loop. Because of this, mode 1 and its derivatives (mode 1a, 1b, 1c, 1d) are faster than modes 2 and 3.

Mode 1a, Figure 17, represents the most simple hook-up of the ML2110. Mode 1a is useful when voltage gain at the bandpass output is required. The bandpass voltage gain, however, is equal to the value of Q, and a second order, clock tunable, BP resonator can be achieved with only 2 resistors. The filter center frequency directly depends on the external clock frequency. For high order filters, mode 1a is not practical as it requires several clock frequencies to tune the overall filter response.

Mode 1, Figure 16, provides a clock tunable notch. Mode 1 is a practical configuration for second order clock tunable bandpass/notch filters. In mode 1, a bandpass output with a very high Q, together with unity gain, can be obtained with the dynamics of the remaining notch and lowpass outputs.

Modes 1b and 1c, Figures 18, 19 are similar. They both produce a notch with a frequency which is always equal to the filter center frequency. The notch and the center frequency can be adjusted with an external resistor ratio.

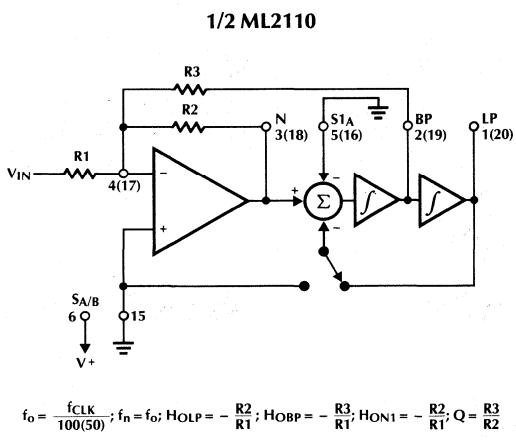
The clock to center frequency ratio range is:

$$\frac{500}{1} \geq \frac{f_{CLK}}{f_o} \geq \frac{100}{1} \text{ or } \frac{50}{1}; \text{ mode 1b}$$

$$\frac{100}{1} \text{ or } \frac{50}{1} \geq \frac{f_{CLK}}{f_o} \geq \frac{100}{\sqrt{2}} \text{ or } \frac{50}{\sqrt{2}}; \text{ mode 1c}$$

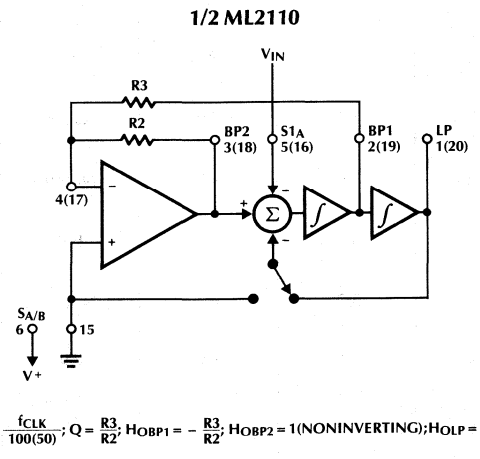
The input impedance of the S1 pin is clock dependent, and in general R5 should not be larger than 5k. Mode 1b can be used to increase the clock to center frequency ratio beyond 100:1. For this mode, the limit for the (f_{CLK}/f_o) ratio is 500:1. Beyond this, the filter will exhibit large output offsets. Mode 1d, Figure 20, is the fastest mode of operation: In the 50:1 mode center frequencies beyond 20kHz can easily be achieved.

Modes 2, 2a, and 2b have a notch output which frequency, f_n, can be tuned independently from the center frequency, f_o. For all cases, however, $f_n < f_o$. These modes are useful when cascading second order functions to create an overall elliptic highpass, bandpass or notch response. The input amplifier and its feedback resistors (R2/R4) are now part of the resonant loop. Because of this, mode 2 and its derivatives are slower than mode 1's.



$f_o = \frac{f_{CLK}}{100(50)}$; $f_n = f_o$; $H_{OLP} = -\frac{R2}{R1}$; $H_{OBP} = -\frac{R3}{R1}$; $H_{ON1} = -\frac{R2}{R1}$; $Q = \frac{R3}{R2}$

Figure 16. Mode 1: 2nd Order Filter Providing Notch, Bandpass, Lowpass

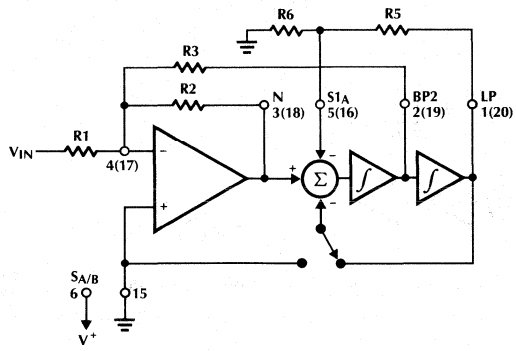


$f_o = \frac{f_{CLK}}{100(50)}$; $Q = \frac{R3}{R2}$; $H_{OBP1} = -\frac{R3}{R2}$; $H_{OBP2} = 1$(NONINVERTING); $H_{OLP} = -1$

Figure 17. Mode 1a: 2nd Order Filter Providing Bandpass, Lowpass

OPERATION MODES (Continued)

1/2 ML2110

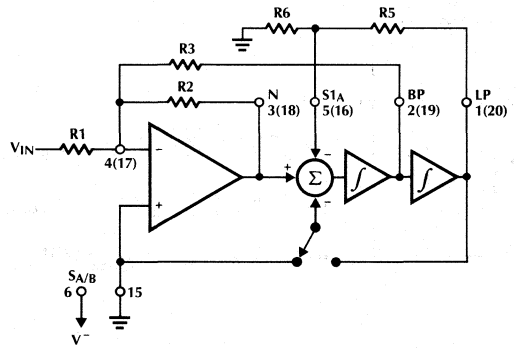


$$f_o = \frac{f_{CLK}}{100(50)}\sqrt{1+\frac{R6}{R5+R6}};\ f_n = f_o;\ Q = \frac{R3}{R2}\sqrt{1+\frac{R6}{R5+R6}};$$

$$H_{ON1}(f\to 0) = H_{ON2}\left(f-\frac{f_{CLK}}{2}\right) = -\frac{R2}{R1};\ H_{OBP} = -\frac{R3}{R1};\ H_{OLP} = \frac{-R2/R1}{1+R6/(R5+R6)};\ R5 < 5k\Omega$$

Figure 18. Mode 1b: 2nd Order Filter Providing Notch, Bandpass, Lowpass

1/2 ML2110

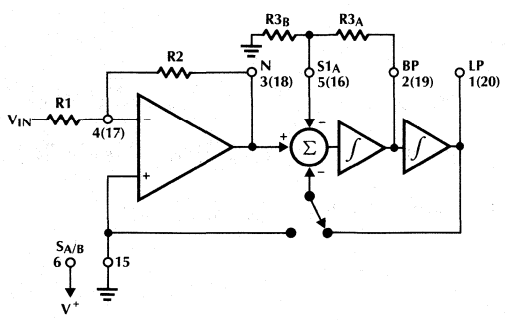


$$f_o = \frac{f_{CLK}}{100(50)}\sqrt{\frac{R6}{R5+R6}};\ f_n = f_o;\ Q = \frac{R3}{R2}\sqrt{\frac{R6}{R5+R6}};$$

$$H_{ON1}(f\to 0) = H_{ON2}\left(f-\frac{f_{CLK}}{2}\right) = -\frac{R2}{R1};\ H_{OLP} = \frac{-R2/R1}{R6/(R5+R6)};\ H_{OBP} = -\frac{R3}{R1};\ R5 < 5k\Omega$$

Figure 19. Mode 1c: 2nd Order Filter Providing Notch, Bandpass, Lowpass

1/2 ML2110



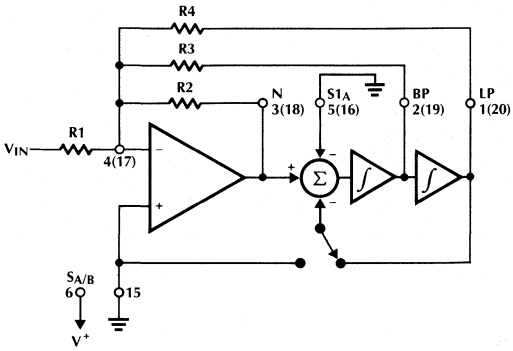
$$f_o = \frac{f_{CLK}}{100(50)};\ Q = 1+\frac{R3_A}{R3_B};\ H_{OBP} = -\frac{R2}{R1}\times Q$$

$$H_{OLP} = -\frac{R2}{R1};\ V_N = -\frac{R2}{R1}V_{IN}$$

Figure 20. Mode 1d: 2nd Order Filter Providing Bandpass and Lowpass for Qs Greater Than or Equal to 1.

OPERATION MODES (Continued)

1/2 ML2110

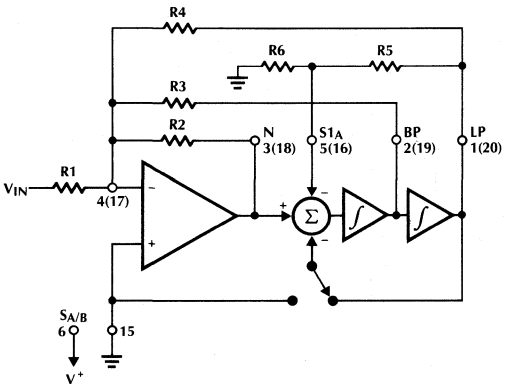


$$f_o = \frac{f_{CLK}}{100(50)}\sqrt{1+\frac{R2}{R4}};\ f_n = \frac{f_{CLK}}{100(50)};\ Q = \frac{R3}{R2}\sqrt{1+\frac{R2}{R4}};\ H_{OLP} = \frac{-R2/R1}{1+(R2/R4)}$$

$$H_{OBP} = -R3/R1;\ H_{ON1}(f\rightarrow 0) = \frac{-R2/R1}{1+(R2/R4)};\ H_{ON2}\left(f\rightarrow\frac{f_{CLK}}{2}\right) = -R2/R1$$

Figure 21. Mode 2: 2nd Order Filter Providing Notch, Bandpass, Lowpass

1/2 ML2110



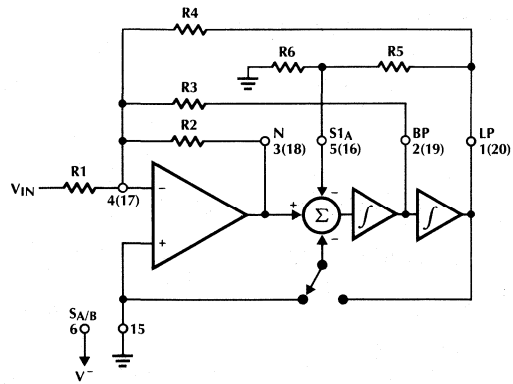
$$f_o = \frac{f_{CLK}}{100(50)}\sqrt{1+\frac{R2}{R4}+\frac{R6}{R5+R6}};\ f_n = \frac{f_{CLK}}{100(50)}\sqrt{1+\frac{R6}{R5+R6}};\ Q = \frac{R3}{R2}\sqrt{1+\frac{R2}{R4}+\frac{R6}{R5+R6}}$$

$$H_{ON1}(f\rightarrow 0) = -\frac{R2}{R1}\left\{\frac{1+R6/(R5+R6)}{1+(R2/R4)+[R6/(R5+R6)]}\right\};\ H_{ON2}\left(f\rightarrow\frac{f_{CLK}}{2}\right) = -R2/R1$$

$$H_{OBP} = -R3/R1;\ H_{OLP} = \frac{-R2/R1}{1+(R2/R4)+[R6/(R5+R6)]}$$

Figure 22. Mode 2a: 2nd Order Filter Providing Notch, Bandpass, Lowpass

1/2 ML2110



$$f_o = \frac{f_{CLK}}{100(50)}\sqrt{\frac{R2}{R4}+\frac{R6}{R5+R6}};\ f_n = \frac{f_{CLK}}{100(50)}\sqrt{\frac{R6}{R5+R6}};\ Q = \frac{R3}{R2}\sqrt{\frac{R2}{R4}+\frac{R6}{R5+R6}}$$

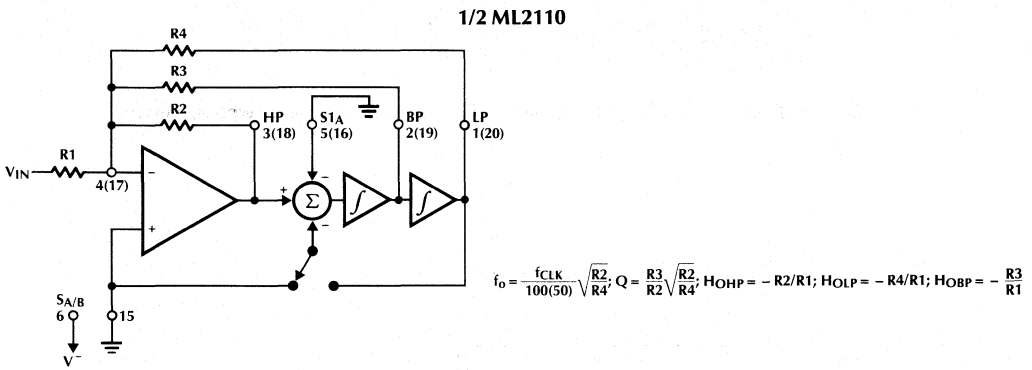
$$H_{ON1}(f\rightarrow 0) = -\frac{R2}{R1}\left\{\frac{R6/(R5+R6)}{(R2/R4)+[R6/(R5+R6)]}\right\};\ H_{ON2}\left(f\rightarrow\frac{f_{CLK}}{2}\right) = -R2/R1$$

$$H_{OBP} = -R3/R1;\ H_{OLP} = \frac{-R2/R1}{(R2/R4)+[R6/(R5+R6)]}$$

Figure 23. Mode 2b: 2nd Order Filter Providing Notch, Bandpass, Lowpass

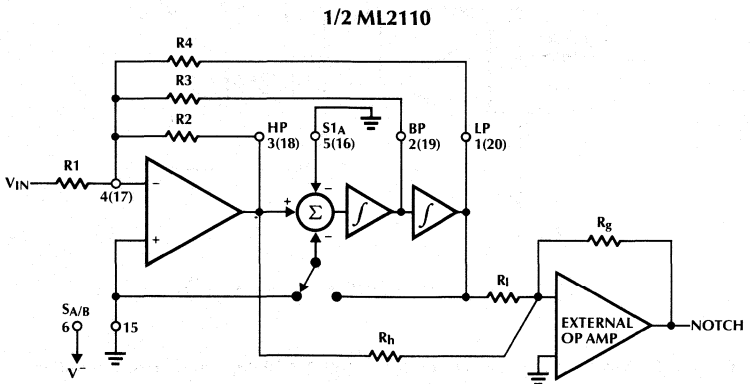
OPERATION MODES (Continued)

In mode 3, Figure 24, a single resistor ratio (R2/R4) can tune the center frequency below or above the $f_{CLK}/100$ (or $f_{CLK}/50$) ratio. Mode 3 is a state variable configuration since it provides a highpass, bandpass, lowpass output through progressive integration; notches are obtained by summing the highpass and lowpass outputs (mode 3a, Figure 25). The notch frequency can be tuned below or above the center frequency through the resistor ratio (R_h/R_l). Because of this, modes 3 and 3a are the most versatile and useful modes for cascading second order sections to obtain high order elliptic filters. Figure 33, shows the 2 sections connected in mode 3a to obtain a clock tunable 4th order sharp elliptic bandpass filter. The first notch is created by summing directly the HP and LP outputs of the first section into the inverting input of the second section op amp. The individual Q's are 29.6 and the filter maintains its shape and performance up to 20kHz center frequency, as shown in Figure 34. For this circuit an external op amp is required to obtain the 2nd notch. The dynamics of Figure 34 show that the amplitude response at each output pin does not exceed 0dB. The gain in the passband depends on the ratio of $(R_g/R_{h2}) \times (R22/R_{h1}) \times (R21/R11)$. Any gain value can be obtained by acting on the (R_g/R_{h2}) ratio of the external op amp, the remaining ratios are adjusted for optimum dynamics of the output nodes. The external op amp of Figure 33 is not always required. In Figure 35, one section in mode 3a is cascaded with the other section in mode 2b to obtain a 4th order, 1dB ripple, elliptic bandreject filter. The clock to center frequency ratio is adjusted to 200:1; this is done in order to better approximate a linear R,C notch filter. The amplitude response of the filter is shown in Figure 36 with up to 1MHz clock frequency. The 0dB bandwidth to the stop bandwidth ratio is 8/1. When the filter is centered at 1kHz, it should theoretically have a 44dB rejection with a 50Hz stop bandwidth. For a more narrow filter than the above, the unused BP output of the mode 2b section, Figure 35, has a gain exceeding unity which limits the dynamic range of the overall filter. For very selective bandpass/bandreject filters, the mode 3a approach as in Figure 25, yields better dynamic range since the external op amp helps to optimize the dynamics of the output nodes of the ML2110.



$$f_o = \frac{f_{CLK}}{100(50)}\sqrt{\frac{R2}{R4}};\ Q = \frac{R3}{R2}\sqrt{\frac{R2}{R4}};\ H_{OHP} = -R2/R1;\ H_{OLP} = -R4/R1;\ H_{OBP} = -\frac{R3}{R1}$$

Figure 24. Mode 3: 2nd Order Filter Providing Highpass, Bandpass, Lowpass

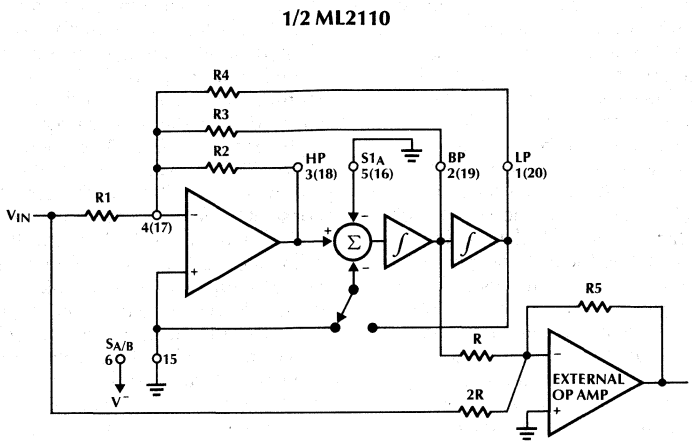


$$f_o = \frac{f_{CLK}}{100(50)}\sqrt{\frac{R2}{R4}};\ f_n = \frac{f_{CLK}}{100(50)}\sqrt{\frac{Rh}{Rl}};\ H_{OHP} = -R2/R1;\ H_{OBP} = -R3/R1,\ H_{OLP} = -R4/R1$$

$$H_{ON1}(f \to 0) = \frac{R_g}{R_l} \times \frac{R4}{R1};\ H_{ON2}\left(f \to \frac{f_{CLK}}{2}\right) = \frac{R_g}{R_h} \times \frac{R2}{R1};\ H_{ON}(f = f_o) = Q\left(\frac{R_g}{R_l} H_{OLP} - \frac{R_g}{R_h} H_{OHP}\right)$$

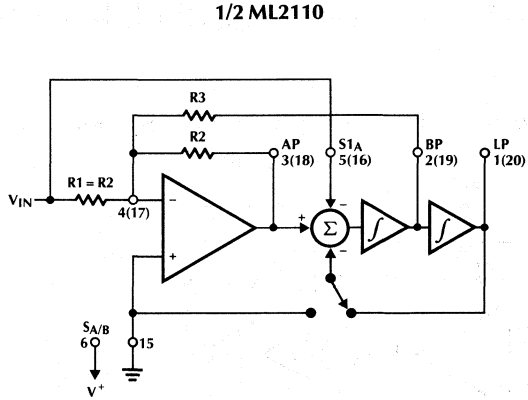
Figure 25. Mode 3a: 2nd Order Filter Providing Highpass, Bandpass, Lowpass, Notch

OPERATION MODES (Continued)



$$f_o = \frac{f_{CLK}}{100(50)}\sqrt{\frac{R2}{R4}};\ Q = \frac{R3}{R2}\sqrt{\frac{R2}{R4}};\ H_{OAP} = \frac{R5}{2R};\ H_{OHP} = -\frac{R2}{R1};\ H_{OBP} = -\frac{R3}{R1};\ H_{OLP} = -\frac{R4}{R1}$$

Figure 26. Mode 4a: 2nd Order Filter Providing Highpass, Bandpass, Lowpass, Allpass

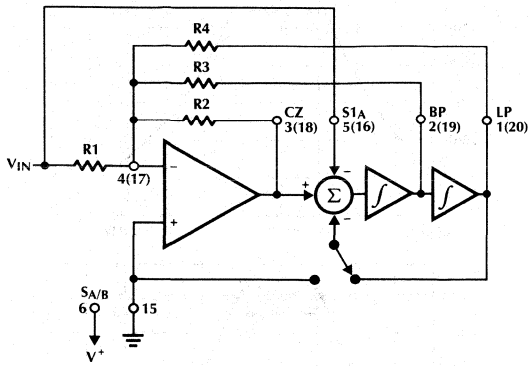


$$f_o = \frac{f_{CLK}}{100(50)};\ Q = \frac{R3}{R2};\ H_{OAP} = -\frac{R2}{R1};\ H_{OLP} = -2;\ H_{OBP} = -2\left(\frac{R3}{R2}\right)$$

Figure 27. Mode 4: 2nd Order Filter Providing Allpass, Bandpass, Lowpass

OPERATION MODES (Continued)

1/2 ML2110



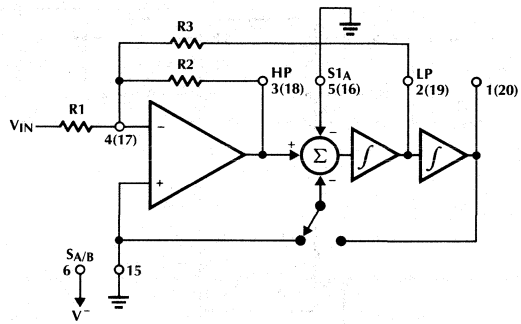
$$f_o = \frac{f_{CLK}}{100(50)}\sqrt{1+\frac{R2}{R4}};\ f_z = \frac{f_{CLK}}{100(50)}\sqrt{1-\frac{R1}{R4}};\ Q = \frac{R3}{R2}\sqrt{1+\frac{R2}{R4}}$$

$$Q_Z = \frac{R3}{R1}\sqrt{1-\frac{R1}{R4}};\ H_{OZ(f-0)} = \frac{(R4/R1)-1}{(R4/R2)+1};\ H_{OZ}\left(f-\frac{f_{CLK}}{2}\right) = \frac{R2}{R1};$$

$$H_{OBP} = \frac{R3}{R2}\left(1+\frac{R2}{R1}\right);\ H_{OLP} = \frac{1+(R2/R1)}{1+(R2/R4)}$$

Figure 28. Mode 5: 2nd Order Filter Providing Numerator Complex Zeros, Bandpass, Lowpass

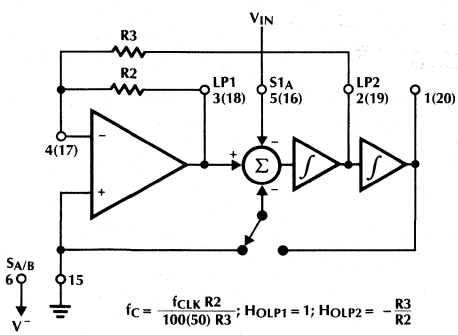
1/2 ML2110



$$f_C = \frac{f_{CLK}\ R2}{100(50)\ R3};\ H_{OLP} = -R3/R1;\ H_{OHP} = -R2/R1$$

Figure 29. Mode 6a: 1st Order Filter Providing Highpass, Lowpass

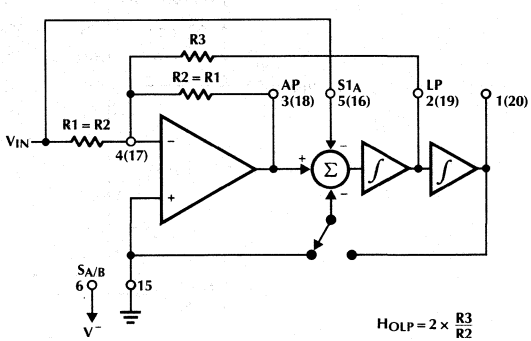
1/2 ML2110



$$f_C = \frac{f_{CLK}\ R2}{100(50)\ R3};\ H_{OLP1} = 1;\ H_{OLP2} = -\frac{R3}{R2}$$

Figure 30. Mode 6b: 1st Order Filter Providing Lowpass

1/2 ML2110

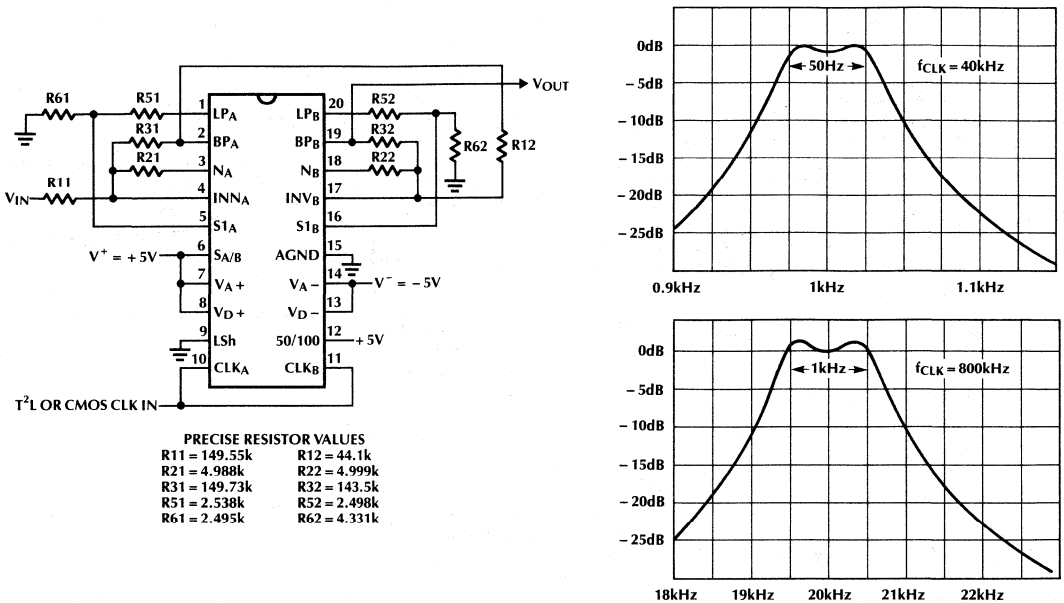


$$H_{OLP} = 2 \times \frac{R3}{R2}$$

$$f_p = \frac{f_{CLK}\ R2}{100(50)\ R3};\ f_Z = \frac{f_{CLK}\ R2}{100(50)\ R3};\ \text{GAIN AT OUTPUT} = 1\ \text{FOR}\ 0 \le f \le \frac{f_{CLK}}{2}$$

Figure 31. Mode 7: 1st Order Filter Providing Allpass, Lowpass

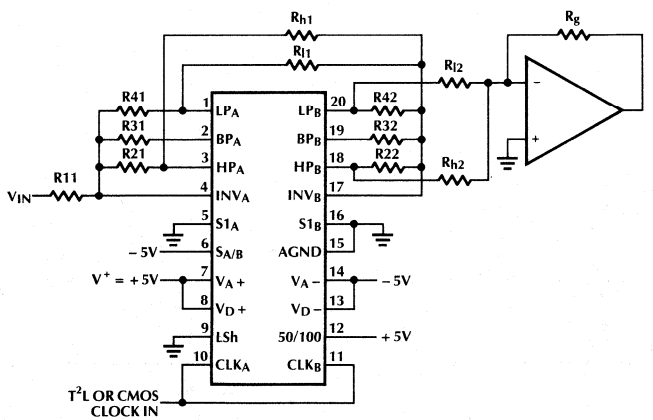
OPERATION MODES (Continued)



PRECISE RESISTOR VALUES

R11 = 149.55k	R12 = 44.1k
R21 = 4.988k	R22 = 4.999k
R31 = 149.73k	R32 = 143.5k
R51 = 2.538k	R52 = 2.498k
R61 = 2.495k	R62 = 4.331k

Figure 32. Cascading the 2 sections connected in mode 1b to obtain a clock tunable 4th order 1dB ripple bandpass Chebyshev filter with (center frequency)/(Ripple Bw) = 20/1.



RESISTOR VALUES

R11 = 155.93k	R21 = 5k	R31 = 152k	R41 = 5.27k
Rh1 = 13.2k	RI1 = 10.74k	R22 = 5.26k	R32 = 151.8k
R42 = 5k	RI2 = 6.11k	Rh2 = 5k	Rg = 37.3k

NOTE: FOR CLOCK FREQUENCIES ABOVE 700kHz A 12pF CAPACITOR ACROSS R41 AND A 20pF CAPACITOR ACROSS R42 WERE USED TO PREVENT THE PASSBAND RIPPLE FROM ANY ADDITIONAL PEAKING.

Figure 33. Combining mode 3 with mode 3a to make the 4th order BP filter of Figure 34 with improved dynamics. The gain at each node is ≤0dB for all input frequencies.

OPERATION MODES (Continued)

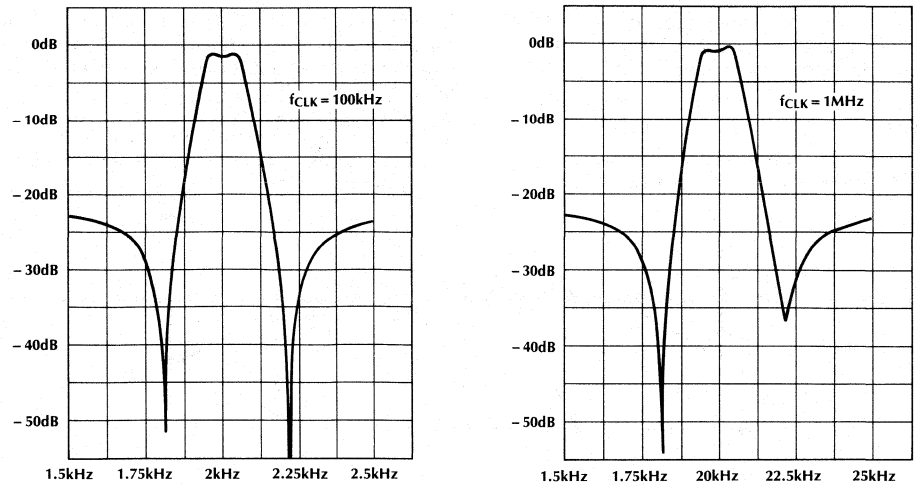


Figure 34. The BP filter of Figure 33, when swept from a 2kHz to 20kHz center frequency.

3

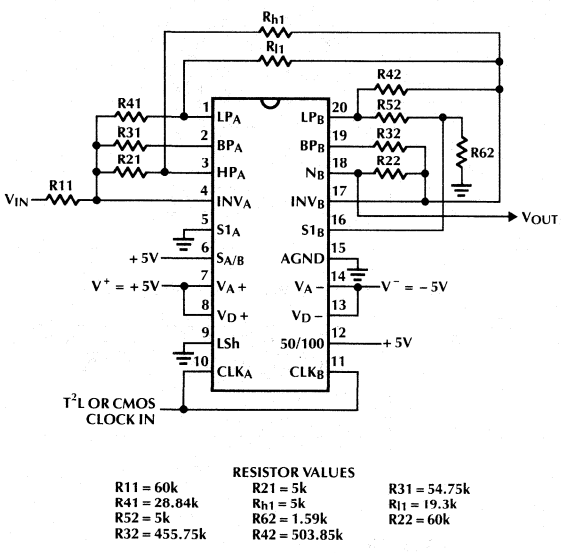


Figure 35. Combining mode 3 with mode 2b to create a 4th order BP elliptic filter with 1dB ripple and a ratio of 0db to stop bandwidth equal to 8/1.

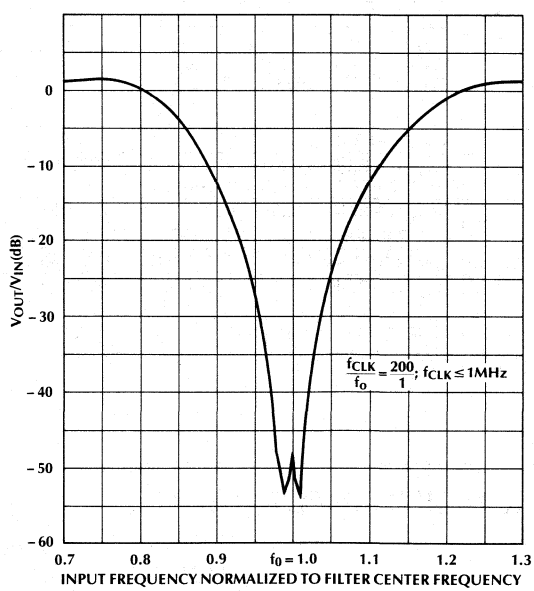


Figure 36. Amplitude Response of the Notch Filter of Figure 35.

OFFSETS

Switched capacitor integrators generally exhibit higher input offsets than discrete R,C integrators.

These offsets are mainly the charge injection of the CMOS switches into the integrating capacitors. The internal op amp offsets also add to the overall offset budget.

Figure 37 shows half of the ML2110 filter with its equivalent input offsets V_{OS1}, V_{OS2}, V_{OS3}.

The DC offset at the filter bandpass output is always equal to V_{OS3}. The DC offsets at the remaining two outputs (Notch and LP) depend on the mode of operation and external resistor ratios. Table 3 illustrates this.

It is important to know the value of the DC output offsets, especially when the filter handles input signals with large dynamic range. As a rule of thumb, the output DC offsets increase when:

1. The Q's decrease
2. The ratio (f_{CLK}/f_o) increases beyond 100:1. This is done by decreasing either the (R2/R4) or the R6/(R5 + R6) resistor ratios.

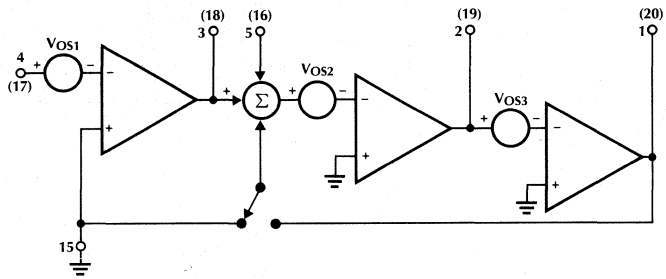


Figure 37. Equivalent Input Offsets of 1/2 ML2110 Filter

Table 3

MODE	V_{OSN} PIN 3 (18)	V_{OSBP} PIN 2 (19)	V_{OSLP} PIN 1 (20)
1,4	$V_{OS1}[(1/Q)+1+\lVert H_{OLP}\rVert]-V_{OS3}/Q$	V_{OS3}	$V_{OSN}-V_{OS2}$
1a	$V_{OS1}[1+(1/Q)]-V_{OS3}/Q$	V_{OS3}	$V_{OSN}-V_{OS2}$
1b	$V_{OS1}[(1/Q)+1+R2/R1]-V_{OS3}/Q$	V_{OS3}	$\sim(V_{OSN}-V_{OS2})(1+R5/R6)$
1c	$V_{OS1}[(1/Q)+1+R2/R1]-V_{OS3}/Q$	V_{OS3}	$\sim(V_{OSN}-V_{OS2})\frac{(R5+R6)}{(R5+2R6)}$
1d	$V_{OS1}[1+R2/R1]$	V_{OS3}	$V_{OSN}-V_{OS2}-V_{OS3}/Q$
2, 5	$[V_{OS1}(1+R2/R1+R2/R3+R2/R4)-V_{OS3}(R2/R3)]\times[R4/(R2+R4)]+V_{OS2}[R2/(R2+R4)]$	V_{OS3}	$V_{OSN}-V_{OS2}$
2a	$[V_{OS1}(1+R2/R1+R2/R3+R2/R4)-V_{OS3}(R2/R3)]\times\left[\frac{R4(1+k)}{R2+R4(1+k)}\right]+V_{OS2}\left[\frac{R2}{R2+R4(1+k)}\right];k=\frac{R6}{R5+R6}$	V_{OS3}	$\sim(V_{OSN}-V_{OS2})\frac{(R5+R6)}{(R5+2R6)}$
2b	$[V_{OS1}(1+R2/R1+R2/R3+R2/R4)-V_{OS3}(R2/R3)]\times\left[\frac{R4k}{R2+R4k}\right]+V_{OS2}\left[\frac{R2}{R2+R4k}\right];k=\frac{R6}{R5+R6}$	V_{OS3}	$\sim(V_{OSN}-V_{OS2})(1+R5/R6)$
3, 4a	V_{OS2}	V_{OS3}	$V_{OS1}\left[1+\frac{R4}{R1}+\frac{R4}{R2}+\frac{R4}{R3}\right]-V_{OS2}\left(\frac{R4}{R2}\right)-V_{OS3}\left(\frac{R4}{R3}\right)$

ORDERING INFORMATION

PART NO.	TEMPERATURE RANGE	PACKAGE
ML2110BCP	0°C to 70°C	Molded DIP
ML2110CCP	0°C to 70°C	Molded DIP
ML2110BCS	0°C to 70°C	Molded SOIC
ML2110CCS	0°C to 70°C	Molded SOIC
ML2110BIJ	−40°C to +85°C	Hermetic DIP
ML2110CIJ	−40°C to +85°C	Hermetic DIP
ML2110BMJ	−55°C to +125°C	Hermetic DIP
ML2110CMJ	−55°C to +125°C	Hermetic DIP

Universal Hi-Frequency Dual Filter

GENERAL DESCRIPTION

The ML2111 consists of two independent switched capacitor filters that operate up to 150kHz. These filters perform second order functions, such as lowpass, bandpass, highpass, notch and allpass. All filter configurations, including Butterworth, Bessel, Cauer and Chebyshev can be formed.

The center frequency of these filters are tuned by an external clock or the external clock and a resistor ratio.

The ML2111 frequency range up to 150kHz is specified with ±5.0V ± 10% power supplies. Using a single 5.0V ± 10% power supply the frequency range is up to 100kHz.

These filters are ideal where center frequency accuracy and high Qs are needed.

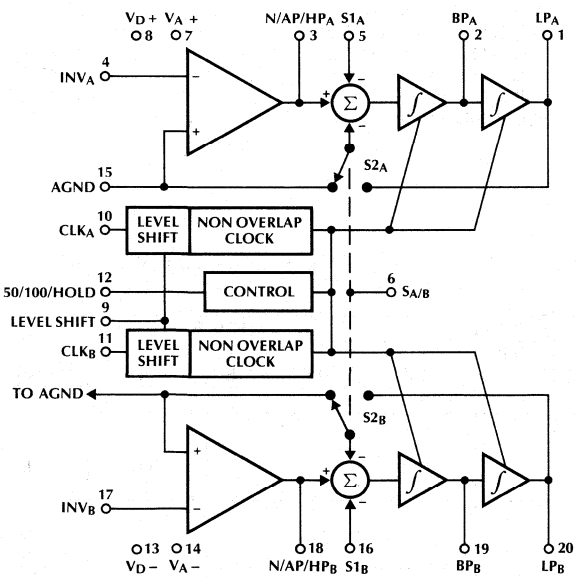
The ML2111 is a pin compatible superior replacement for MF10, LMF100, and LTC1060 filters.

FEATURES

- Guaranteed frequency range to 150kHz
- Center frequency × Q product ≤5MHz
- Separate highpass, notch, allpass, bandpass, and lowpass outputs
- Center frequency accuracy ±0.4% or ±0.8% max
- Q accuracy ±4%, or ±8% max
- Clock inputs TTL or CMOS compatible
- Single 5V (±2.25V) or ±5V ±10% supply operation guaranteed
- 0°C to +70°C, −40°C to +85°C, −55°C to +125°C operating temperature range
- Standard 0.3" 20-pin DIP or 20-pin small outline (SOIC) package

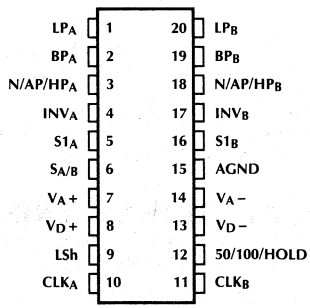
3

BLOCK DIAGRAM



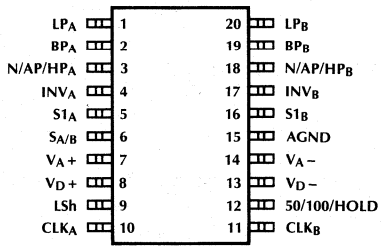
PIN CONNECTIONS

ML2111
20-PIN DIP



TOP VIEW

ML2111
20-PIN SOIC



TOP VIEW

PIN DESCRIPTION

PIN NO.	NAME	FUNCTION
1	LP_A	Lowpass output for biquad A.
2	BP_A	Bandpass output for biquad A.
3	$N/AP/HP_A$	Notch/allpass/highpass output for biquad A.
4	INV_A	Inverting input of the summing op amp for biquad A.
5	$S1_A$	Auxiliary signal input pin used in modes 1a, 1d, 4, 5, and 6b.
6	$S_{A/B}$	Controls S2 input function.
7	V_A+	Positive analog supply.
8	V_D+	Positive digital supply.
9	LSh	Reference point for clock input levels. Logic threshold typically 1.4V above LSh voltage.
10	CLK_A	Clock input for biquad A.
11	CLK_B	Clock input for biquad B.
12	50/100/HOLD	Input pin to control the clock to center frequency ratio of 50:1 or 100:1, or stops the clock to hold the last sample of the bandpass or lowpass outputs.
13	V_D-	Negative digital supply.
14	V_A-	Negative analog supply.
15	AGND	Analog ground.
16	$S1_B$	Auxiliary signal input used in modes 1a, 1d, 4, 5, and 6b.
17	INV_B	Inverting input of the summing op amp for biquad B.
18	$N/AP/HP_B$	Notch/allpass/highpass output for biquad B.
19	BP_B	Bandpass output for biquad B.
20	LP_B	Lowpass output for biquad B.

ABSOLUTE MAXIMUM RATINGS
(Note 1)

Supply Voltage
$|V_A+|, |V_D+|-|V_A-|, |V_D-|$ 13V
V_A+, V_D+ to LSh 13V
Inputs ..... $|V_A+, V_D+|+0.3V$ to $|V_A-, V_D-|-0.3V$
Outputs ..... $|V_A+, V_D+|+0.3V$ to $|V_A-, V_D-|-0.3V$
$|V_A+|$ to $|V_D+|$ ..... ±0.3V
Power Dissipation 750mW
Storage Temperature Range ..... −65°C to 150°C
Lead Temperature (soldering, 10 sec) ..... 300°C

OPERATING CONDITIONS

Temperature Range (Note 2)
ML2111BCP, ML2111CCP,
ML2111BCS, ML2111CCS ..... 0°C to 70°C
ML2111BIJ, ML2111CIJ ..... −40°C to +85°C
ML2111BMJ, ML2111CMJ ..... −55°C to +125°C
Supply Voltage Range ..... ±2.25V to ±6.0V

ELECTRICAL CHARACTERISTICS

Unless otherwise specified $T_A = T_{MIN}$ to T_{MAX}, $V_A+ = V_D+ = 5V \pm 10\%$, $V_A- = V_D- = -5V \pm 10\%$, $C_L = 25pF$, $V_{IN} = 1.41V_{PK}$ (1.00 V_{RMS}), Clock Duty Cycle 45% to 55%.

PARAMETER	NOTES	CONDITIONS	ML2111B MIN	ML2111B TYP NOTE 3	ML2111B MAX	ML2111C MIN	ML2111C TYP NOTE 3	ML2111C MAX	UNITS
Filter									
f_o, Center Frequency Maximum	5, 6	Figure 15 (Mode 1) $V_{IN} = 1V_{PK}$ (.707 V_{RMS}) $Q \le 50$, Q Accuracy $\le \pm 25\%$ $Q \le 20$, Q Accuracy $\le \pm 15\%$			100 150			100 150	kHz kHz
f_o, Center Frequency Minimum	5, 6	Figure 15 (Mode 1) $Q \le 50$, Q Accuracy $\le \pm 30\%$ $Q \le 20$, Q Accuracy $\le \pm 15\%$	25 25			25 25			Hz Hz
f_o, Temperature Coefficient		$f_{CLK} < 5MHz$		−10			−10		ppm/°C
Clock to Center Frequency Ratio	 4 4	Q = 10 Figure 15 (Mode 1) 50:1, $f_{CLK} = 5MHz$ 100:1, $f_{CLK} = 5MHz$	 49.65 99.60	 49.85 100	 50.05 100.40	 49.45 99.20	 49.85 100	 50.25 100.80	

ELECTRICAL CHARACTERISTICS (Continued)

Unless otherwise specified $T_A = T_{MIN}$ to T_{MAX}, $V_{A+} = V_{D+} = 5V \pm 10\%$, $V_{A-} = V_{D-} = -5V \pm 10\%$, $C_L = 25pF$, $V_{IN} = 1.41V_{PK}$ (1.00 V_{RMS}), Clock Duty Cycle 50% (Note 8).

PARAMETER	NOTES	CONDITIONS	ML2111B MIN	ML2111B TYP NOTE 3	ML2111B MAX	ML2111C MIN	ML2111C TYP NOTE 3	ML2111C MAX	UNITS
Filter (Continued)									
Clock Frequency	5	Q ≤ 20, Q Accuracy ≤ ±15%	2.5k		7.5M	2.5k		7.5M	Hz
Clock Feedthrough	5	$f_{CLK} \leq 5MHz$		10	20		10	20	mV(p-p)
Q Accuracy	4	$f_{CLK} = 5MHz$, Q = 10, Figure 15 (Mode 1) 50:1			±3			±5	%
		100:1			±4			±8	%
Q Temperature Coefficient	5	$f_{CLK} < 5MHz$, Q = 10		20			20		ppm/°C
DC Offset		50:1, $f_{CLK} = 5MHz$							
V_{OS} 2, 3	4	$S_{A/B}$ High		7	40		7	60	mV
V_{OS} 2, 3	4	$S_{A/B}$ Low		7	40		7	60	mV
DC Offset		100:1, $f_{CLK} = 5MHz$							
V_{OS} 2, 3	4	$S_{A/B}$ High		14	60		14	100	mV
V_{OS} 2, 3	4	$S_{A/B}$ Low		14	60		14	100	mV
Gain Accuracy									
DC Lowpass	4	R1 = 20k, R2 = 2k, R3 = 20k		0.01	2		0.01	2	%
Bandpass at f_o	4	100:1, f_o = 50kHz, Q = 10		1	4		1	6	%
DC Notch Output	5			0.02	2		0.02	2	%
Noise	7	Figure 15 (Mode 1) Q = 1, R1 = R2 = R3 = 2k							
		Bandpass, 100kHz, 50:1		103			103		μV_{RMS}
		50kHz, 100:1		121			121		μV_{RMS}
		Lowpass, 100kHz, 50:1		120			120		μV_{RMS}
		50kHz, 100:1		150			150		μV_{RMS}
		Notch, 100kHz, 50:1		115			115		μV_{RMS}
		50kHz, 100:1		135			135		μV_{RMS}
		Figure 15 (Mode 1) Q = 10, R1 = R3 = 20k, R2 = 2k							
		Bandpass, 100kHz, 50:1		262			262		μV_{RMS}
		50kHz, 100:1		333			333		μV_{RMS}
		Lowpass, 100kHz, 50:1		268			268		μV_{RMS}
		(R1 = 2k) 50kHz, 100:1		342			342		μV_{RMS}
		Notch, 100kHz, 50:1		64			64		μV_{RMS}
		(R1 = 2k) 50kHz, 100:1		72			72		μV_{RMS}
Crosstalk		$f_{CLK} = 5MHz$, $f_o = 100kHz$		−50			−50		dB
Filter, $V_{A+} = V_{D+} = 2.25V$, $V_{A-} = V_{D-} = -2.25V$, $V_{IN} = 0.707\ V_{PK}$ (0.5 V_{RMS})									
f_o, Center Frequency Maximum	5	Figure 15 (Mode 1)							
		Q ≤ 50, Q Accuracy ≤ ±30%			75			75	kHz
		Q ≤ 20, Q Accuracy ≤ ±15%			100			100	kHz
f_o, Center Frequency Minimum	5	Figure 15 (Mode 1)							
		Q ≤ 50, Q Accuracy ≤ ±30%	25			25			Hz
		Q ≤ 20, Q Accuracy ≤ ±15%	25			25			Hz
Clock to Center Frequency Ratio		Q = 10, Figure 15 (Mode 1)							
	4	50:1, $f_{CLK} = 2.5MHz$	49.65	49.85	50.05	49.45	49.85	50.25	
	5	100:1, $f_{CLK} = 2.5MHz$	99.60	100	100.40	99.20	100	100.80	
Clock Frequency	5	Q ≤ 20, Q Accuracy ≤ ±15%	2.5k		5M	2.5k		5M	Hz
Q Accuracy	4	$f_{CLK} = 2.5MHz$, Q = 10, 50:1			±4			±8	%
		Figure 15 (Mode 1) 100:1		±3			±6		%

ELECTRICAL CHARACTERISTICS (Continued)

Unless otherwise specified $T_A = T_{MIN}$ to T_{MAX}, $V_{A+} = V_{D+} = 5V \pm 10\%$, $V_{A-} = V_{D-} = -5V \pm 10\%$, $C_L = 25pF$, $V_{IN} = 1.41V_{PK}$ (1.00 V_{RMS}), Clock Duty Cycle 50% (Note 8).

PARAMETER	NOTES	CONDITIONS	ML2111B MIN	ML2111B TYP NOTE 3	ML2111B MAX	ML2111C MIN	ML2111C TYP NOTE 3	ML2111C MAX	UNITS
Filter, $V_{A+} = V_{D+} = 2.25V$, $V_{A-} = V_{D-} = -2.25V$, $V_{IN} = 0.707\ V_{PK}$ (0.5 V_{RMS}) (Continued)									
Noise	7	Figure 15 (Mode 1) Q – 1, R1 – R2 – R3 – 2k							
		Bandpass, 100kHz, 50:1		105			105		μV_{RMS}
		50kHz, 100:1		123			123		μV_{RMS}
		Lowpass, 100kHz, 50:1		122			122		μV_{RMS}
		50kHz, 100:1		152			152		μV_{RMS}
		Notch, 100kHz, 50:1		117			117		μV_{RMS}
		50kHz, 100:1		138			138		μV_{RMS}
		Figure 15 (Mode 1) Q = 10, R1 = R3 = 20k, R2 = 2k							
		Bandpass, 100kHz, 50:1		265			265		μV_{RMS}
		50kHz, 100:1		335			335		μV_{RMS}
		Lowpass, 100kHz, 50:1		270			270		μV_{RMS}
		(R1 = 2k) 50kHz, 100:1		245			245		μV_{RMS}
		Notch, 100kHz, 50:1		65			65		μV_{RMS}
		(R1 = 2k) 50kHz, 100:1		73			73		μV_{RMS}
Operational Amplifiers and Power Supply									
V_{OS} DC Offset	4			2	15		2	15	mV
DC Open Loop Gain		$R_L = 1k$		95			95		dB
Gain Bandwidth Product				2.4			2.4		MHz
Slew Rate				2.0			2.0		V/μs
Output Voltage Swing (Clipping Level)	5	$R_L = 2k$, |V| from V_{A+} or V_{A-}		0.5	1.2		0.5	1.2	V
Output Short Circuit Current		Source		50			50		mA
		Sink		25			25		mA
Power Supply And Clock									
Supply Current	4	$f_{CLK} = 5MHz$							
$(I_{A+}) + (I_{D+})$				13	22		13	22	mA
$(I_{A-}) + (I_{D-})$				12	21		12	21	mA
I_{LSH}				0.5	1		0.5	1	mA
V_{CLK} Input Threshold	4	$f_{CLK} = 5MHz$ Low			0.6			0.6	V
		High	3.0			3.0			V
	5	$f_{CLK} < 2.5MHz$ Low			0.8			0.8	V
		High	2.0			2.0			V
CLKA, CLKB Pulse Width	5, 8	CLK High or $\|V_{D+}\| - \|V_{D-}\| \geq 4.5V$	100			100			ns
		CLK Low $\|V_{D+}\| - \|V_{D-}\| \geq 9.0V$	66			66			ns

Note 1: Absolute maximum ratings are limits beyond which the life of the integrated circuit may be impaired. All voltages unless otherwise specified are measured with respect to ground.

Note 2: –55°C to +125°C operating temperature range devices are 100% tested at temperature extremes with worst-case test conditions. 0°C to 70°C and –40°C to +85°C operating temperature range devices are 100% tested with temperature limits guaranteed by 100% testing, sampling, or by correlation with worst-case test conditions.

Note 3: Typicals are parametric norm at 25°C.

Note 4: Parameter guaranteed and 100% production tested.

Note 5: Parameter guaranteed. Parameters not 100% tested are not in outgoing quality level calculation.

Note 6: Center frequency is defined as the peak of the bandpass output.

Note 7: The noise is measured with the HP8903A audio analyzer with a bandwidth of 750kHz which is 7.5 times the f_O at 50:1 and 15 times the f_O at 100:1.

Note 8: For best performance with $f_{CLK} > 2.5MHz$ use a 50% duty cycle.

FUNCTIONAL DESCRIPTION

POWER SUPPLIES

The analog (V_A+) and digital (V_D+) supply voltage pins should be tied together and bypassed to AGND with at least a 0.1μF and a 0.01μF disc ceramic capacitor. If high digital noise exists, the supply pins can be bypassed separately. The ML2111 positive analog and positive digital supply pins are internally connected by the IC substrate and should be biased from the same DC source. The ML2111 negative analog and negative digital supply are not connected internally, however they should be biased from the same DC source and bypassed with at least a 0.1μF and a 0.01μF disc ceramic capacitor.

The ML2111 operates with a single supply from 4V to 12V and with split supplies from ±2.0V to ±6V.

CLOCK INPUT PINS AND LEVEL SHIFT

With dual supplies equal to or higher than ±4.0V, the level shift (LSh) pin 9 can be connected to the same potential as the AGND or V_A- pin. With single supply operation, the negative supply pins and the LSh pin should be tied to the system ground. The AGND, pin 15, should be biased at 1/2 supplies. Under these conditions, the clock levels are TTL or CMOS. The input clock pins (10, 11) share the same level shift pin.

50/100/HOLD (Pin 12)

By tying pin 12 to (V_A+, V_D+) the filter operates in the 50:1 mode. By tying pin 12 to 1/2 of the voltage supplies (AGND potential), the ML2111 operates in the 100:1 mode. The range of pin 12 without affecting the 100:1 filter operation with total supply voltage of +5V is 2.5±0.5V; +10V is 5V±0.5V. When pin 12 is tied to the negative supply pin, the filter operation is stopped and the bandpass and lowpass outputs act as an S/H circuit holding the last sample.

$S1_A$, $S1_B$, (Pins 5 and 16)

These are the auxiliary voltage signal input pins always connected to one of the negative inputs of the voltage summer (the other negative input switches between LPo and AGND according to control pin $S_{A/B}$ (pin 6). The positive input of the voltage summer is always connected to N/AP/HP pin of the corresponding section. They should be driven with a source impedance below 5k for $f_{CLK} < 2.5$MHz and 1k to 2k for $f_{CLK} > 2.5$MHz. The $S1_A$, $S1_B$ pins can be used to alter the clock to center frequency ratio (f_{CLK}/f_o) of the filter (see modes 1b, 1c, 2a, 2b) or to feedforward the input signal for allpass filter configurations (see modes 4 and 5). They can also be used, as in mode 1d to avoid the finite phase shift through the input amplifier, hence allowing higher operating frequencies. When these pins are not used, they should be tied to the AGND pin.

$S_{A/B}$ (Pin 6)

When $S_{A/B}$ is high, the S2 negative input of the voltage summer is tied to the lowpass output. When the $S_{A/B}$ pin is connected to the negative supply, the S2 input switches to ground.

AGND (Pin 15)

AGND is connected to the system ground for dual supply operation. When operating with a single positive supply, the analog ground pin should be tied to 1/2 of the supply and bypassed with a 0.1μF and a 0.01μF disc ceramic capacitor. The positive inputs of the internal op amps and the reference point of the internal switches are connected to the AGND pin.

f_{CLK}/f_o RATIO

The ML2111 is a sampled data filter and approximates continuous time filters. The filter deviates from its ideal continuous filter model when the (f_{CLK}/f_o) ratio decreases and when the Qs are low.

$f_o \times Q$ PRODUCT RATIO

The $f_o \times Q$ product of the ML2111 depends on the clock frequency and the mode of operation. For clock frequencies below 5MHz, in mode 1 and its derivatives, the $f_o \times Q$ product is mainly limited by the desired f_o and Q accuracy. For the same clock frequency and for the same Q value the $f_o \times Q$ product can be further increased if the clock to center frequency ratio is lowered below 50:1.

Mode 3, Figure 23, and the modes of operation where R4 is finite, are "slower" than the basic mode 1. The resistor R4 places the input op amp inside the resonant loop. The finite GBW of this op amp creates an additional phase shift and enhances the Q value at high clock frequencies.

OUTPUT NOISE

The wideband RMS noise of the ML2111 outputs is nearly independent from the clock frequency provided that the clock itself does not become part of the noise. The noise at the BP and LP outputs increases for high Qs.

TYPICAL PERFORMANCE CURVES

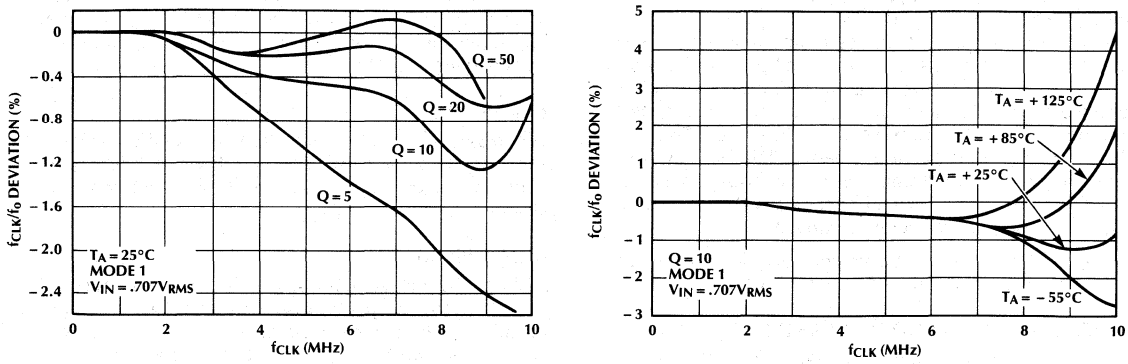


Figure 1A. f_{CLK}/f_o vs. f_{CLK} (50:1, $V_S = \pm 5V$)

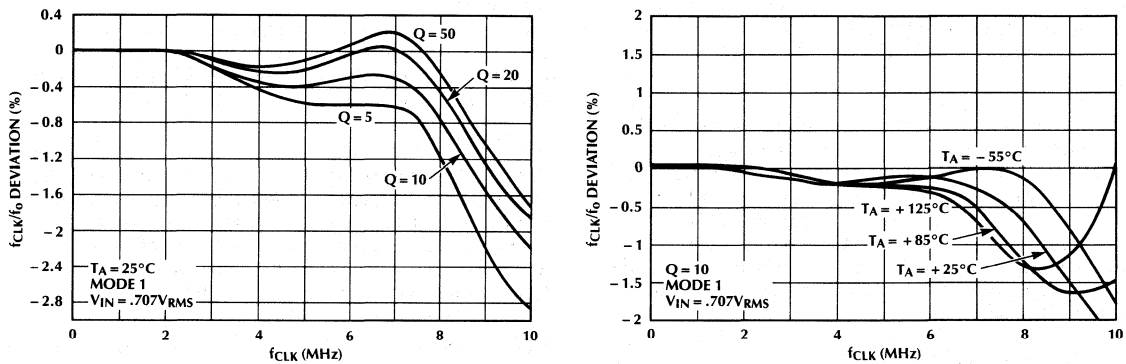


Figure 1B. f_{CLK}/f_o vs. f_{CLK} (100:1, $V_S = \pm 5V$)

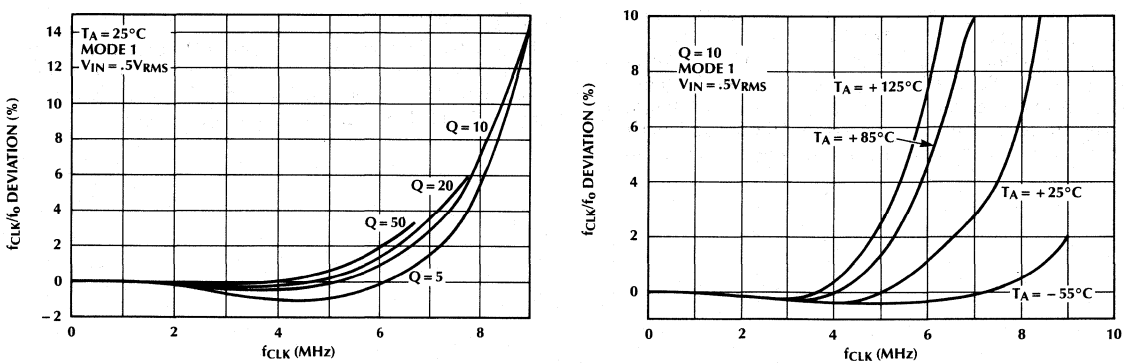
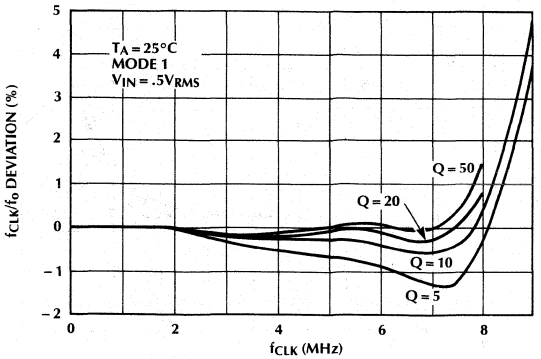


Figure 1C. f_{CLK}/f_o vs. f_{CLK} (50:1, $V_S = \pm 2.5V$)

TYPICAL PERFORMANCE CURVES (Continued)



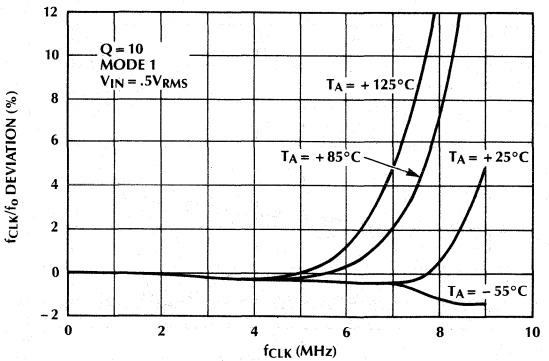


Figure 1D. f_{CLK}/f_o vs. f_{CLK} (100:1, $V_S = \pm 2.5V$)

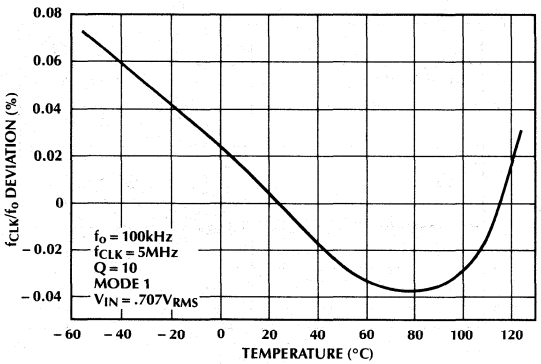


Figure 2A. f_{CLK}/f_o Deviation vs. Temperature (50:1, $V_S = \pm 5V$)

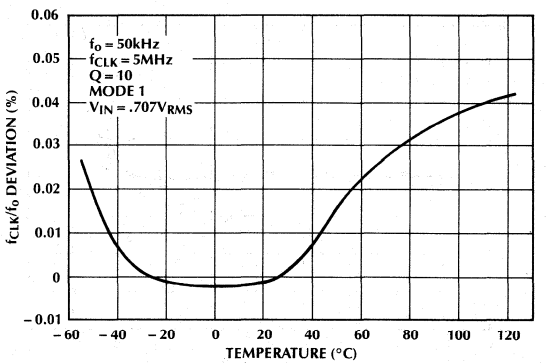


Figure 2B. f_{CLK}/f_o Deviation vs. Temperature (100:1, $V_S = \pm 5V$)

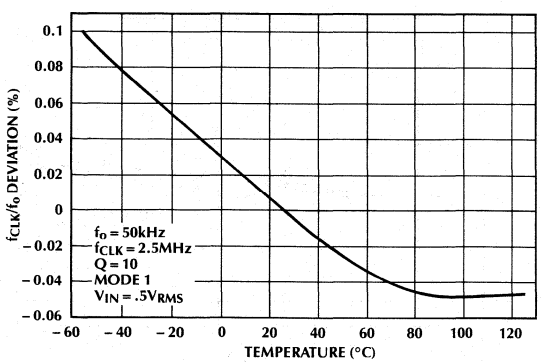


Figure 2C. f_{CLK}/f_o Deviation vs. Temperature (50:1, $V_S = \pm 2.5V$)

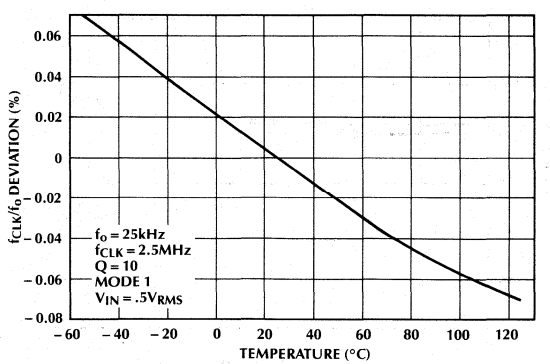
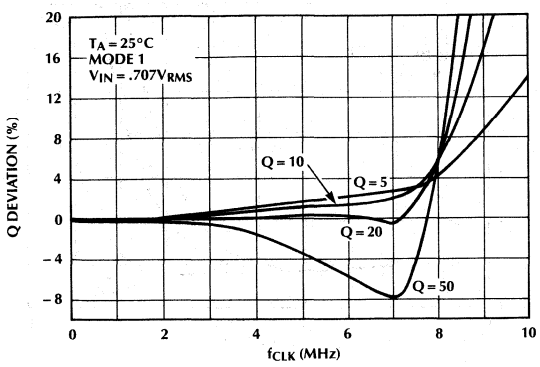


Figure 2D. f_{CLK}/f_o Deviation vs. Temperature (100:1, $V_S = \pm 2.5V$)

TYPICAL PERFORMANCE CURVES (Continued)



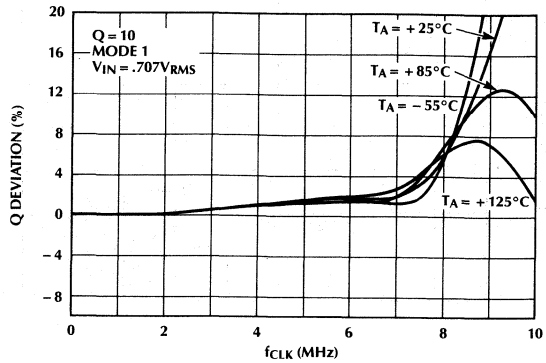
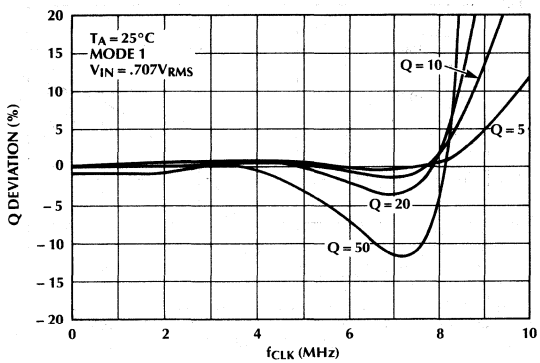


Figure 2E. Q Error vs. f_{CLK} (50:1, $V_S = \pm 5V$)



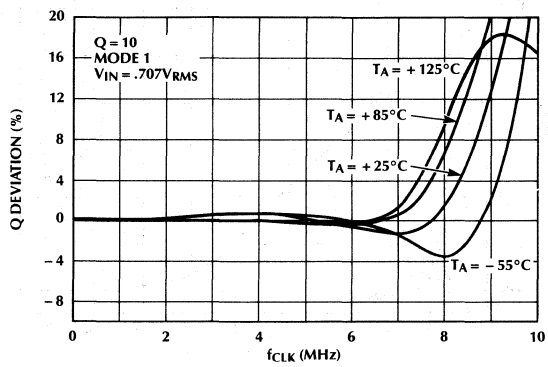
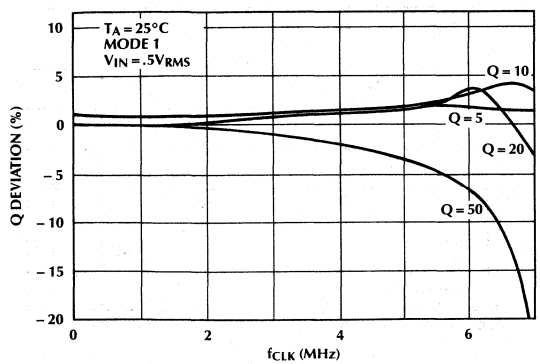


Figure 2F. Q Error vs. f_{CLK} (100:1, $V_S = \pm 5V$)



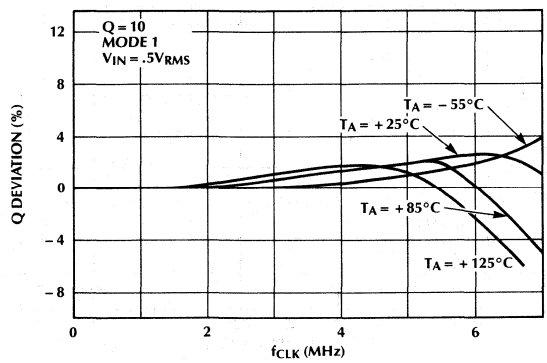
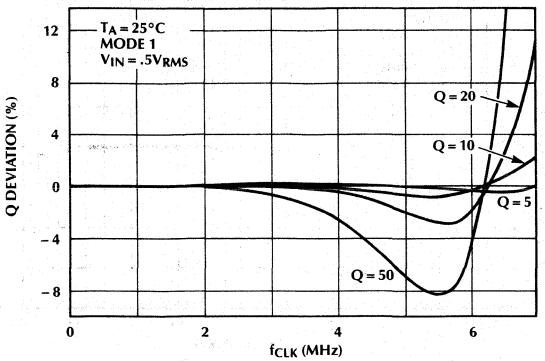


Figure 2G. Q Error vs. f_{CLK} (50:1, $V_S = \pm 2.5V$)

TYPICAL PERFORMANCE CURVES (Continued)



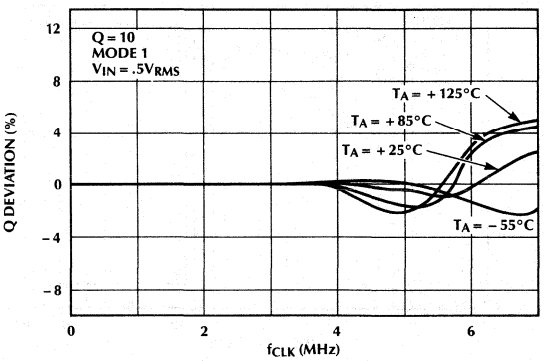


Figure 2H. Q Error vs. f_{CLK} (100:1, $V_S = \pm 2.5V$)

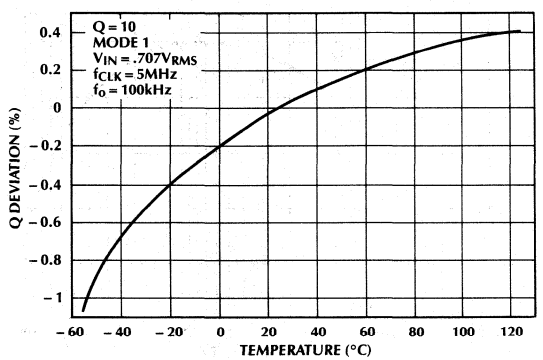


Figure 3A. Q Deviation vs. Temperature (50:1, $V_S = \pm 5V$)

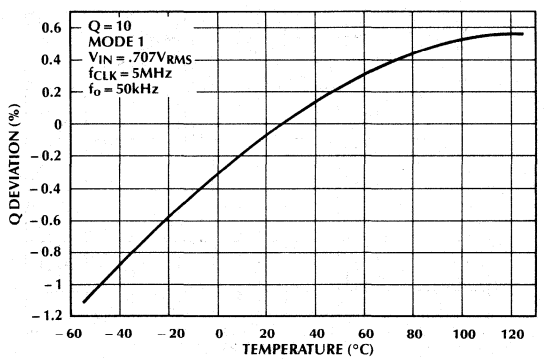


Figure 3B. Q Deviation vs. Temperature (100:1, $V_S = \pm 5V$)

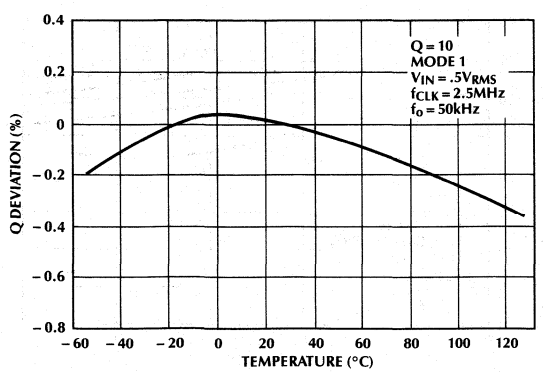


Figure 3C. Q Deviation vs. Temperature (50:1, $V_S = \pm 2.5V$)

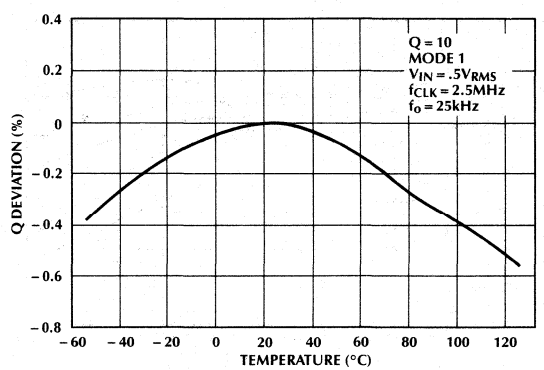


Figure 3D. Q Deviation vs. Temperature (100:1, $V_S = \pm 2.5V$)

TYPICAL PERFORMANCE CURVES (Continued)

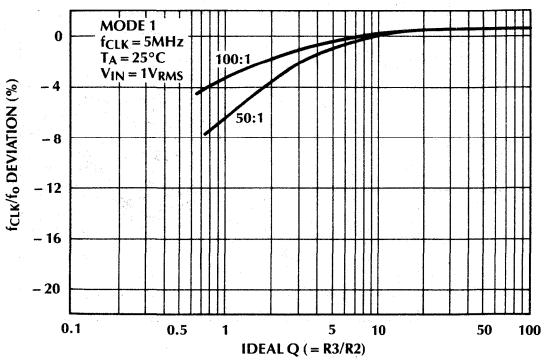


Figure 4A. f_{CLK}/f_o Deviation vs. Q (V_S = ±5V)

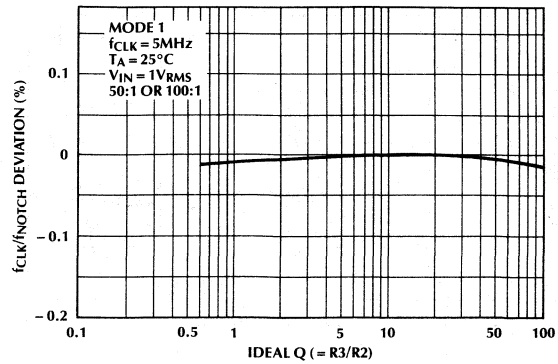


Figure 4B. f_{CLK}/f_{NOTCH} Deviation vs. Q (V_S = ±5V)

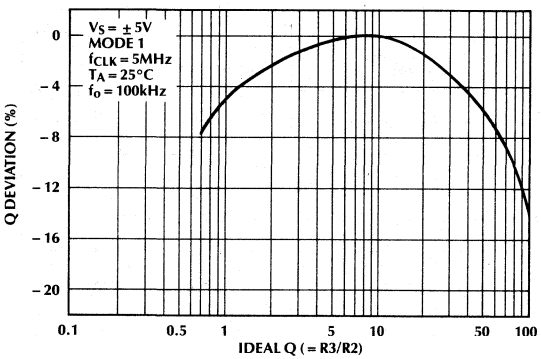


Figure 5A. Q Deviation vs. Q (50:1, V_S = ±5V)

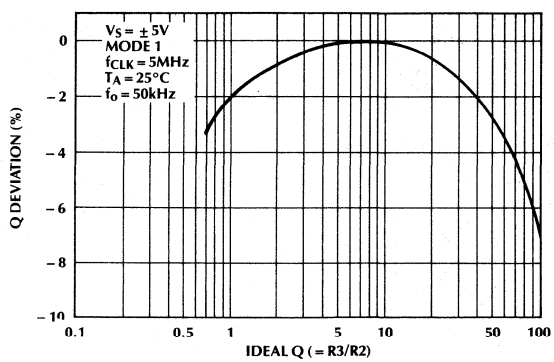


Figure 5B. Q Deviation vs. Q (100:1, V_S = ±5V)

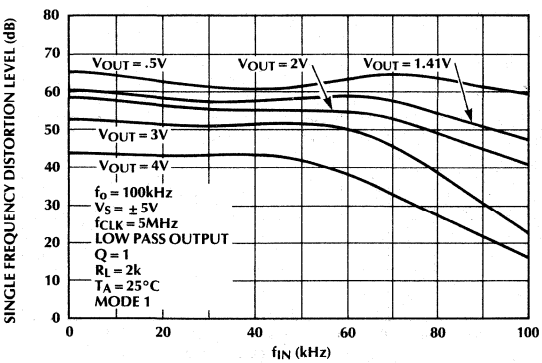


Figure 6A. Distortion vs. f_{IN} (50:1, V_S = ±5V)

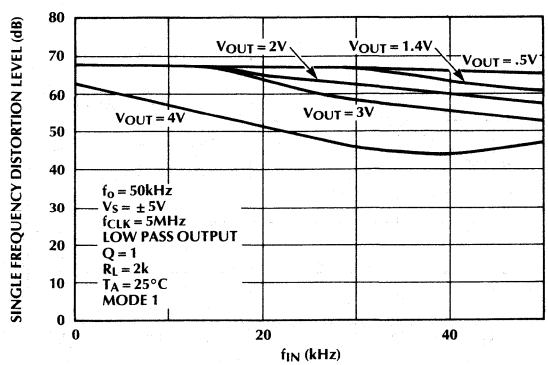


Figure 6B. Distortion vs. f_{IN} (100:1, V_S = ±5V)

TYPICAL PERFORMANCE CURVES (Continued)

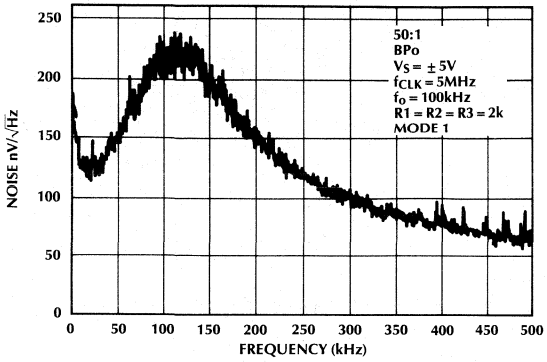


Figure 7A. Noise Spectrum Density (Q = 1)

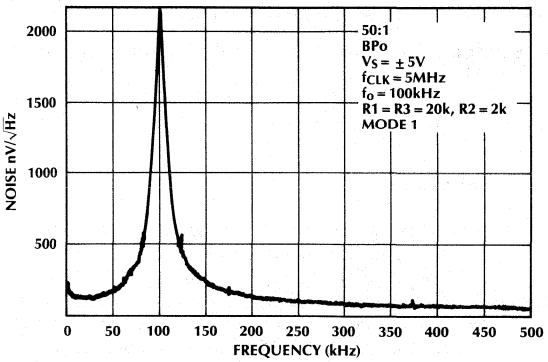


Figure 7B. Noise Spectrum Density (Q = 10)

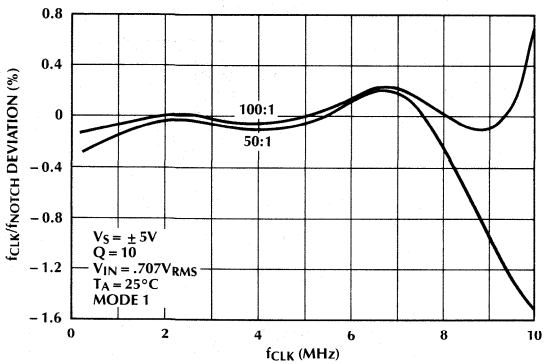


Figure 8. f_{CLK}/f_{NOTCH} vs. f_{CLK}

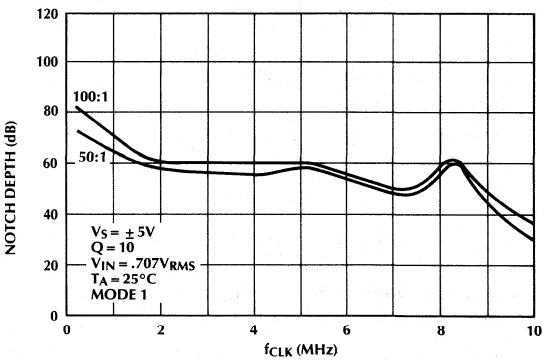


Figure 9. Notch Depth vs. f_{CLK}

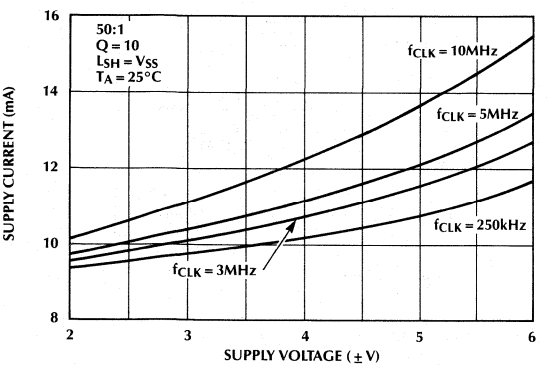


Figure 10. Supply Current vs. Supply Voltage

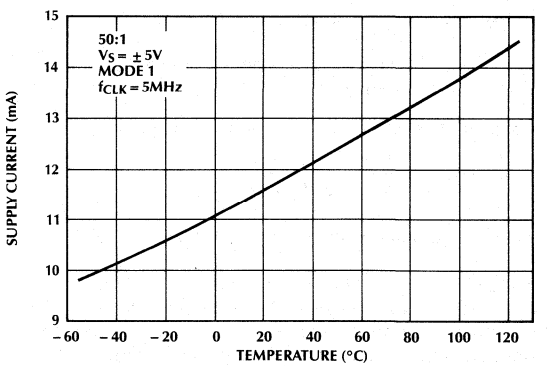


Figure 11. Supply Current vs. Temperature

FILTER FUNCTION DEFINITIONS

Each filter of the ML2111 with an external clock and resistors approximates 2nd order filter functions. These are tabulated below in the frequency domain.

1. **Bandpass function:** available at the bandpass output pins (2, 19), Figure 12.

$$G(s) = H_{OBP}\frac{s\omega_o/Q}{s^2 + (s\omega_o/Q) + \omega_o^2}$$

H_{OBP} = Gain at $\omega = \omega_o$

$f_o = \omega_o/2\pi$; f_o is the center frequency of the complex pole pair. f_o is measured as the peak frequency of the bandpass output.

Q = Quality factor of the complex pole pair. It is the ratio of f_o to the −3dB bandwidth of the 2nd order bandpass function. The Q is always measured at the filter BP output.

2. **Lowpass function:** available at the LP output pins (1, 20), Figure 13.

$$G(s) = H_{OLP}\frac{\omega_o^2}{s^2 + s(\omega_o/Q) + \omega_o^2}$$

H_{OLP} = DC gain of the LP output.

3. **Highpass function:** available only in mode 3 at the output pins (3, 18), Figure 14.

$$G(s) = H_{OHP}\frac{s^2}{s^2 + s(\omega_o/Q) + \omega_o^2}$$

H_{OHP} = gain of the HP output for $f \rightarrow \frac{f_{CLK}}{2}$

4. **Notch function:** available at pins 3 (18) for several modes of operation.

$$G(s) = (H_{ON2})\frac{(s^2 + \omega_n^2)}{s^2 + s(\omega_o/Q) + \omega_o^2}$$

H_{ON2} = gain of the notch output for $f \rightarrow \frac{f_{CLK}}{2}$

H_{ON1} = gain of the notch output for $f \rightarrow 0$

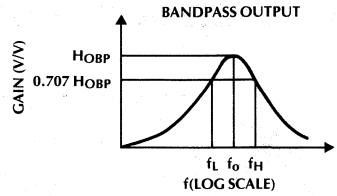
$f_n = \omega_n/2\pi$; f_n is the frequency of the notch occurrence.

5. **Allpass function:** available at pins 3(18) for mode 4, 4a.

$$G(s) = H_{OAP}\frac{[s^2 - s(\omega_o/Q) + \omega_o^2]}{s^2 + s(\omega_o/Q) + \omega_o^2}$$

H_{OAP} = gain of the allpass output for $0 < f < \frac{f_{CLK}}{2}$

For allpass functions, the center frequency and the Q of the numerator complex zero pair is the same as the denominator. Under these conditions, the magnitude response is a straight line. In mode 5, the center frequency f_Z, of the numerator complex zero pair, is different than f_o. For high numerator Q's, the magnitude response will have a notch at f_Z.

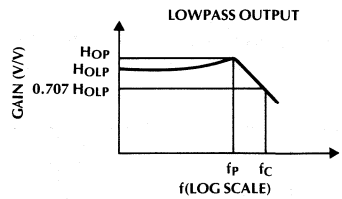


$$Q = \frac{f_o}{f_H - f_L};\ f_o = \sqrt{f_L f_H}$$

$$f_L = f_o\left(\frac{-1}{2Q} + \sqrt{\left(\frac{1}{2Q}\right)^2 + 1}\right)$$

$$f_H = f_o\left(\frac{1}{2Q} + \sqrt{\left(\frac{1}{2Q}\right)^2 + 1}\right)$$

Figure 12

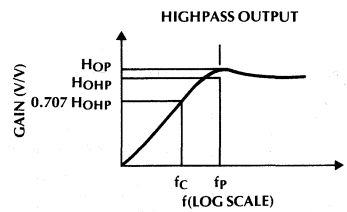


$$f_C = f_o \times \sqrt{\left(1 - \frac{1}{2Q^2}\right) + \sqrt{\left(1 - \frac{1}{2Q^2}\right)^2 + 1}}$$

$$f_P = f_o\sqrt{1 - \frac{1}{2Q^2}}$$

$$H_{OP} = H_{OLP} \times \frac{1}{\frac{1}{Q}\sqrt{1 - \frac{1}{4Q^2}}}$$

Figure 13



$$f_C = f_o \times \left[\sqrt{\left(1 - \frac{1}{2Q^2}\right) + \sqrt{\left(1 - \frac{1}{2Q^2}\right)^2 + 1}}\right]^{-1}$$

$$f_P = f_o \times \left[\sqrt{1 - \frac{1}{2Q^2}}\right]^{-1}$$

$$H_{OP} = H_{OHP} \times \frac{1}{\frac{1}{Q}\sqrt{1 - \frac{1}{4Q^2}}}$$

Figure 14

OPERATION MODES

Table 1. 1st Order Functions

MODE	PIN 2 (19)	PIN 3 (18)	f_C	f_Z
6a	LP	HP	$\frac{f_{CLK}}{100(50)} \times \frac{R2}{R3}$	
6b	LP	LP	$\frac{f_{CLK}}{100(50)} \times \frac{R2}{R3}$	
7	LP	AP	$\frac{f_{CLK}}{100(50)} \times \frac{R2}{R3}$	$\frac{f_{CLK}}{100(50)} \times \frac{R2}{R3}$

Table 2. 2nd Order Functions

MODE	PIN 1 (20)	PIN 2 (19)	PIN 3 (18)	f_o	f_N
1	LP	BP	Notch	$\frac{f_{CLK}}{100(50)}$	f_o
1a	LP	BP	BP	$\frac{f_{CLK}}{100(50)}$	
1b	LP	BP	Notch	$\frac{f_{CLK}}{100(50)} \times \sqrt{1 + \frac{R6}{R5+R6}}$	$\frac{f_{CLK}}{100(50)} \times \sqrt{1 + \frac{R6}{R5+R6}}$
1c	LP	BP	Notch	$\frac{f_{CLK}}{100(50)} \times \sqrt{\frac{R6}{R5+R6}}$	$\frac{f_{CLK}}{100(50)} \times \sqrt{\frac{R6}{R5+R6}}$
1d	LP	BP		$\frac{f_{CLK}}{100(50)}$	
2	LP	BP	Notch	$\frac{f_{CLK}}{100(50)} \times \sqrt{1 + \frac{R2}{R4}}$	$\frac{f_{CLK}}{100(50)}$
2a	LP	BP	Notch	$\frac{f_{CLK}}{100(50)} \times \sqrt{1 + \frac{R2}{R4} + \frac{R6}{R5+R6}}$	$\frac{f_{CLK}}{100(50)} \times \sqrt{1 + \frac{R6}{R5+R6}}$
2b	LP	BP	Notch	$\frac{f_{CLK}}{100(50)} \times \sqrt{\frac{R2}{R4} + \frac{R6}{R5+R6}}$	$\frac{f_{CLK}}{100(50)} \times \sqrt{\frac{R6}{R5+R6}}$
3	LP	BP	HP	$\frac{f_{CLK}}{100(50)} \times \sqrt{\frac{R2}{R4}}$	
3a	LP	BP	Notch	$\frac{f_{CLK}}{100(50)} \times \sqrt{\frac{R2}{R4}}$	$\frac{f_{CLK}}{100(50)} \times \sqrt{\frac{R_h}{R_l}}$
4	LP	BP	AP	$\frac{f_{CLK}}{100(50)}$	
4a	LP	BP	AP	$\frac{f_{CLK}}{100(50)} \times \sqrt{\frac{R2}{R4}}$	
5	LP	BP	C.Z	$\frac{f_{CLK}}{100(50)} \times \sqrt{1 + \frac{R2}{R4}}$	$\frac{f_{CLK}}{100(50)} \times \sqrt{1 - \frac{R1}{R4}}$

OPERATION MODES (Continued)

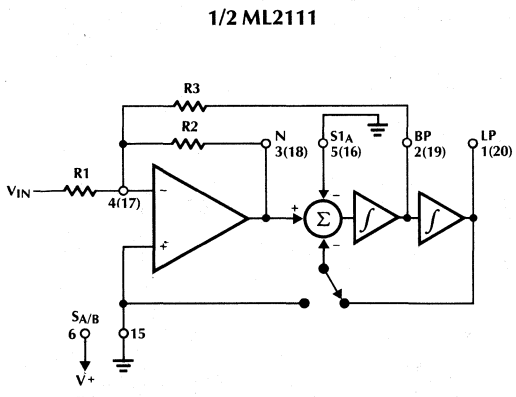
There are basically three modes of operation: mode 1, mode 2, mode 3. In the mode 1, Figure 15, the input amplifier is outside the resonant loop. Because of this, mode 1 and its derivatives (mode 1a, 1b, 1c, 1d) are faster than modes 2 and 3. The table below gives an approximation of the frequency range for each mode.

Mode 1*	High Frequency Mode
1, 1a, 1d	f_0 up to 150kHz; Q up to 20**
1b, 1c	f_0 up to 100kHz; Q up to 30
Mode 2	**Flexible for Notches**
2, 2a, 2b	f_0 up to 30kHz; Q up to 30
Mode 3	**Most Flexible/Low Component Count**
3, 3a	f_0 up to 30kHz; Q up to 30

* Q and f_0 have an inverse relationship. This table is only an approximation. Actual performance depends on board layout and stray capacitance.

** 15% of less Q deviation. Higher Q's can be realized with greater deviation.

Mode 1a, Figure 16, represents the most simple hook-up of the ML2111. Mode 1a is useful when voltage gain at the bandpass output is required. The bandpass voltage gain, however, is equal to the value of Q, and a second order, clock tunable, BP resonator can be achieved with only 2 resistors. The filter center frequency directly depends on the external clock frequency. For high order filters, mode 1a is not practical as it requires several clock frequencies to tune the overall filter response.



$$f_o = \frac{f_{CLK}}{100(50)};\ f_n = f_o;\ H_{OLP} = -\frac{R2}{R1};\ H_{OBP} = -\frac{R3}{R1};\ H_{ON1} = -\frac{R2}{R1};\ Q = \frac{R3}{R2}$$

NOTE: ELECTRICAL TESTING IS PERFORMED WITH FOLLOWING RESISTOR VALUES:
Q = 1 WITH R1 = R2 = R3 = 2k
Q = 10 WITH R1 = R3 = 20k, R2 = 2k

Figure 15. Mode 1: 2nd Order Filter Providing Notch, Bandpass, Lowpass

Mode 1a is a good choice when Butterworth filters are desired since they have poles in a circle with the same f_o. Figure 31 shows an example of a 4th order 100kHz lowpass Butterworth filter clocked at 5MHz.

A monotonic passband response with a smooth transition band results, showing the circuit's low sensitivity, even though 1% resistors are used which result in an approximate value of Q.

Mode 1, Figure 15, provides a clock tunable notch. Mode 1 is a practical configuration for second order clock tunable bandpass/notch filters. In mode 1, a bandpass output with a very high Q, together with unity gain, can be obtained with the dynamics of the remaining notch and lowpass outputs. Figure 32 is an example of a 4th order bandpass filter implemented by cascading 2 sections each with a Q of 10. This figure shows the amplitude response when $f_{CLK} = 7.5$MHz resulting in a center frequency of 150kHz and a Q of 15.5.

Modes 1b and 1c, Figures 17, 18 are similar. They both produce a notch with a frequency which is always equal to the filter center frequency. The notch and the center frequency can be adjusted with an external resistor ratio.

The clock to center frequency ratio range is:

$$\frac{500}{1} \geq \frac{f_{CLK}}{f_o} \geq \frac{100}{1} \text{ or } \frac{50}{1};\ \text{mode 1c}$$

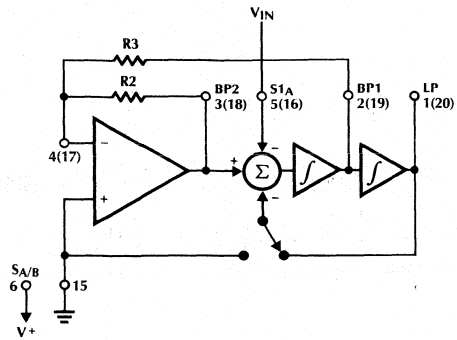
$$\frac{100}{1} \text{ or } \frac{50}{1} \geq \frac{f_{CLK}}{f_o} \geq \frac{100}{\sqrt{2}} \text{ or } \frac{50}{\sqrt{2}};\ \text{mode 1b}$$

The input impedance of the S1 pin is clock dependent, and in general R5 should not be larger than 5k for $f_{CLK} < 2.5$MHz and 1k to 2k for $f_{CLK} > 2.5$MHz. Mode 1b can be used to increase the clock to center frequency ratio beyond 100:1. For this mode, the limit for the (f_{CLK}/f_o) ratio is 500:1. Beyond this, the filter will exhibit large output offsets. Mode 1d, Figure 19, is the fastest mode of operation: In the 50:1 mode center frequencies beyond 150kHz can easily be achieved. Figure 33 is an example using mode 1d of a 4th order filter where each section has a Q of 1 independent of resistor ratios. In this mode the input amplifier is outside the damping (Q) loop. Therefore, its finite bandwidth does not degrade the response at high frequency. This allows the amplifier to be used as an anti-aliasing and continuous smoothing filter by placing a capacitor across R2.

Modes 2, 2a, and 2b have a notch output which frequency, f_n, can be tuned independently from the center frequency, f_o. For all cases, however, $f_n < f_o$. These modes are useful when cascading second order functions to create an overall elliptic highpass, bandpass or notch response. The input amplifier and its feedback resistors (R2/R4) are now part of the resonant loop. Because of this, mode 2 and its derivatives are slower than mode 1's.

OPERATION MODES (Continued)

1/2 ML2111

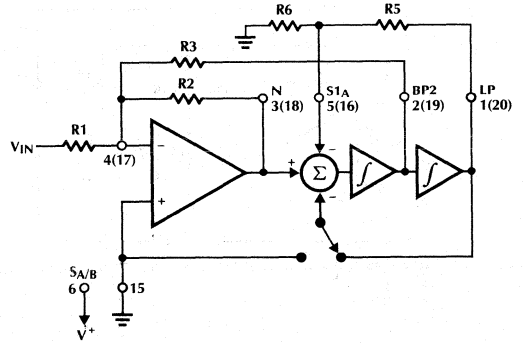


$$f_o = \frac{f_{CLK}}{100(50)}; Q = \frac{R3}{R2}; H_{OBP1} = -\frac{R3}{R2};$$

$$H_{OBP2} = 1(\text{NONINVERTING}); H_{OLP} = -1$$

Figure 16. Mode 1a: 2nd Order Filter Providing Bandpass, Lowpass

1/2 ML2111

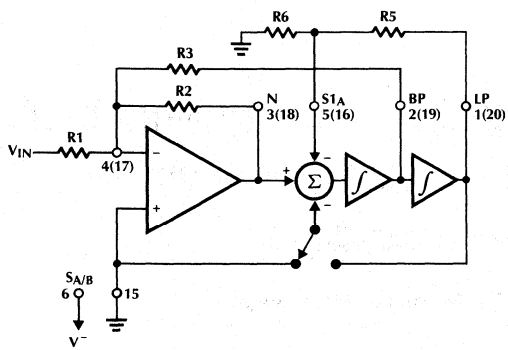


$$f_o = \frac{f_{CLK}}{100(50)}\sqrt{1+\frac{R6}{R5+R6}}; f_n = f_o; Q = \frac{R3}{R2}\sqrt{1+\frac{R6}{R5+R6}};$$

$$H_{ON1(f\to 0)} = H_{ON2}\left(f - \frac{f_{CLK}}{2}\right) = -\frac{R2}{R1}; H_{OBP} = -\frac{R3}{R1}; H_{OLP} = \frac{-R2/R1}{1+R6/(R5+R6)}; R5 < 5k\Omega$$

Figure 17. Mode 1b: 2nd Order Filter Providing Notch, Bandpass, Lowpass

1/2 ML2111

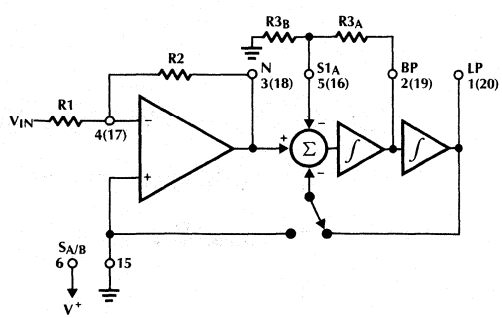


$$f_o = \frac{f_{CLK}}{100(50)}\sqrt{\frac{R6}{R5+R6}}; f_n = f_o; Q = \frac{R3}{R2}\sqrt{\frac{R6}{R5+R6}};$$

$$H_{ON1(f\to 0)} = H_{ON2}\left(f - \frac{f_{CLK}}{2}\right) = -\frac{R2}{R1}; H_{OLP} = \frac{-R2/R1}{R6/(R5+R6)}; H_{OBP} = -\frac{R3}{R1}; R5 < 5k\Omega$$

Figure 18. Mode 1c: 2nd Order Filter Providing Notch, Bandpass, Lowpass

1/2 ML2111



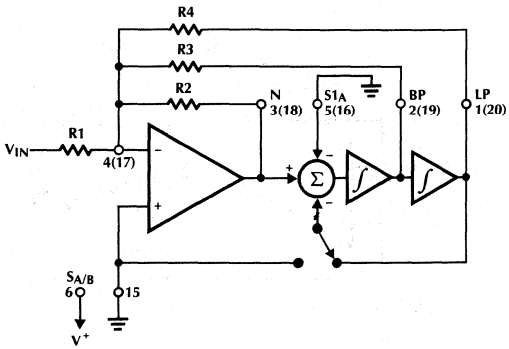
$$f_o = \frac{f_{CLK}}{100(50)}; Q = 1 + \frac{R3_A}{R3_B}; H_{OBP} = -\frac{R2}{R1} \times Q$$

$$H_{OLP} = -\frac{R2}{R1}; V_N = -\frac{R2}{R1} V_{IN}$$

Figure 19. Mode 1d: 2nd Order Filter Providing Bandpass and Lowpass for Qs Greater or Equal to 1

OPERATION MODES (Continued)

1/2 ML2111

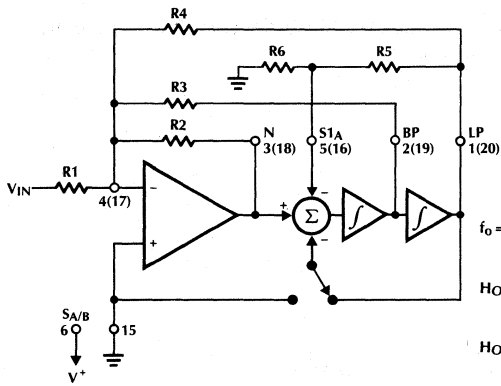


$$f_o = \frac{f_{CLK}}{100(50)}\sqrt{1+\frac{R2}{R4}};\ f_n = \frac{f_{CLK}}{100(50)};\ Q = \frac{R3}{R2}\sqrt{1+\frac{R2}{R4}};\ H_{OLP} = \frac{-R2/R1}{1+(R2/R4)}$$

$$H_{OBP} = -R3/R1;\ H_{ON1(f\to 0)} = \frac{-R2/R1}{1+(R2/R4)};\ H_{ON2}\left(f\to\frac{f_{CLK}}{2}\right) = -R2/R1$$

Figure 20. Mode 2: 2nd Order Filter Providing Notch, Bandpass, Lowpass

1/2 ML2111



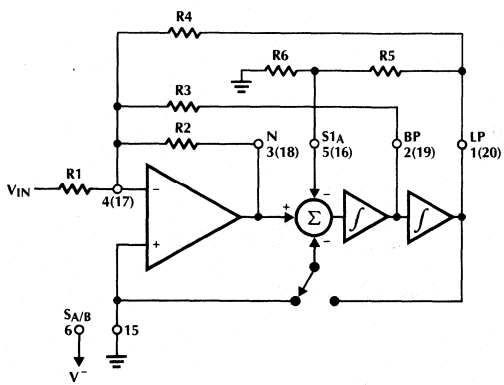
$$f_o = \frac{f_{CLK}}{100(50)}\sqrt{1+\frac{R2}{R4}+\frac{R6}{R5+R6}};\ f_n = \frac{f_{CLK}}{100(50)}\sqrt{1+\frac{R6}{R5+R6}};\ Q = \frac{R3}{R2}\sqrt{1+\frac{R2}{R4}+\frac{R6}{R5+R6}}$$

$$H_{ON1(f\to 0)} = -\frac{R2}{R1}\left\{\frac{1+R6/(R5+R6)}{1+(R2/R4)+[R6/(R5+R6)]}\right\};\ H_{ON2}\left(f\to\frac{f_{CLK}}{2}\right) = -R2/R1$$

$$H_{OBP} = -R3/R1;\ H_{OLP} = \frac{-R2/R1}{1+(R2/R4)+[R6/(R5+R6)]}$$

Figure 21. Mode 2a: 2nd Order Filter Providing Notch, Bandpass, Lowpass

1/2 ML2111



$$f_o = \frac{f_{CLK}}{100(50)}\sqrt{\frac{R2}{R4}+\frac{R6}{R5+R6}};\ f_n = \frac{f_{CLK}}{100(50)}\sqrt{\frac{R6}{R5+R6}};\ Q = \frac{R3}{R2}\sqrt{\frac{R2}{R4}+\frac{R6}{R5+R6}}$$

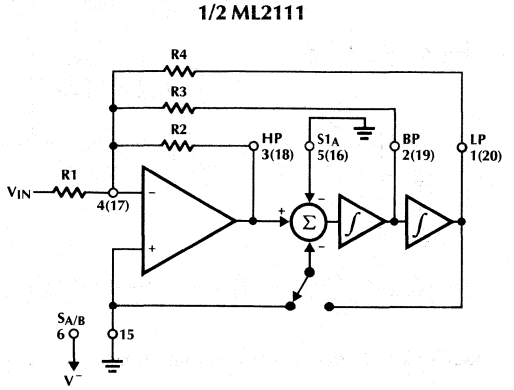
$$H_{ON1(f\to 0)} = -\frac{R2}{R1}\left\{\frac{R6/(R5+R6)}{(R2/R4)+[R6/(R5+R6)]}\right\};\ H_{ON2}\left(f\to\frac{f_{CLK}}{2}\right) = -R2/R1$$

$$H_{OBP} = -R3/R1;\ H_{OLP} = \frac{-R2/R1}{(R2/R4)+[R6/(R5+R6)]}$$

Figure 22. Mode 2b: 2nd Order Filter Providing Notch, Bandpass, Lowpass

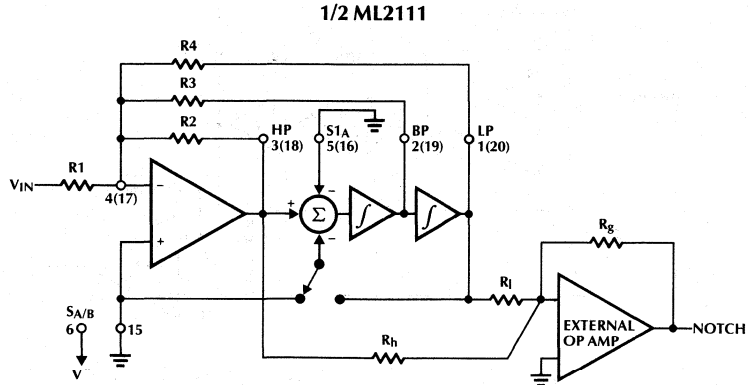
OPERATION MODES (Continued)

In mode 3, Figure 23, a single resistor ratio (R2/R4) can tune the center frequency below or above the $f_{CLK}/100$ (or $f_{CLK}/50$) ratio. Mode 3 is a state variable configuration since it provides a highpass, bandpass, lowpass output through progressive integration; notches are obtained by summing the highpass and lowpass outputs (modes 3a, Figure 24). The notch frequency can be tuned below or above the center frequency through the resistor ratio (R_h/R_l). Because of this, modes 3 and 3a are the most versatile and useful modes for cascading second order sections to obtain high order elliptic filters with frequencies up to 30 kHz.



$$f_o = \frac{f_{CLK}}{100(50)}\sqrt{\frac{R2}{R4}};\ Q = \frac{R3}{R2}\sqrt{\frac{R2}{R4}};\ H_{OHP} = -R2/R1;\ H_{OLP} = -R4/R1;\ H_{OBP} = -\frac{R3}{R1}$$

Figure 23. Mode 3: 2nd Order Filter Providing Highpass, Bandpass, Lowpass

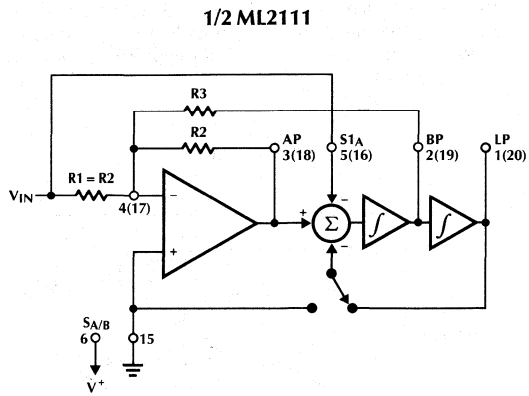


$$f_o = \frac{f_{CLK}}{100(50)}\sqrt{\frac{R2}{R4}};\ f_n = \frac{f_{CLK}}{100(50)}\sqrt{\frac{Rh}{Rl}};\ H_{OHP} = -R2/R1;\ H_{OBP} = -R3/R1,\ H_{OLP} = -R4/R1$$

$$H_{ON1}(f\to 0) = \frac{Rg}{Rl} \times \frac{R4}{R1};\ H_{ON2}\left(f\to \frac{f_{CLK}}{2}\right) = \frac{Rg}{Rh} \times \frac{R2}{R1};\ H_{ON}(f = f_o) = Q\left(\frac{Rg}{Rl}H_{OLP} - \frac{Rg}{Rh}H_{OHP}\right)$$

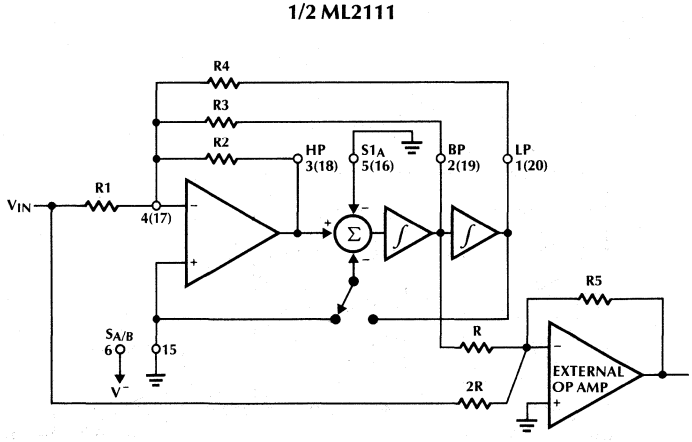
Figure 24. Mode 3a: 2nd Order Filter Providing Highpass, Bandpass, Lowpass, Notch

OPERATION MODES (Continued)



$$f_o = \frac{f_{CLK}}{100(50)}; Q = \frac{R3}{R2}; H_{OAP} = -\frac{R2}{R1}; H_{OLP} = -2; H_{OBP} = -2\left(\frac{R3}{R2}\right)$$

Figure 25. Mode 4: 2nd Order Filter Providing Allpass, Bandpass, Lowpass

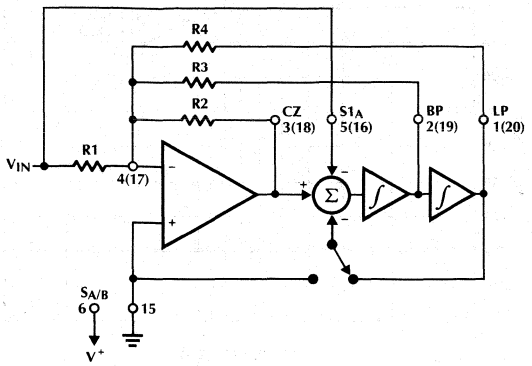


$$f_o = \frac{f_{CLK}}{100(50)}\sqrt{\frac{R2}{R4}}; Q = \frac{R3}{R2}\sqrt{\frac{R2}{R4}}; H_{OAP} = \frac{R5}{2R}; H_{OHP} = -\frac{R2}{R1}; H_{OBP} = -\frac{R3}{R1}; H_{OLP} = -\frac{R4}{R1}$$

Figure 26. Mode 4a: 2nd Order Filter Providing Highpass, Bandpass, Lowpass, Allpass

OPERATION MODES (Continued)

1/2 ML2111



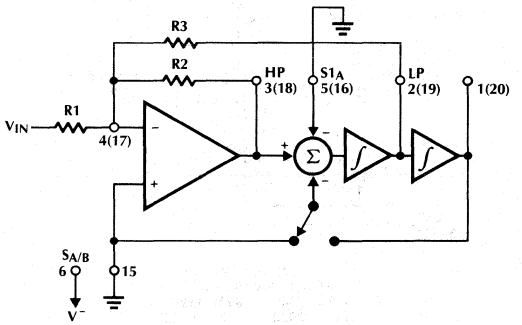
$$f_o = \frac{f_{CLK}}{100(50)}\sqrt{1+\frac{R2}{R4}};\ f_z = \frac{f_{CLK}}{100(50)}\sqrt{1-\frac{R1}{R4}};\ Q = \frac{R3}{R2}\sqrt{1+\frac{R2}{R4}}$$

$$Q_Z = \frac{R3}{R1}\sqrt{1-\frac{R1}{R4}};\ H_{OZ(f\to 0)} = \frac{(R4/R1)-1}{(R4/R2)+1};\ H_{OZ}\left(f\to\frac{f_{CLK}}{2}\right) = \frac{R2}{R1};$$

$$H_{OBP} = \frac{R3}{R2}\left(1+\frac{R2}{R1}\right);\ H_{OLP} = \frac{1+(R2/R1)}{1+(R2/R4)}$$

Figure 27. Mode 5: 2nd Order Filter Providing Numerator Complex Zeros, Bandpass, Lowpass

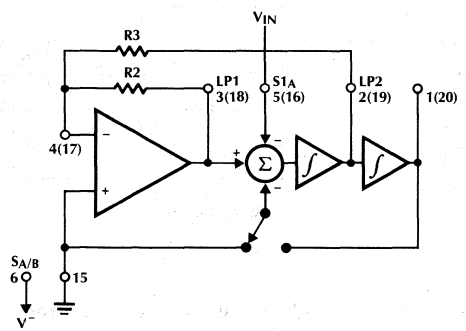
1/2 ML2111



$$f_C = \frac{f_{CLK}\,R2}{100(50)\,R3};\ H_{OLP} = -R3/R1;\ H_{OHP} = -R2/R1$$

Figure 28. Mode 6a: 1st Order Filter Providing Highpass, Lowpass

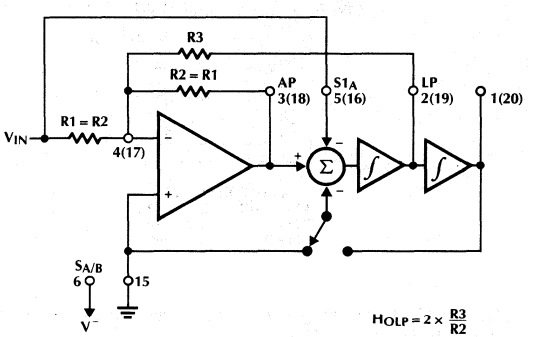
1/2 ML2111



$$f_C = \frac{f_{CLK}\,R2}{100(50)\,R3};\ H_{OLP1} = 1;\ H_{OLP2} = -\frac{R3}{R2}$$

Figure 29. Mode 6b: 1st Order Filter Providing Lowpass

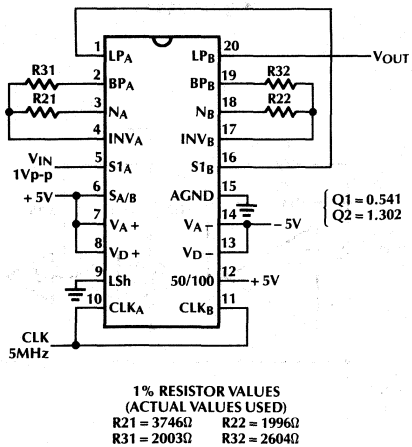
1/2 ML2111



$$f_p = \frac{f_{CLK}\,R2}{100(50)\,R3};\ f_Z = \frac{f_{CLK}\,R2}{100(50)\,R3};\ \text{GAIN AT OUTPUT} = 1\ \text{FOR}\ 0 \le f \le \frac{f_{CLK}}{2}$$

Figure 30. Mode 7: 1st Order Filter Providing Allpass, Lowpass

OPERATION MODES (Continued)



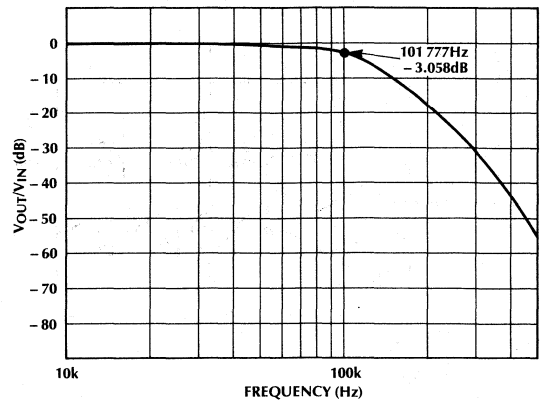
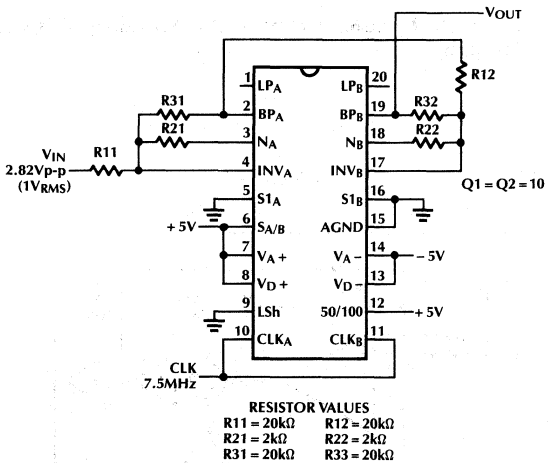


Figure 31. 4th Order, 100kHz Lowpass Butterworth Filter Obtained by Cascading 2 Sections in Mode 1a



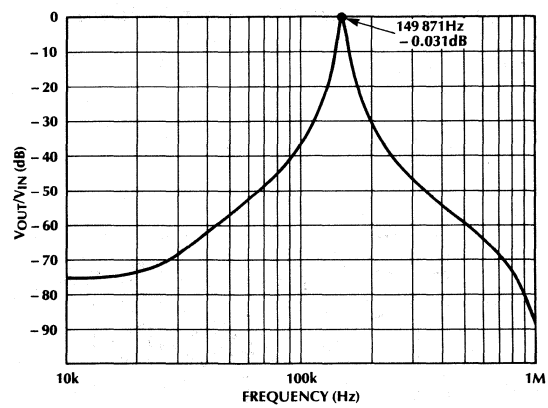


Figure 32. Cascading Two Sections in Mode 1, Each With Q = 10 Results in a Bandpass Filter with Q = 15.5 and f_o = 150kHz (f_{CLK} = 7.5MHz)

OPERATION MODES (Continued)

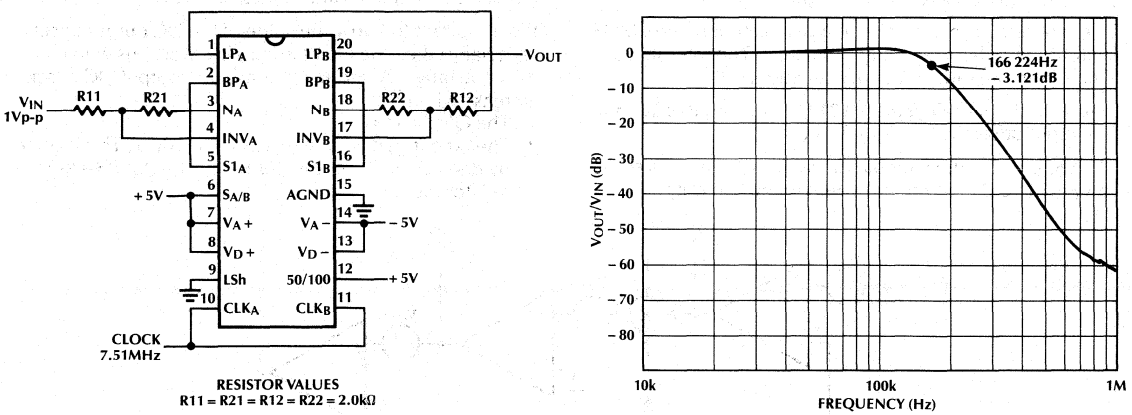


Figure 33. Cascading Two Sections in Mode 1d, Each With Q = 1 (Independent of Resistor Ratios) Creates a Sharper 4th Order Lowpass Filter

3

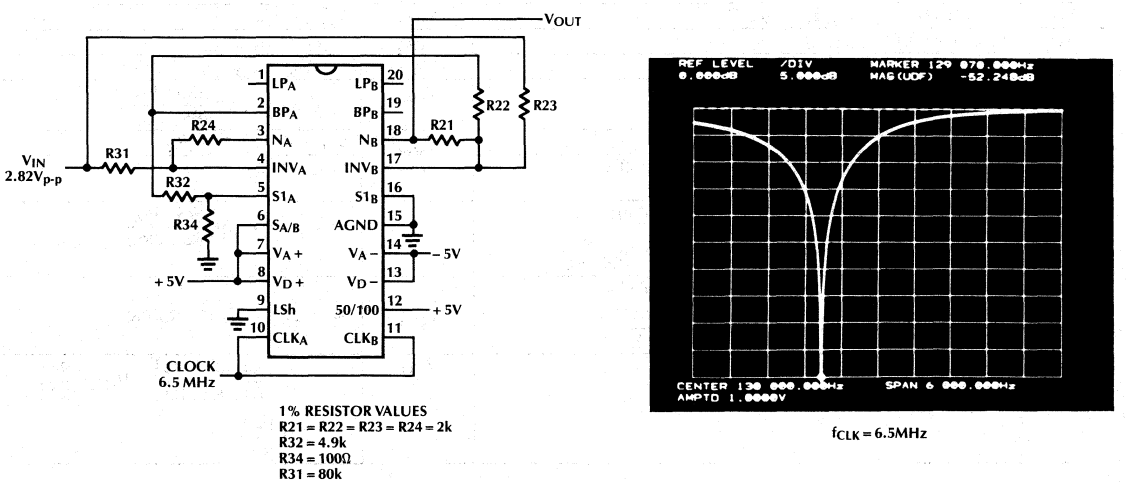


Figure 34. Notch Filter with Q = 50 and f_o = 130kHz. This Circuit Uses Side A's Biquad in Mode 1d and the Side B Op Amp to Create a Notch Whose Depth is Controlled by R31. The Notch is Created by Subtracting the Bandpass from V_{IN}. The Bandpass of Side A is Subtracted Using the Op Amp of Side B.

OFFSETS

Switched capacitor integrators generally exhibit higher input offsets than discrete R, C integrators.

These offsets are mainly the charge injection of the CMOS switches into the integrating capacitors. The internal op amp offsets also add to the overall budget.

Figure 35 shows half of the ML2111 filter with its equivalent input offsets V_{OS1}, V_{OS2}, V_{OS3}.

The DC offset at the filter bandpass output is always equal to V_{OS3}. The DC offsets at the remaining two outputs (Notch and LP) depend on the mode of operation and external resistor ratios. Table 3 illustrates this.

It is important to know the value of the DC output offsets, especially when the filter handles input signals with large dynamic range. As a rule of thumb, the output DC offsets increase when:

1. The Q's decrease
2. The ratio (f_{CLK}/f_o) increases beyond 100:1. This is done by decreasing either the (R2/R4) or the R6/(R5 + R6) resistor ratios.

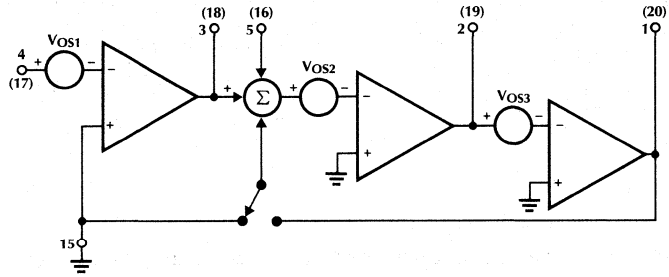


Figure 35. Equivalent Input Offsets of 1/2 ML2111 Filter

Table 3

MODE	V_{OSN} PIN 3 (18)	V_{OSBP} PIN 2 (19)	V_{OSLP} PIN 1 (20)
1,4	$V_{OS1}[(1/Q)+1+\|H_{OLP}\|]-V_{OS3}/Q$	V_{OS3}	$V_{OSN}-V_{OS2}$
1a	$V_{OS1}[1+(1/Q)]-V_{OS3}/Q$	V_{OS3}	$V_{OSN}-V_{OS2}$
1b	$V_{OS1}[(1/Q)+1+R2/R1]-V_{OS3}/Q$	V_{OS3}	$\sim(V_{OSN}-V_{OS2})\,(1+R5/R6)$
1c	$V_{OS1}[(1/Q)+1+R2/R1]-V_{OS3}/Q$	V_{OS3}	$\sim(V_{OSN}-V_{OS2})\,\frac{(R5+R6)}{(R5+2R6)}$
1d	$V_{OS1}[1+R2/R1]$	V_{OS3}	$V_{OSN}-V_{OS2}-V_{OS3}/Q$
2, 5	$[V_{OS1}(1+R2/R1+R2/R3+R2/R4)-V_{OS3}(R2/R3)]\times[R4/(R2+R4)]+V_{OS2}[R2/(R2+R4)]$	V_{OS3}	$V_{OSN}-V_{OS2}$
2a	$[V_{OS1}(1+R2/R1+R2/R3+R2/R4)-V_{OS3}(R2/R3)]\times\left[\frac{R4(1+k)}{R2+R4(1+k)}\right]+V_{OS2}\left[\frac{R2}{R2+R4(1+k)}\right];k=\frac{R6}{R5+R6}$	V_{OS3}	$\sim(V_{OSN}-V_{OS2})\,\frac{(R5+R6)}{(R5+2R6)}$
2b	$[V_{OS1}(1+R2/R1+R2/R3+R2/R4)-V_{OS3}(R2/R3)]\times\left[\frac{R4k}{R2+R4k}\right]+V_{OS2}\left[\frac{R2}{R2+R4k}\right];k=\frac{R6}{R5+R6}$	V_{OS3}	$\sim(V_{OSN}-V_{OS2})\,(1+R5/R6)$
3, 4a	V_{OS2}	V_{OS3}	$V_{OS1}\left[1+\frac{R4}{R1}+\frac{R4}{R2}+\frac{R4}{R3}\right]-V_{OS2}\left(\frac{R4}{R2}\right)-V_{OS3}\left(\frac{R4}{R3}\right)$

ORDERING INFORMATION

PART NO.	TEMPERATURE RANGE	PACKAGE
ML2111BCP	0°C to 70°C	Molded DIP
ML2111CCP	0°C to 70°C	Molded DIP
ML2111BCS	0°C to 70°C	Molded SOIC
ML2111CCS	0°C to 70°C	Molded SOIC
ML2111BIJ	−40°C to +85°C	Hermetic DIP
ML2111CIJ	−40°C to +85°C	Hermetic DIP
ML2111BMJ	−55°C to +125°C	Hermetic DIP
ML2111CMJ	−55°C to +125°C	Hermetic DIP

Data Communications

Section 4

10BASE-T Transceivers

Part Number	Applications	LED Outputs	Autopolarity	Package Types
ML4651	Internal MAU External MAU	2	No	20 Pin Skinny DIP
ML4652	Internal MAU External MAU	6	No	24 Pin Skinny DIP 28 Pin PLCC
ML4657	Internal MAU External MAU	2	Yes	20 Pin Skinny DIP
ML4658	Internal MAU External MAU	6	Yes	24 Pin Skinny DIP 28 Pin PLCC
ML4654	HUB MAU	5	Yes	20 Pin Skinny DIP 28 Pin PLCC

Fiber Optic Quantizers

Part Number	Output Types	Bandwidth	Package Types
ML4621	TTL, ECL	50 MHz min.	24 Pin Skinny DIP 28 Pin PLCC
ML4622	TTL, ECL	40 MHz min.	16 Pin Skinny DIP 16 Pin Narrow SOIC

FOIRL Transceiver

Part Number	Applications	LED Outputs	Package Types
ML4661	Internal MAU External MAU	5	28 Pin PLCC

Micro Linear

ML4621, ML4622

Data Quantizer

GENERAL DESCRIPTION

The ML4621 and ML4622 Data Quantizers are low noise, wideband, bipolar monolithic ICs designed specifically for signal recovery applications in fiberoptic receiver systems. They contain a two stage wideband limiting amplifier which is capable of accepting an input signal as low as 2mV with a 55dB dynamic range. This high level of sensitivity is achieved by using a DC restoration feedback loop which nulls any offset voltage produced in the limiting amplifier.

The output stage is a high speed comparator circuit with both TTL and ECL outputs. An enable pin is included for added control.

The Minimum Signal Discriminator circuit provides a Link Monitor function with a user selectable reference voltage. This circuit monitors the peaks of the input signal and provides a logic level output indicating when the input falls below an acceptable level. This output can be used to disable the Quantizer and/or drive an LED, providing a visible link status.

The ML4621 is the most flexible Quantizer because of the additional nodes made available and a slightly higher bandwidth. The ML4622 is a reduced pin count version of the ML4621 with a slighly lower bandwidth and burst mode receive ability.

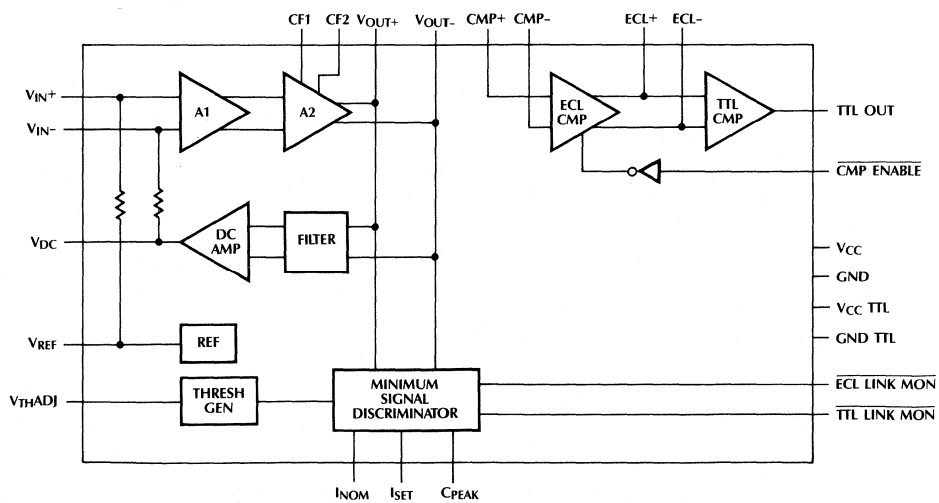
FEATURES

- 50MHz minimum bandwidth (ML4621) for data rates of up to 100MBd
- 40MHz minimum bandwidth (ML4622) for data rates up to 80MBd
- Can be powered by either +5V providing TTL level outputs or –5.2V providing ECL levels
- Low noise design:
  25μV RMS over 50MHz noise bandwidth
- Adjustable Link Monitor function
- Wide 55dB input dynamic range
- 10ns minimum input pulse
- Low power design
- Available in 16-pin SOIC (Narrow) or DIP (ML4622), 24-pin Skinny DIP (ML4621) and 28-pin PLCC (ML4621)

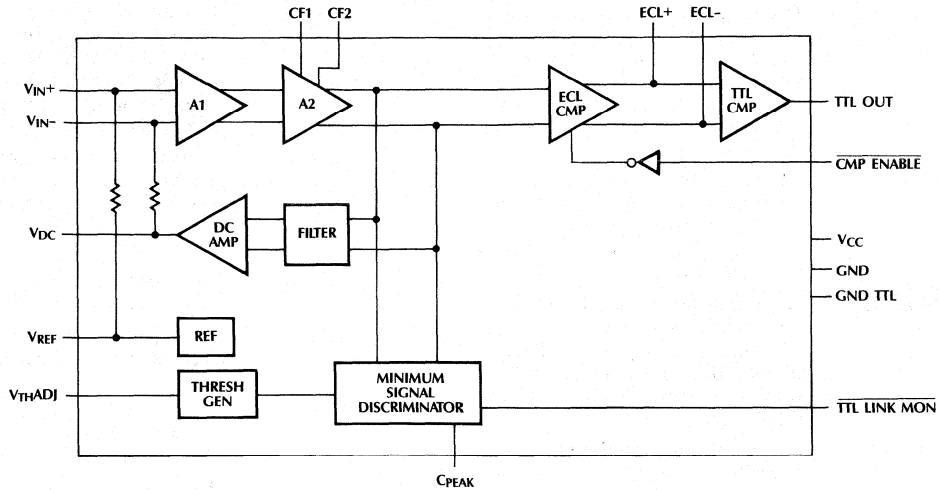
APPLICATIONS

- IEEE 802.3 FOIRL Receiver
- IEEE 802.5 4 and 16 Mbps Fiber Optic Token Ring
- IEEE 802.4 Fiber Optic Token Bus
- Fiber Optic Data Communications and Telecommunications Receivers

ML4621 BLOCK DIAGRAM

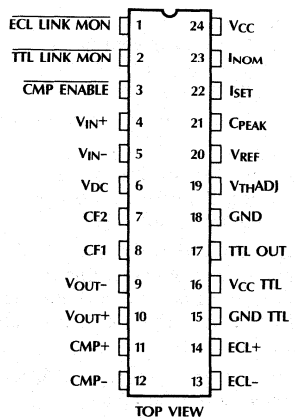


ML4622 BLOCK DIAGRAM

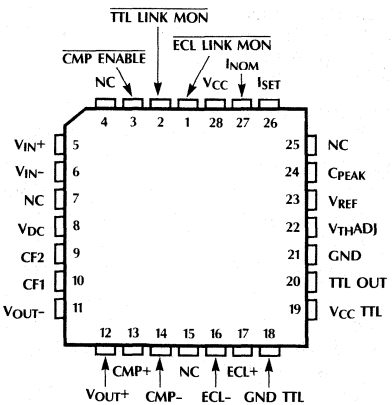


PIN CONNECTIONS

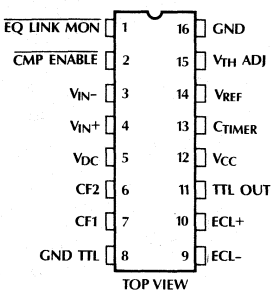
ML4621
24-Pin Skinny DIP



ML4621
28-Pin PCC



ML4622
16-Pin DIP or SOIC (Narrow)



PIN DESCRIPTION

NAME	FUNCTION
$\overline{\text{ECL LINK MON}}$	ECL Link Monitor output. Signal is low when the V_{IN}+, V_{IN}– inputs exceed the minimum threshold, which is set by a voltage on the V_{TH}ADJ pin. Signal is high when the input signal level is below the threshold.
$\overline{\text{TTL LINK MON}}$	TTL Link Monitor output. Same logic function as ECL LINK MON. Capable of driving a 10mA LED indicator. This pin normally tied to CMP ENABLE.
$\overline{\text{CMP ENABLE}}$	A low voltage at this TTL input pin enables both the ECL and the TTL outputs. A high TTL voltage disables the comparator output with ECL+ high, ECL– low, and TTL OUT high.
V_{IN}–	This input pin should be capacitively coupled to the input source or to ground. (The input resistance is approximately 8kΩ.)
V_{IN}+	This input pin should be capacitively coupled to the input source or to ground. (The input resistance is approximately 8kΩ.)
CMP–	This comparator input pin is an open base configuration which relies on the DC bias of the amplifier output to establish the proper DC operating voltage. This voltage should be reestablished if filtering is implemented between V_{OUT}– and CMP–.
ECL–	The ECL comparator negative output.
ECL+	The ECL comparator positive output.
GND TTL	The negative supply for the TTL comparator stage. If the TTL output is not necessary, connect GND TTL and V_{CC} TTL to V_{CC}.
V_{CC} TTL	The positive supply for the TTL comparator stage. If the TTL output is not necessary, connect GND TTL and V_{CC} TTL to V_{CC}.
TTL OUT	TTL data output. (Totem pole type output stage.)

NAME	FUNCTION
V_{DC}	An external capacitor on this pin integrates an error signal which nulls the offset of the input amplifier. If the DC feedback loop is not being used, this pin should be connected to V_{REF}.
CF2	A capacitor from this pin to ground controls the maximum bandwidth of the amplifier to accommodate lower operating frequencies.
CF1	The capacitor on this pin should match the one on CF2.
V_{OUT}–	The negative output of the amplifier, which is normally tied to CMP–.
V_{OUT}+	The positive output of the amplifier, which is normally tied to CMP+.
CMP+	This comparator input pin is an open base configuration which relies on the DC bias of the amplifier output to establish the proper DC operating voltage. This voltage should be reestablished if filtering is implemented between V_{OUT}+ and CMP+.
GND	Negative supply. Connect to –5.2V for ECL operation, or to ground for TTL operation.
V_{TH}ADJ	This input pin sets the minimum amplitude of the input signal required to cause the link monitors to go low.
V_{REF}	A 2.5V reference with respect to GND.
C_{PEAK}	A capacitor from this pin to ground determines the Link Monitor response time.
I_{SET}	Current into an internal diode connected between this pin and GND is turned around and pulled from C_{PEAK}. This pin is normally connected to I_{NOM}.
I_{NOM}	Sets a current of approx. 125μA when connected to I_{SET}.
V_{CC}	Positive supply. Connect to ground for ECL operation, or to 5V for TTL operation.

ABSOLUTE MAXIMUM RATINGS

V_{CC} - GND ..... -0.3 to +7.0
V_{CC} TTL - GND TTL ..... -0.3 to +7.0
Inputs/Output GND ..... -0.3 to V_{CC} +0.3
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering 10 sec.) ..... +260°C

Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

ML4621 ELECTRICAL CHARACTERISTICS

Over recommended operating conditions of T_A = 0°C to 70°C, V_{CC} = 5V ± 5%, GND = 0V unless otherwise noted.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
I_{CC1}	V_{CC} Supply Current		65	100	mA	V_{CC} TTL = GND TTL = V_{CC}
I_{CC2}	V_{CC} Supply Current (TTL Out Enabled)		70	110	mA	V_{CC} TTL = V_{CC} GND TTL = GND
$I_{V_{REF}}$	V_{REF} Output Current	-5.0		0.5	mA	
V_{REF}	Reference Voltage	2.45	2.55	2.65	V	
A_V	Amplifier Gain A1 A2		75		V/V	V_{IN} = 5mV
V_{IN}	Input Signal Range	2		1400	mV_{P-P}	
V_{TH}ADJ Range	External Voltage at V_{TH}ADJ to set V_{TH}	1		2.5	V	
V_{OS}	Input Offset		3		mV	V_{DC} = V_{REF} (DC loop inactive)
E_N	Input Referred Noise		25		μV	50MHz BW
BW	3dB Bandwidth	50	65		MHz	
V_{IN} PW	Min Input Pulsewidth		10		ns	
R_{IN}	Input Resistance		8		kΩ	V_{IN}+, V_{IN}-
t_{PD} AMP	Amplifier Propagation Delay	4		8	ns	From V_{IN}+, V_{IN}- to V_{OUT}+, V_{OUT}- V_{IN} = $10mV_{P-P}$
t_{PD} ECL	ECL Comparator Propagation Delay	4		8	ns	From CMP+, CMP- to ECL+, ECL- V_{IN} = $10mV_{P-P}$
t_{PD} TTL	TTL Comparator Propagation Delay	4		8	ns	From ECL+, ECL- to TTL OUT V_{IN} = $10mV_{P-P}$
$R_{V_{TH}ADJ}$	Input Resistance of V_{TH}ADJ		6.8		kΩ	
$I_{V_{OUT}}$	Output Current of V_{OUT}+ and V_{OUT}-			3	mA	
I_{CMP}	Leakage Current of CMP+ and CMP-		25		μA	
VCM_{CMP}	Common Mode Range of CMP+ and CMP-	GND + 2.0		V_{CC} - 1.0	V	
ECL V_{OH}	Output High Voltage at ECL+, ECL-	3.94		4.30	V	With 200Ω load tied to V_{CC} - 2V T_A = 25°C
ECL V_{OL}	Output Low Voltage at ECL+, ECL-	3.11		3.38	V	With 200Ω load tied to V_{CC} - 2V T_A = 25°C
A_V ECL	ECL CMP Gain		100		V/V	
TTL V_{OH}		2.4			V	V_{CC} TTL = 5V, I_{OH} = -50μA
TTL V_{OL}				0.4	V	V_{CC} TTL = 5V, I_{OL} = 2mA
TTL V_{IH}		2.0			V	
TTL V_{IL}				0.8	V	
TTL I_{IH}		-50		50	μA	V_{IH} = 2.4V
TTL I_{IL}		-1.6		0	mA	V_{IH} = 0.4V
I_{NOM}			125		μA	I_{NOM} = I_{SET}

ML4622 ELECTRICAL CHARACTERISTICS

Over recommended operating conditions of T_A = 0°C to 70°C, V_{CC} = 5V ± 10%, GND = 0V unless otherwise noted.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
I_{CC1}	V_{CC} Supply Current (TTL Output Disabled)		25	40	mA	GND TTL = V_{CC}
I_{CC2}	V_{CC} Supply Current (TTL Output Enabled)		45	65	mA	GND TTL = GND
V_{REF}	Reference Voltage	2.45	2.55	2.65	V	
$I_{V_{REF}}$	V_{REF} Output Current	-5.0		0.5	mA	
A_V	Amplifier Gain A1 A2		75		V/V	V_{IN} = 5mV
V_{IN}	Input Signal Range	2		1400	mV_{P-P}	
V_{TH}ADJ Range	External Voltage at V_{TH}ADJ to set V_{TH}	0		2.5	V	
V_{OS}	Input Offset		3		mV	V_{DC} = V_{REF} (DC loop inactive)
E_N	Input Referred Noise		25		μV	50MHz BW
BW	3dB Bandwidth	40	55		MHz	
V_{IN} PW	Min Input Pulsewidth		10		ns	
R_{IN}	Input Resistance		5		kΩ	V_{IN}+, V_{IN}-
$I_{V_{TH}ADJ}$	Input Bias Current of V_{TH}ADJ	-40		40	μA	
t_{PDTTL}	Propagation Delay	12		24	ns	From V_{IN}+, V_{IN}- to TTL Out V_{IN} = 10mV_{P-P}
t_{PDECL}	Propagation Delay	8		16	ns	From V_{IN}+, V_{IN}- to ECL+, ECL- V_{IN} = 10mV_{P-P}
TTL V_{OH}		2.4			V	V_{CC} TTL = 5V, I_{OH} = -50μA
TTL V_{OL}				0.5	V	V_{CC} TTL = 5V, I_{OL} = 2mA
TTL V_{IH}		2.0			V	
TTL V_{IL}				0.8	V	
TTL I_{IH}		-50		50	μA	V_{IH} = 2.4V
TTL I_{IL}		-1.6		0	mA	V_{IH} = 0.4V

FUNCTIONAL DESCRIPTION

AMPLIFIER

The Quantizers have a two stage limiting amplifier with an input common mode range of (GND + 1.8V) to (V_{CC} – 1.5V). Maximum sensitivity is achieved through the use of a DC restoration feedback loop and AC coupling the input. When AC coupled, the input DC bias voltage is set by an on-chip network at about 1.9V. These coupling capacitors, in conjunction with the input impedance of the amplifier, establish a high pass filter with a 3dB corner frequency, f_L, at

$$f_L = \frac{1}{2\pi\ 8000\ C} \text{ (ML4621)} \quad (1)$$

$$f_L = \frac{1}{2\pi\ 5000\ C} \text{ (ML4622)}$$

Since the amplifier has a differential input, two capacitors of equal value are required. If the signal driving the input is single ended, one of the coupling capacitors can be tied to V_{CC} as shown in figure 1. The high corner frequency can also be adjusted by attaching capacitors to CF1 and CF2. The equation for adjusting this corner is

$$f_H = \frac{1}{2\pi\ 425\ C} \quad (2)$$

Although the input is AC coupled, the offset voltage *within* the amplifier will be present at the amplifier's output. This is represented by V_{OS} in figure 2. In order to reduce this error a DC feedback loop is incorporated. This negative feedback loop nulls the offset voltage, forcing V_{OS} to be zero. An external capacitor at V_{DC} is used to store the offset voltage. Although the value of this capacitor is non-critical, the pole it creates can effect the stability of the feedback loop. To avoid stability problems using the ML4621, the

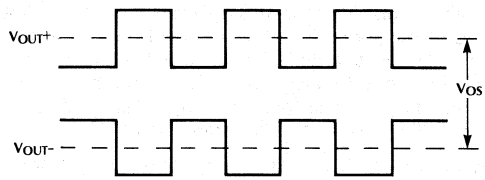


Figure 2.

value of this capacitor should be at least 100 times smaller than the input coupling capacitors. On the ML4622 the input coupling capacitors should be 100 times smaller than the V_{DC} capacitor.

On the ML4621, the output of the amplifier is isolated from the comparator and made available to the user. This allows the user to add circuitry between the amplifier and the comparator for wave shaping and other signal conditioning as desired.

COMPARATOR

Two types of comparators are employed in the output section of these Quantizers. The high speed ECL comparator is used to provide the ECL level outputs and in turn drives the TTL comparator. The enable pin, CMP ENABLE, is provided to control the ECL comparator. When CMP ENABLE is low the comparators function normally. When it's high, it forces ECL+ high, ECL– low, and TTL OUT high. On the ML4622 when CMP ENABLE is high, it forces ECL+ low, ECL– high, and TTL OUT low. The CMP ENABLE pin can be controlled with TTL level signals when the Quantizer is powered by 5V and ground.

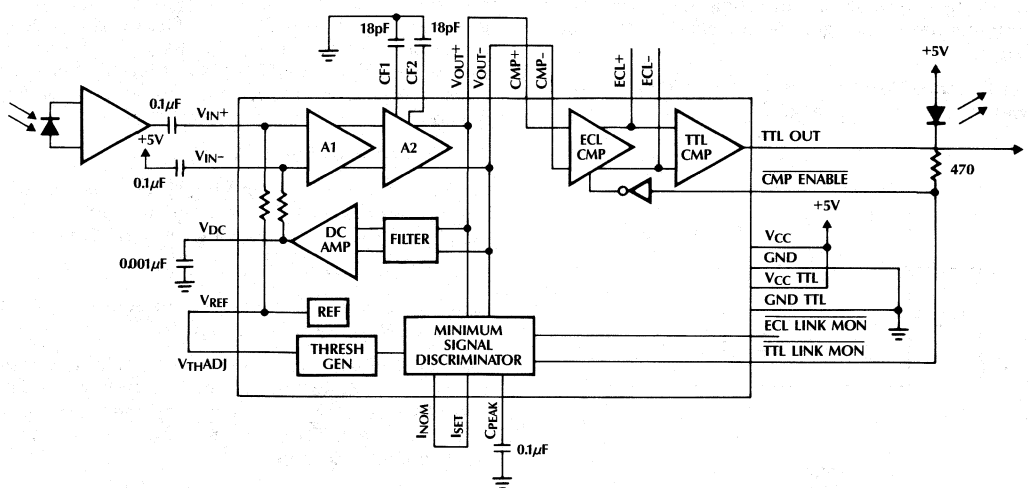


Figure 1. The ML4621 Configured for 20MHz Bandwidth with TTL Output

LINK MONITOR (ML4621)

This function is implemented by the Minimum Signal Discriminator and the Threshold Generator circuits. The purpose of this function is to monitor the input signal and provide a status signal indicating when the input falls below a preset voltage level. This is done by peak detecting the output of the amplifier section and comparing this level with the voltage at $V_{TH}ADJ$.

The equation which determines the droop rate of the peak detector is

$$\frac{dV}{dt} = \frac{I_{SET}}{C} \quad (3)$$

In this equation C is the peak capacitor at C_{PEAK}. On the ML4621 the droop rate of the peak detector can be adjusted two ways:

1) By adjusting the value of the peak capacitor at C_{PEAK}.
2) By adjusting the charge current into the peak capacitor at I_{SET}.

The charge current, I_{ISET}, can be controlled externally by connecting a resistor, R_{EXT}, between I_{SET} and V_{CC}. I_{ISET} will then be

$$I_{ISET} = \frac{V_{CC} - 0.7}{R_{EXT} + 1700} \quad (4)$$

For convenience, an on-chip current source of 125μA is available by connecting I_{NOM} to I_{SET}.

The Threshold Generator level shifts the reference voltage at $V_{TH}ADJ$ through a circuit which has a temperature coefficient matching that of the limiting amplifier. The relationship between $V_{TH}ADJ$ and V_{TH} (the minimum *peak* voltage at the input which will trigger the Link Monitor) is:

$$V_{TH}ADJ = 600V_{TH} + 0.7 \quad (5)$$

The on-chip reference voltage, V_{REF}, can be tied directly to $V_{TH}ADJ$ to set the threshold level. This will set the minimum input signal on the ML4621 at about 3mV (peak).

A lower threshold level can be set by dividing down V_{REF} with a resistor string, as in figure 3.

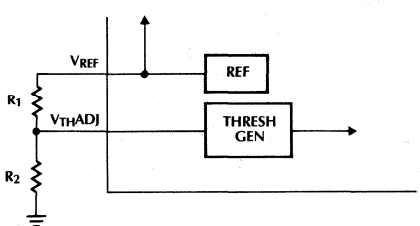


Figure 3.

Since the ML4621 has a relatively low input impedance of 6.8K and is offset by one diode drop, the equation which accounts for the load and offset is:

$$V_{TH}ADJ = \frac{R_2(6800V_{REF} + 0.7R_1)}{6800(R_1 + R_2) + R_1R_2} \quad (8)$$

LINK MONITOR (ML4622)

The ML4622 Link Monitor circuit operates slightly different than the ML4621. Instead of using the droop rate of the peak detector to determine the time for the link monitor to shut off, the ML4622 uses both a threshold detector to measure the peaks and a timer to measure the time between the peaks.

The equation which determines the time between peaks is:

$$\frac{C_{PEAK} \times R_{PEAK}}{4.3}$$

where $500\Omega < R_{PEAK} < 200k\Omega$ and R_{PEAK} is in parallel with C_{PEAK}

The threshold generator level shifts the reference voltage at $V_{TH}ADJ$ through a circuit that has a temperature coefficient matching the limiting amplifier. The relationship between $V_{TH}ADJ$ and V_{TH} (the minimum peak voltage at the input which will trigger the Link Monitor) is:

$$V_{TH}ADJ = 800\ V_{TH}$$

The on-chip reference voltage, V_{REF}, can be tied directly to $V_{TH}ADJ$ to set the threshold level. This will set the minimum input signal to about 6.5mV peak.

A lower threshold level can be set by dividing down V_{REF} with a resistor string, as in figure 3.

THRESHOLD ADJUSTMENT EXAMPLE

If you are using the ML4621 and you want the Link Monitor to trigger when the received optical power goes below 1μW (-30dBm), you first need to calculate the resultant voltage at $V_{IN}+$ and $V_{IN}-$. If you are using the Hewlett-Packard HFBR-24X6 Fiberoptic Receiver with a responsitivity of 8mV/μW, the peak-to-peak voltage would be:

$$1\mu W \times 8mV/\mu W = 8mV_{P-P} \quad (9)$$

So the Link Monitor should trigger at some point slightly lower than 4mV peak, say 3mV. Setting V_{TH} in equation 5 to 3mV and solving for $V_{TH}ADJ$ yields:

$$V_{TH}ADJ = 600(.003) + 0.7 = 2.5V$$

This is a convenient value since the reference voltage supplied by the Quantizer, V_{REF}, is 2.5V.

The Link Monitor has about 0.4mV (peak) hysteresis built-in. The ML4622 has about 1dB hysteresis built-in. More hysteresis can be induced by connecting a resistor between TTL LINK MON and $V_{TH}ADJ$ creating a positive feedback loop.

Refer to Micro Linear's Application Note 6 for more detail.

BURST MODE

In some fiber optic links, the idle signal is DC, or of a frequency that is substantially different from the data. For these links, a faster response time of the DC loop and the Link Monitor is required.

The ML4622 has been designed to accommodate these two requirements. The input coupling capacitors can be relatively small and still maintain stability. The smaller the input coupling capacitors are, the faster the DC loop response time is. The Link Monitor is also enhanced to have a faster response time.

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ML4621CP	0°C to +70°C	MOLDED DIP
ML4621CQ	0°C to +70°C	MOLDED PCC
ML4622CP	0°C to +70°C	MOLDED DIP
ML4622CS	0°C to +70°C	MOLDED SOIC

Micro Linear

ML4651, ML4652, ML4657, ML4658

10BASE-T Transceiver

GENERAL DESCRIPTION

The ML4651/ML4652/ML4657/ML4658 10BASE-T Transceivers are single chip cable line driver/receivers that provides all of the functionality required to implement both an internal and external IEEE 802.3 10BASE-T MAU. These parts offer a standard IEEE 802.3 AU interface that allows them to directly connect to industry standard manchester encoder/decoder chips or an AUI cable.

These parts require a minimal number of external components, and fully conform to the IEEE 802.3 10BASE-T standard. The differential current driven transmitter offers superior performance because of its highly symetrical switching. This results in low RFI noise and low jitter.

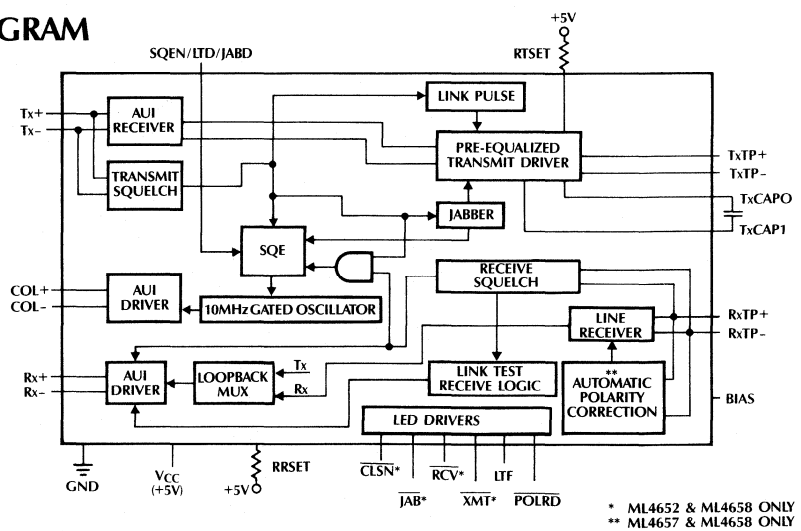
The Transceiver easily interfaces to 100Ω unshielded twisted pair cable, 150Ω shielded twisted pair cable, or a range of other characteristic impedances by simply changing one external resistor. Jabber, Link Test, and SQE Test are fully integrated onto the chip with enable/disable options. A polarity detection status pin, which can drive an LED, is provided for receive data, and the ML4657 and ML4658 offer automatic polarity correction.

The ML4651 and ML4657 are available in a 20 pin skinny DIP. The ML4652 and ML4658 add four more pins which are used to drive network status LEDs. The ML4652 and ML4658 are available in 24 pin skinny DIP as well as a 28 pin PLCC.

FEATURES

- Complete implementation of IEEE 802.3 10BASE-T Medium Attachment Unit (MAU)
- Incorporates an AU interface for use in an external MAU or internal MAU
- Single +5 volt supply ± 10%
- No crystal or clock input
- Current Driven Output for low RFI noise and low jitter
- Capable of driving 100Ω unshielded twisted pair cable or 150Ω shielded twisted pair cable
- Polarity detect status pin capable of driving an LED
- Automatic Polarity Correction on the ML4657 and ML4658
- On-chip Jabber logic, Link Test, and SQE test with enable/disable option
- ML4652 and ML4658 provide six network status LED output pins
- ML4651 and ML4657 are available in a 20 pin skinny DIP
- ML4652 and ML4658 are available in a 24 pin skinny DIP or 28 pin PLCC
- Semi-standard option using Micro Linear's FB3651 LAN Transceiver Tile Array

BLOCK DIAGRAM



PIN DESCRIPTION (DIP)

PIN NO. ML4651	PIN NO. ML4652	NAME	FUNCTION
	1	$\overline{\text{CLSN}}$	Indicates that a collision is taking place. Active low LED driver, open collector. Event is extended 100ms for visibility.
1	2	COL+	Gated 10MHz signal used to indicate a collision, SQE test, or jabber. Balanced differential line driver outputs that meet AU interface specifications. AC or DC coupled.
2	3	COL–	
3	4	SQEN/LTD/JABD	SQE Test Enable, Link Test Disabled, Jabber Disabled. This input uses four voltage levels to configure the chip as shown in Table 1.

Table 1. SQEN/LTD/JABD Pin Configuration

Pin	SQE Test	Link Test	Jabber
0V (GND)	Disabled	Enabled	Enabled
1.2V	Disabled	Disabled	Disabled
BIAS	Enabled	Disabled	Enabled
5V (V_{CC})	Enabled	Enabled	Enabled

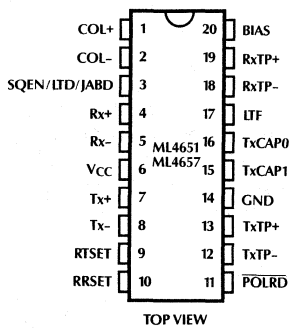
When link test is disabled, no link pulses are transmitted, and the transmitter and receiver will not be disabled as a result of a loss of receive link pulses. When Jabber is disabled the transmitter can transmit continuously without interruption, and the collision oscillator will not be activated.

4	5	Rx+	Manchester encoded receive data output to the local device. Balanced differential line driver outputs that meet AU interface specifications. AC or DC coupled.
5	6	Rx–	
6	7	V_{CC}	+5 Volt power input.
7	8	Tx+	Balanced differential line receiver inputs that meet AU interface specifications. These inputs may be AC or DC coupled. When AC coupled, the BIAS pin is used to set the common mode voltage. Signals meeting the transmitter squelch input requirements are pre-equalized and output on TxTP+ and TxTP–.
8	9	Tx–	
9	10	RTSET	When using 100Ω unshielded twisted pair, a 220Ω resistor is tied between this pin and V_{CC}. When using 150Ω shielded twisted pair, a 330Ω resistor is tied between this pin and V_{CC}.
10	11	RRSET	A 1% 61.9KΩ resistor tied from this pin to V_{CC} is used for internal biasing.
11	12	$\overline{\text{POLRD}}$	Receive Polarity status. Active low LED Driver, open collector output. Indicates the polarity of the receive twisted pair regardless of auto polarity correction. When this pin is high, the receive polarity is correct, and when this pin is low the receive polarity is reversed.
	13	$\overline{\text{XMT}}$	Indicates that transmission is taking place on the TxTP+, TxTP– pair. Active low LED driver, open collector. It is extended 100ms for visibility.
	14	$\overline{\text{RCV}}$	Indicates that the transceiver has unsquelched and is receiving data from the twisted pair. Active low LED driver, open collector. It is extended 100ms for visibility.
12	15	TxTP–	Pre-equalized differential balanced current driven output. These outputs are connected to a balanced transmit output filter which drives the twisted pair cable through pulse transformers. The output current is set with an external resistor connected to RTSET allowing the chip to drive 100Ω unshielded twisted pair, 150Ω shielded twisted pair cables or a range of other characteristic impedances.
13	16	TxTP+	
14	17	GND	Ground reference.
15	18	TxCAP1	An external capacitor of 330pF is tied between these two pins to set the pulse width for the pre-equalization on the transmitter. If these two pins are shorted together, no pre-equalization occurs.
16	19	TxCAP0	

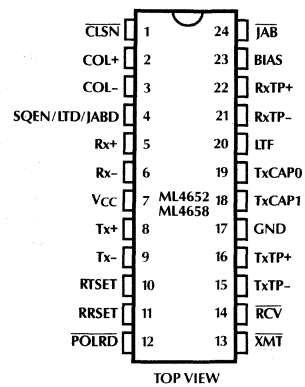
PIN DESCRIPTION (DIP) (Continued)

PIN NO. ML4651	PIN NO. ML4652	NAME	FUNCTION
17	20	LTF	Link Test Fail. Active high. Normally this pin is low, indicating that the link is operational. If the link goes down resulting from the absence of link pulses or frames being received, the chip will go into the Link Test Fail state and bring LTF high. In the Link Test Fail state, both the transmitter and receiver are disabled, however link pulses are still sent. A station that only has access to the AUI can detect a Link Test Fail by the absence of loopback. This pin is low when the Link Test is disabled. Open collector LED output.
18	21	RxTP–	Twisted Pair receive data input. When this signal exceeds the receive squelch requirements the receive data is buffered and sent to the Rx+/– outputs.
19	22	RxTP+	
20	23	BIAS	Bias voltage, output. Used to bias the receive twisted pair inputs as well as the Tx+/– inputs when they are AC coupled.
	24	$\overline{JAB}$	Open collector TTL output capable of driving an LED. When in the Jabber state, this pin will be low and the transmitter will be disabled. In the Jabber "OK" state this pin will be high.

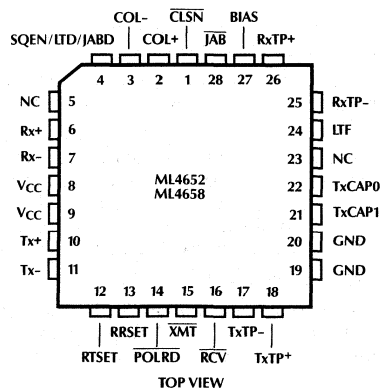
PIN CONNECTION



TOP VIEW



TOP VIEW



TOP VIEW

ABSOLUTE MAXIMUM RATINGS
(Note 1)

Power Supply Voltage Range
- V_{CC} ..... -0.3 to 6V

Input Voltage Range
- Digital Inputs (SQEN, LTD) ..... -0.3 to V_{CC}
- Tx+, Tx–, RxTP+, RxTP– ..... -0.3 to V_{CC}

Input Current
- RRSET, RTSET, $\overline{JAB}$, $\overline{CLSN}$, $\overline{XMT}$, $\overline{RCV}$, LTF 60mA

Output Current
- TxTP+, TxTP– 80mA

Storage Temperature ..... -65°C to +150°C

Lead Temperature (Soldering 10 seconds) ..... 260°C

OPERATING CONDITIONS
(Note 2)

Supply Voltage (V_{CC}) ..... 5V ± 10%
LED on Current 10mA
RRSET ..... 61.9KΩ ± 1%
RTSET ..... 220Ω ± 1%
TxCAP 330pF

ELECTRICAL CHARACTERISTICS
Unless otherwise specified T_A = 0°C to 70°C (Note 3), V_{CC} = 5V ± 10%

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Power Supply Current I_{CC} (Note 4)	V_{CC} = 5V			140	mA
LED Drivers: V_{OL}	R_L = 510Ω (Note 5)			0.8	V
Transmit Peak Output Current	RTSET = 220Ω		42 (Note 6)		mA
Transmit Squelch Voltage Level (Tx+, Tx–)			–170		mV
Differential Input Voltage (RxTP+, RxTP–)		±0.300		±3.1	V
Receiver Input Resistance		10			KΩ
SQEN/LTD/JABD Input Resistance			12		KΩ
Receive Squelch Voltage Level (RxTP+, RxTP–)		300	450	585	mV-p
Differential Output Voltage (Rx+/–, COL+/–)		±550		±1200	mV
Common Mode Output Voltage (Rx+/–, COL+/–)			4.0		V
Differential Output Voltage Imbalance (Rx+/–, COL+/–)			2	±40	mV
BIAS Voltage			3.2		V
SQEN/LTD/JABD	SQE TEST disabled All disabled Link Test disabled All Enabled	 1.1 BIAS–0.15 V_{CC}–0.05V		.3 1.4 BIAS+0.15	V

Note 1: Absolute maximum ratings are limits beyond which the life of the integrated circuit may be impaired. All voltages unless otherwise specified are measured with respect to ground.
Note 2: Limits are guaranteed by 100% testing, sampling, or correlation with worst-case test conditions.
Note 3: Low Duty cycle pulse testing is performed at T_A.
Note 4: This does not include the current from the AUI pull down resistors, the transmit pins TxTP+ and TxTP– or the LED output pins.
Note 5: LED drivers can sink up to 20mA, but V_{OL} will be higher.
Note 6: This current will result in a 2.5V peak output voltage on unshielded twisted pair cable when connected through an external filter and transformer as shown in Figure 12.

ELECTRICAL CHARACTERISTICS (Continued)

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
Transmit					
t_{TXNPW}	Transmit Turn-On Pulse Width		20		ns
t_{TXFPW}	Transmit Turn-Off Pulse Width		180		ns
t_{TXLP}	Transmit Loopback Startup Delay			100	ns
t_{TXODY}	Transmitter Turn-On Delay			100	ns
t_{TXSDY}	Transmit Steady State Prop. Delay		15	100	ns
t_{TXJ}	Transmitter Jitter		±2	±3.5	ns
Receive					
t_{RXODY}	Receive Turn-On Delay if Transmit is Idle		420	500	ns
t_{RXTDY}	Receive Turn-On Delay if Transmit is Active		650	800	ns
t_{RXFX}	Last Bit Received to Start Slow Decay Output	230	800		ns
t_{RXSDY}	Receive Steady State Prop. Delay		15	100	ns
t_{RXJ}	Receiver Jitter		±0.7	±1.5	ns
t_{AR}	Differential Output Rise Time 20% to 80% (Rx+/–, COL+/–)		3		ns
t_{AF}	Differential Output Fall Time 20% to 80% (Rx+/–, COL+/–)		3		ns
Collision					
t_{CPSQE}	Collision Present to SQE Assert	0		900	ns
t_{TXRX}	Time for Loopback to Switch from Tx to RxTP During a Collision	0		900	ns
t_{SQEXR}	Time for SQE to Deactivate Given That RxTP Goes Idle and TxTP Continues	0		900	ns
t_{SQEXT}	Time for SQE to Deactivate Given That TxTP Goes Idle and RxTP Continues	0		900	ns
t_{CLF}	Collision Frequency	8.5	10	11.5	MHz
t_{CLPDC}	Collision Pulse Duty Cycle	40	50	60	%
t_{SQEDY}	SQE Test Delay (Tx Inactive to SQE)	0.6	1.1	1.6	μs
t_{SQETD}	SQE Test Duration	0.5	1.0	1.5	μs
Jabber, Link Test and LED Timing					
t_{JAD}	Jabber Activation Delay	20	70	150	ms
t_{JRT}	Jabber Reset Unjab Time	250	450	750	ms
t_{JSQE}	Delay from Outputs Disabled to Collision Oscillator On		100		ns
t_{LLT}	Link Loss Time	50	95	150	ms
t_{LTN}	Link Test Pulse Receive Minimum Time	2	4.2	7	ms
t_{LTX}	Link Test Pulse Receive Maximum Time	25	70	150	ms
t_{TLP}	Link Test Pulse Repetition Rate	8	16	24	ms
t_{LTPW}	Link Test Pulse Width	85	100	130	ns
t_{LEDT}	$\overline{XMT}$, $\overline{RCV}$, $\overline{CLSN}$ On Time	30	100	300	ms

TIMING DIAGRAMS

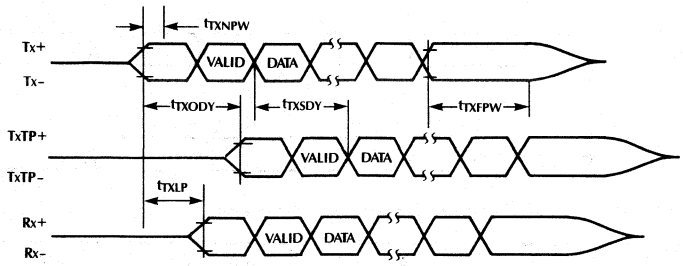


Figure 1. Transmit and Loopback Timing

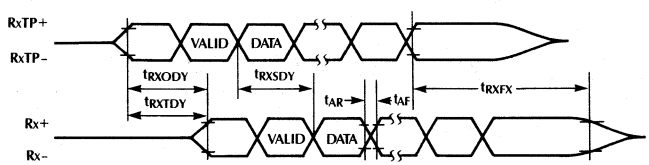


Figure 2. Receive Timing

TIMING DIAGRAMS (Continued)

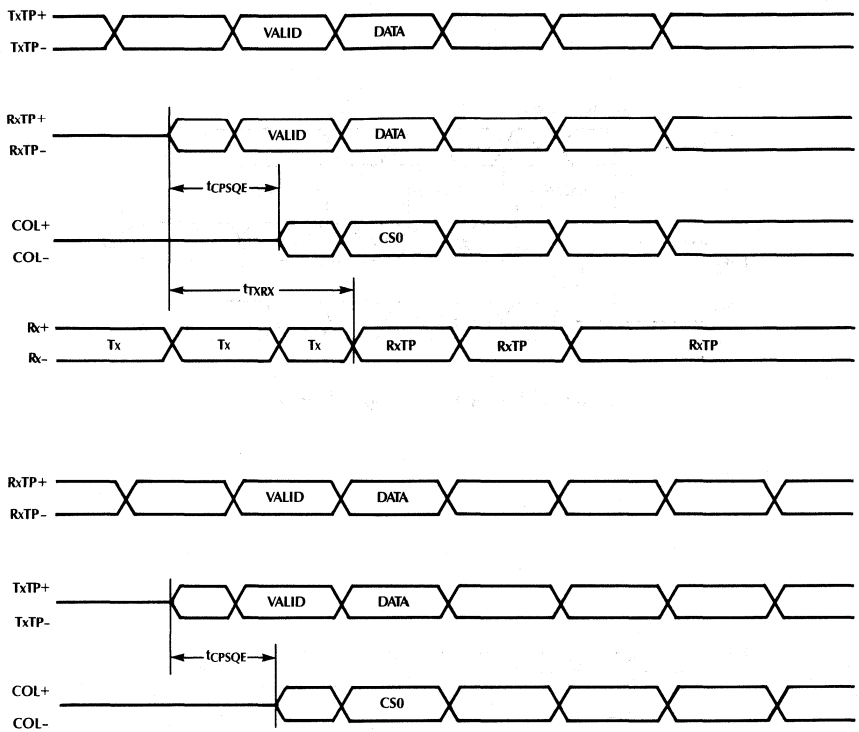


Figure 3. Collision Timing

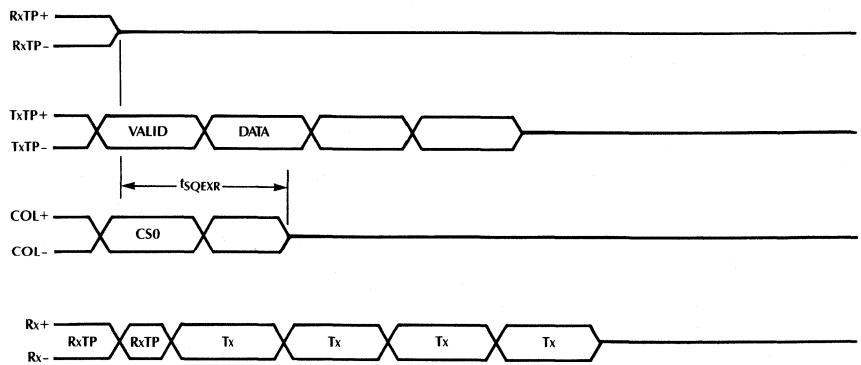


Figure 4. Collision Timing

TIMING DIAGRAMS (Continued)

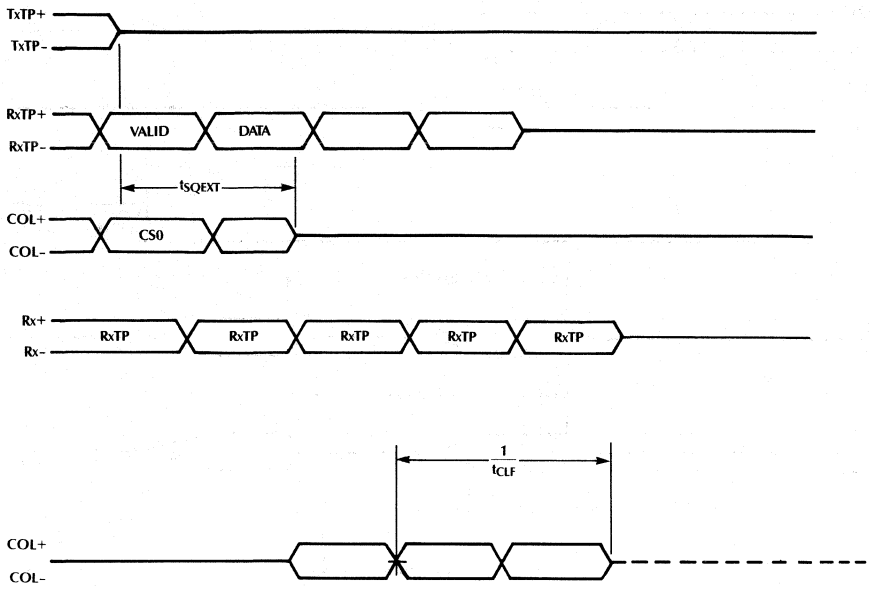


Figure 5. Collision Timing

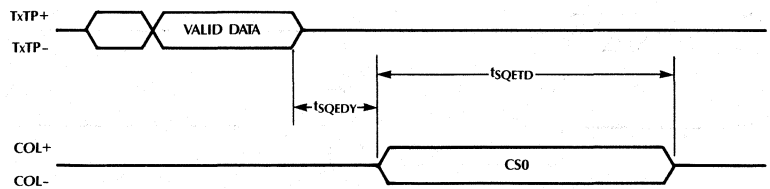


Figure 6. SQE Timing

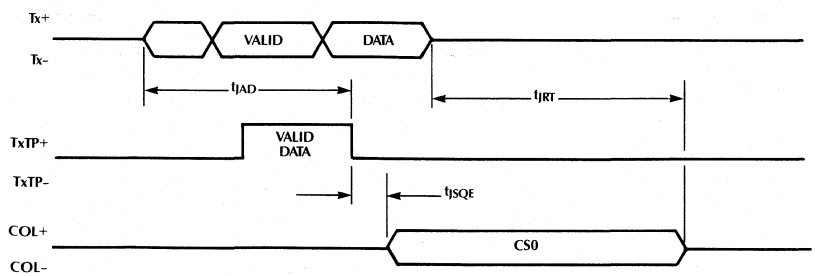


Figure 7. Jabber Timing

TIMING DIAGRAMS (Continued)

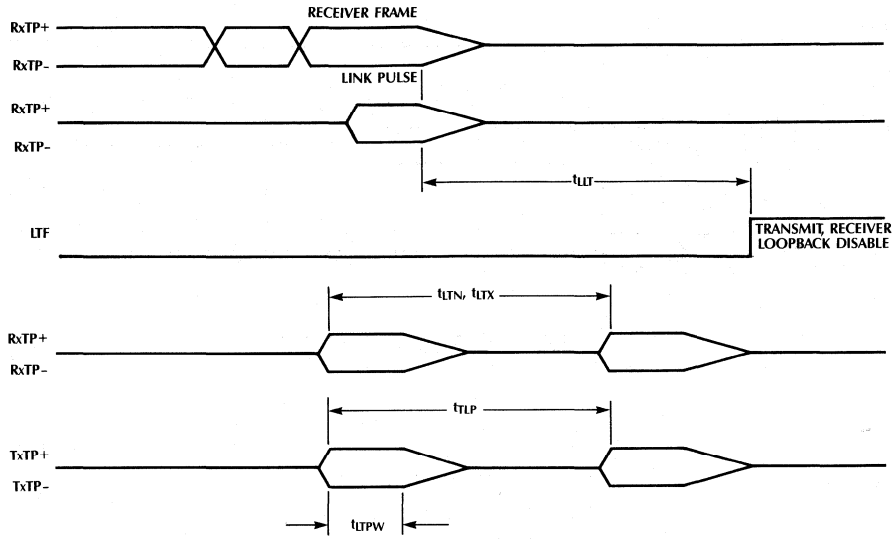


Figure 8. Link Pulse Timing

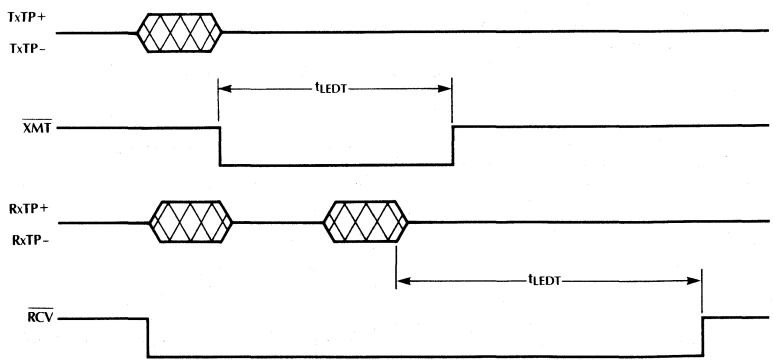


Figure 9. LED Timing

SYSTEM DESCRIPTION

Figure 10 shows a typical block diagram of an external 10BASE-T transceiver interface. On one side of the transceiver is the AU interface and the other is the twisted pair. The AU interface is AC coupled when used in an external transceiver or can be AC or DC coupled when used in an internal transceiver. The AU interface for an external transceiver includes isolation transformers, some biasing resistors, and a voltage converter for power.

The twisted pair side of the transceiver requires external transmit and receive filters, isolation transformers, and terminating resistors. These components can be obtained in a single hybrid package from suppliers listed in figure 12. The transmitter sends pre-equalized data through the transmit filters onto the twisted pair. The pre-equalized data uses a standard two step output waveform that lowers the amplitude of the 5MHz component so that at the receiving end both the 5MHz and 10MHz components have the same amplitude. The external transmit filter smooths the edges of the signal before passing it onto the twisted pair.

The receive pair side of the transceiver accepts the data after it passes through the isolation transformer and the receive low pass filter. Since this is an AC coupled input, the Bias pin is used to set the proper common mode voltage for the receive inputs. A pair of 50Ω resistors correctly terminate the receive pair and provide a common mode for the Bias voltage connection point.

AU INTERFACE

The AU interface consists of 3 pair of signals, DO, CI and DI as shown in Figure 10. The DO pair contains transmit data from the DTE which is received by the transceiver and sent out onto the twisted pair. The DI pair contains valid data that has been either received from the twisted pair or looped back from the DO and output through the DI pair to the DTE. The CI pair indicates whether a transmit based collision has occurred. It is an output that oscillates at 10MHz. CI pair is also used for Jabber and SQE Test.

The transceiver may be AC or DC coupled depending on the application. For the AC coupled interface, the DO input must be DC biased (shifted up in voltage) for the proper common mode input voltage. The BIAS pin serves this purpose. When DC coupled, the manchester encoder/decoder transmit output pair provides this common mode voltage and the Bias pin is not connected.

The two 39Ω 1% resistors tied to the Tx+ and Tx– pins serve two purposes. They provide a point to connect the common mode bias voltage, and they provide the proper matching termination for the AUI cable. The CI and DI pair, which are output drivers from the transceiver to the AUI cable, require 360Ω pull down resistors when terminated with a 78Ω load. However on a DTE card, CI and DI do not need 78Ω terminating resistors. This also means that the pull down resistors on CI and DI can be 1KΩ or greater depending upon the particular manchester encoder/decoder chip used.

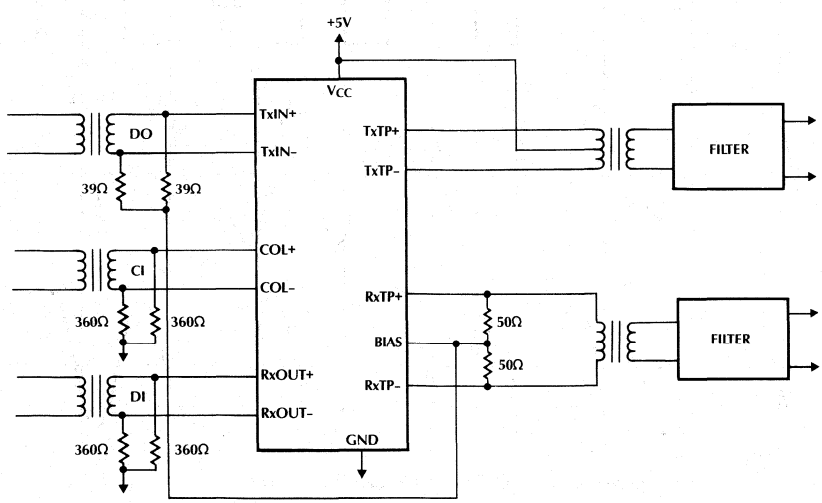


Figure 10. System Block Diagram

The AUI drivers are capable of driving the full 50 meters of cable length and have a rise and fall time of typically 3ns. The rise and fall times match to within 1ns. In the idle state, the outputs go to the same voltage to prevent DC standing current in the isolation transformers.

TRANSMISSION

The transmit function consists of detecting the presence of data from the AUI DO input (Tx+, Tx–) and driving that data onto the transmit twisted pair (TxTP+, TxTP–). A positive signal on the Tx+ lead relative to the Tx– lead of the DO circuit will result in a positive signal on the TxTP+ lead of the chip with respect to the TxTP– lead.

Before data will be transmitted onto the twisted pair from the AU interface, it must exceed the squelch requirements for the DO pair. The Tx squelch circuit serves the function of preventing any noise from being transmitted onto the twisted pair. This circuit rejects signals with pulse widths less than typically 20ns and voltage levels more positive than –175mV. Once the Tx squelch circuit has unsquelched, it looks for the start of idle signal to turn on the squelch circuit again. The transmitter turns on the squelch again when it receives an input signal at Tx+/– that is more positive than –175mV for more than approximately 180ns.

At the start of a packet transmission, no more than 2 bits are received from the DO circuit and not transmitted onto the twisted pair. The difference between start-up delays (bit loss plus steady-state propagation delay) for any two packets that are separated by 9.6μs or less will not exceed 200ns.

The output stage of the transmitter is a current mode switch which develops the output voltage by driving current through the terminating resistor and the output filter. The transmitter employs a center tap 2:1 transformer where the center tap is tied to V_{CC} (+5V). While one pin of the transmit pair (TxTP+, TxTP–) is pulled low, the other pin floats. The output pins to the twisted pair wires, TxTP+ and TxTP–, can drive a 100Ω, 150Ω load, or a variety of impedances that are characteristic of the twisted pair wire. RTSET selects the current into the TxTP+, TxTP– pins. This current along with the characteristic impedance of the cable determines the output voltage.

Once the characteristic impedance of the twisted pair is determined, one must select the appropriate RTSET resistor as well as match the terminating impedances of the transmit and receive filter. The RTSET resistor can be selected as follows:

$$RTSET = (R_L/100) * 220\Omega$$

where R_L is the characteristic impedance of the twisted pair cable.

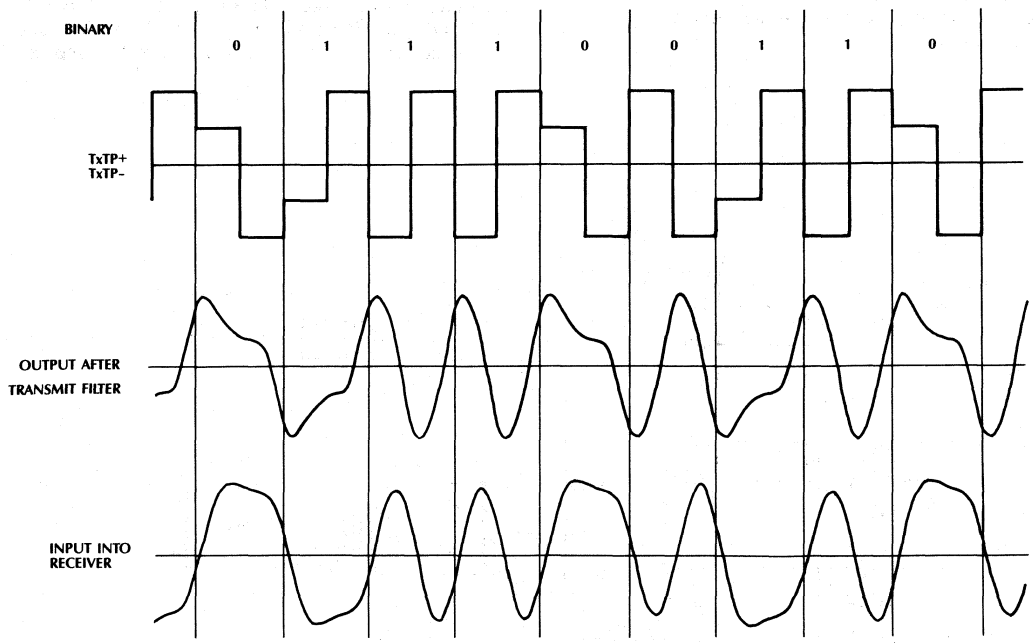


Figure 11. Transmit Pre-Equalization Waveform

The transmitter incorporates a pre-equalization circuit for driving the twisted pair line. Pre-equalization compensates for the amplitude and phase distortion introduced by the twisted pair cable. The twisted pair line will attenuate the 10MHz signal more than the 5MHz signal. Therefore pre-equalization insures that both the 5 and 10MHz components will be roughly the same amplitude at the far end receiver.

The pre-equalization circuit reduces the current output when a 5MHz bit is being transmitted. After 50ns of a 5MHz bit, the current level is reduced to approximately 2/3 of its peak for the remaining 50ns. Figure 11 illustrates the pre-equalization.

An on-chip one-shot determines the pulse width of the pre-equalized transmit signal. This requires an external capacitor connected to pins TxCAP0 and TxCAP1. The proper value for this one-shot is 330pF. Pre-equalization can be disabled by shorting TxCAP0 and TxCAP1 together.

The transmitter enters the idle state when it detects start of idle on Tx+ and Tx– input pins. The transmitter maintains a minimum differential output voltage of at least 450mV for 250ns after the last low to high transition. The driver differential output voltage will then be within 50mV of 0V within 45 bit times.

RECEPTION

The twisted pair receive data is transformer coupled and low pass filtered before it is fed into the input pins RxTP+/–. The input is differential with the common mode voltage set by the chip's Bias pin. At the start of packet reception from the twisted pair link, no more than 5 bits are received from the twisted pair cable and not transmitted onto the DI circuit. The first bit sent on the DI circuit may contain phase violations or invalid data, but all subsequent bits are valid.

The receive squelch will reject the following differential signals on the RxTP+ and RxTP– inputs:

1. All signals that produce a peak magnitude less than 300mV.
2. All continuous sinusoidal signals of amplitude less than $6.2V_{P\_P}$ and frequency less than 2MHz.
3. All single sinusoidal cycles of amplitude less than $6.2V_{P\_P}$ and either polarity, where the frequency is between 2MHz and 15MHz. For a period of 4 BT before and after this single cycle, the signal will conform to (1) above.
4. All sinusoidal cycles gated by a 100ns pulse gate of amplitude less than $6.2V_{P\_P}$ and either polarity, where the sinusoidal frequency is between 2MHz and 30MHz. The off time of the pulse gate on the sinusoidal signal shall be at least 400ns.

The first three receive squelch criteria are required to conform to the 10BASE-T standard. The fourth receive squelch criteria exceeds the 10BASE-T requirements and enhances the performance of the receiver. The fourth squelch criteria prevents a false unsquelch caused by cross talk or noise typically found coupling from the phone lines onto the receive twisted pair.

When the receive squelch is on during idle, the input voltage must exceed approximately ±450mV peak several times before unsquelch occurs. If the transmitter is inactive, the receiver has up to 5 bit times to unsquelch and output the receive data on the Rx+, Rx– pair. If the transmitter is active, the receive squelch extends the time it takes to determine whether to unsquelch. If the receiver unsquelches while the transmitter is active, a collision will result. Therefore the receive squelch uses the additional time to insure that a collision will not be reported as a result of a false receive squelch.

After the receiver is unsquelched, the detection threshold is lowered to 275mV. Upon passing the receive squelch requirements the receive data propagates into the multiplexer and eventually passes to the Rx+ and Rx– outputs of the AU interface. The addition of jitter through the receive section is no more than ±1.5ns.

While in the unsquelch state, the receive squelch circuit looks for the start of idle signal at the end of the packet. When start of idle is detected, receive squelch is turned on again. The proper start of idle occurs when the input signal remains above 300mV for 160ns. Nevertheless, if no transitions occur for 160ns, receive squelch is still turned on.

COLLISION

Whenever the receiver and the transmitter are active at the same time the chip will activate the collision output. The collision output is a differential square wave matching the AUI specifications and capable of driving a 78Ω load. The frequency of the square wave is 10MHz ± 15% with a 60/40 to 40/60 duty cycle. The collision oscillation turns on no more than 9 bit times after the collision condition begins, and turns off no more than 9 bit times after the collision condition is removed. The collision oscillator also is activated during SQE Test and Jabber.

LOOPBACK

The loopback function emulates a coax Ethernet transceiver where the transmit data sent by the DTE is looped back over the AUI receive pair. Many LAN controllers report the status of the carrier sense for each packet transmitted. The software can use this loopback information to determine whether a MAU is connected to the DTE by checking the status of carrier sense after each packet transmission.

When data is received by the chip while transmitting, a collision condition exits. This will cause the collision oscillator to turn on within 9 bit times. The data on the DI AUI pair (Rx+, Rx–) changes from Tx+, Tx– to RxTP+, RxTP–, when entering the collision state. During a collision, if the receive data (RxTP+, RxTP–) drops out before the transmit data (Tx+, Tx–), Rx+, Rx– will switch back to Tx+, Tx–.

SQE TEST FUNCTION (SIGNAL QUALITY ERROR)

The SQE test function allows the DTE to determine whether the collision detect circuitry is functional. After each transmission, during the inter-packet gap time, the collision oscillator will be activated for typically 1μs. The SQE test will not be activated if the chip is in the link fail state, or the Jabber state.

For SQE to operate, the SQEN pin must be tied to V_{CC} or BIAS. The SQE test can be disabled by tying the SQEN pin to 1.2V or ground. This allows the chip to be interfaced to a repeater.

JABBER FUNCTION

The Jabber function prevents a babbling transmitter from bringing down the network. Within the transceiver is a Jabber timer that starts at the beginning of each transmission and resets at the end of each transmission. If the transmission lasts longer than 20ms the jabber logic disables the transmitter, and turns on the collision oscillator COL+, COL–. When Tx+ and Tx– finally go idle, a second timer measures 0.5 seconds of idle on Tx+ and Tx– before re-enabling the transmitter and turning off the collision oscillator. If transmission starts up again before 0.5 seconds has expired, the timer is reset and measures another 0.5 seconds of idle time.

Even though the transmitter is disabled during jabber, Link Pulses are still transmitted if the Link Test is enabled.

Jabber can be disabled by placing 1.2V on the SQEN/LTD/JABD pin. This is useful for measuring jitter performance on the transmitter.

LINK TEST FUNCTION

Transmission — Whenever data is not being delivered to the twisted pair link, the idle signal is applied. The idle signal is a sequence of Link Pulses separated by a 16ms period of silence. The idle signal starts with a period of silence after a packet transmission ends. The link test pulse is a single high pulse with the same amplitude requirements as the data signal.

Reception — The transceiver monitors the receive twisted pair input for packet and link pulse activity. If neither a packet nor a link test pulse is received for 50 to 150ms, the transceiver enters the Link Test Fail state and inhibits transmission and reception. Link pulses received with the wrong polarity will be ignored and cause the chip to go into link test fail.

A DTE can determine that the transceiver is in Link Test Fail one of two ways: it can monitor the LTF pin if the transceiver is internal, or it can monitor loopback. If the MAU is on-board the LTF pin can be sampled to determine that the transceiver is in the link fail state. If the MAU is external the DTE can monitor carrier sense during transmission. A loss of carrier sense is an indication of Link Test Fail State, since in Link Test Fail, loopback is disabled. Note that jabber also disables loopback but with Jabber the collision signal will be on.

When a packet, or two consecutive link test pulses is received from the twisted pair input, the transceiver will exit the Link Test Fail state upon transmit and receive data being idle, and re-enable transmission and reception.

Link test pulses that do not occur within at most 25 to 150ms of each other are not considered consecutive. In addition, detected pulses that occur within a time between 2 to 7ms of a previous pulse will be considered as noise by the link test circuitry.

POLARITY CIRCUITRY

The ML4651 and ML4652 offer polarity detection, while the ML4657 and ML4658 offer automatic polarity correction. The ML4651 and ML4657 are pin for pin compatible, and so are the ML4652 and ML4658. The $\overline{\text{POLRD}}$ pin is used to report the status of the receive pair polarity. This pin reflects the true status of the receive polarity regardless of whether the part has autopolarity correction or not.

Polarity Detection — ML4651, ML4652 — The internal circuitry uses the start of idle signal to determine the receive polarity. With the correct receive polarity, the Start of Idle signal (the end of the frame) will remain above 300mV for more than 160ns. If the polarity is reversed, the Start of Idle signal will end with a negative voltage.

The $\overline{\text{POLRD}}$ status pin is updated only when two consecutive frames are received with the same Start of Idle polarity. In the case where the part is powered up with the receive polarity reversed and no frames are received, the part will go into link test fail without reflecting a reverse polarity condition. Without autopolarity correction, the part will remain in link test fail unless a frame is received or the correct polarity link pulses are received.

Automatic Polarity Correction — ML4657, ML4658 — In the link OK state, receive polarity is updated when two consecutive frames are received with the same Start of Idle polarity. In the Link Test Fail state the part will use either the Start of Idle signal or link pulses to correct the receive polarity.

In the case where the part is powered up with the receive polarity reversed and no frames are received, the part will go into Link Test Fail. After two link pulses are received with the same polarity, the part will exit Link Test Fail and correct the receive polarity. The POLRD pin will continue to reflect the true polarity of the receive pair.

LED DRIVERS

The ML4651, ML4657 have two LED driver pins. One is for Link Test Fail while the other is a reverse polarity indicator. The ML4652, ML4658 have four additional LED drivers for transmit, receive, collision, and jabber. The four additional LED driver pins are active low. The LEDs are normally off except for LTF which is normally on and active high. The LEDs are tied to their respective pins through a 510Ω resistor to 5 Volts.

The $\overline{XMT}$, $\overline{RCV}$ and $\overline{CLSN}$ pins have pulse stretchers on them which enables the LEDs to be visible. When transmission or reception occurs, the LED $\overline{XMT}$, $\overline{RCV}$ or $\overline{CLSN}$ status pins will activate low for 100ms. If another transmit, receive or collision condition occurs during the first 100ms, the LED timer will reset and begin timing again for 100ms. The LEDs will remain on for consecutive frames. The JAB, $\overline{POLRD}$, and LTF LEDs do not have pulse stretchers on them since their conditions occur long enough for the eye to see.

SEMI-STANDARD OPTION

The ML4651, ML4652, ML4657, and ML4658 are designed using Micro Linear's Bipolar Tile Array technology. They use a special Tile Array, the FB3651, that was designed for Data Communications applications. As a result these parts are customizable, and can be modified to suit a specific customer application. Please contact your local representative or Micro Linear for more information on semi-standard options.

APPLICATION: EXTERNAL MAU

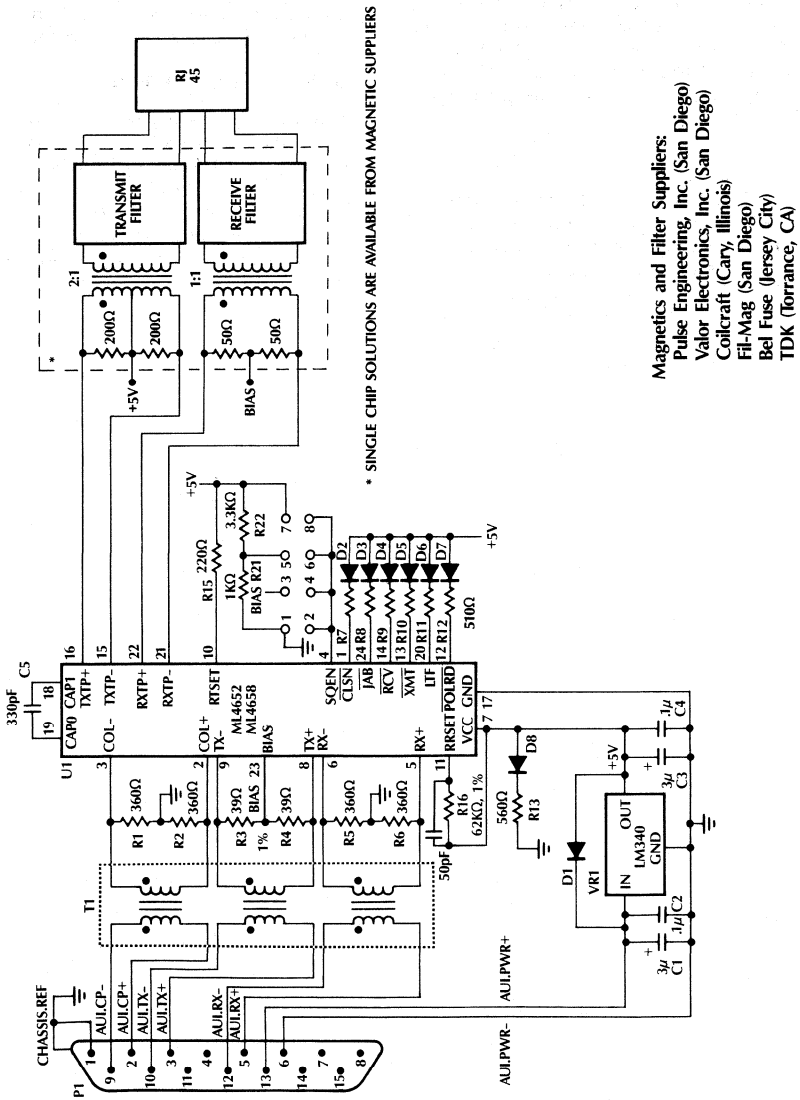


Figure 12. External MAU

APPLICATION: INTERNAL MAU

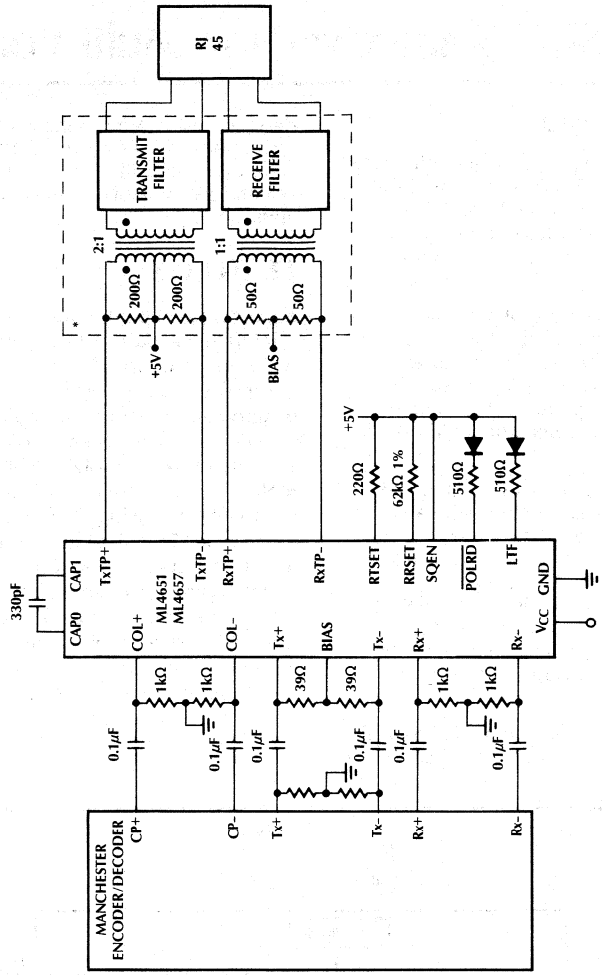


Figure 13. Internal MAU

ORDERING INFORMATION

ORDERING NUMBER	PACKAGE	PIN COUNT	AUTO-POLARITY
ML4651CP	Skinny DIP	20 pins	No
ML4652CP	Skinny DIP	24 pins	No
ML4657CP	Skinny DIP	20 pins	Yes
ML4658CP	Skinny DIP	24 pins	Yes
ML4652CQ	PLCC	28 pins	No
ML4658CQ	PLCC	28 pins	Yes

Micro Linear

ML4654

10BASE-T Transceiver for Multi-Port Repeaters

GENERAL DESCRIPTION

The ML4654 10BASE-T Transceiver is a single chip cable line driver/receiver that provides all of the functionality required to implement an internal 10BASE-T Transceiver for a Multi-Port Repeater. The ML4654 provides a TTL interface well suited for Multi-Port Repeater control logic.

The ML4654 uses a minimal number of external components, and fully conforms to the IEEE 802.3 10BASE-T standard. The transmitter offers a current driven output that is less sensitive to power supply variation and noise. It offers superior performance because of its highly symetrical switching which results in low RFI noise and low jitter.

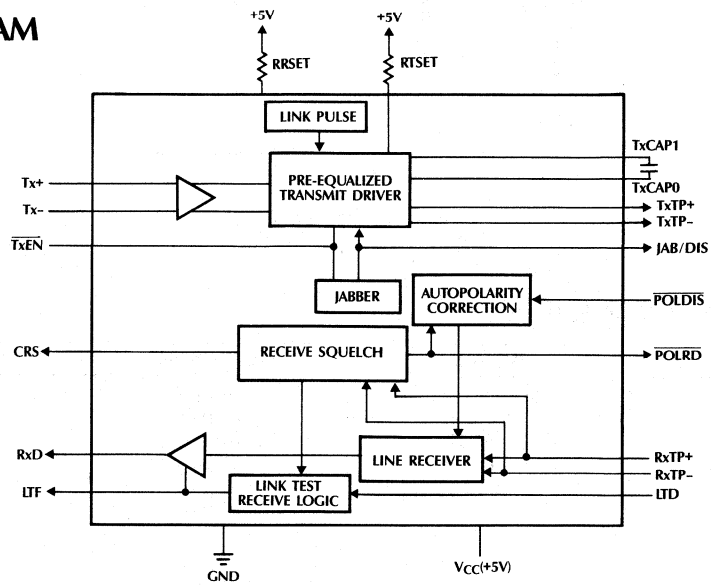
The Transceiver easily interfaces to 100Ω unshielded twisted pair cable, 150Ω shielded twisted pair cable, or a range of other characteristic impedances by changing one external resistor. Jabber and Link Test Function are fully integrated into the chip with enable/disable options. An autopolarity circuit detects the polarity of the receive pair and automatically corrects it if necessary. A polarity status pin that can drive an LED reflects the true polarity of the receive pair.

The ML4654 is available in a 20 pin skinny DIP as well as a surface mount 28 pin PLCC. The ML4654 is designed using Micro Linear's Bipolar Tile Array technology. It uses a special Tile Array designed for Data Communications applications. Semi-Standard options are available to suit a particular customer application.

FEATURES

- Complete implementation of IEEE 802.3 10BASE-T internal Medium Attachment Unit (MAU)
- TTL interface for direct connection to Multi-Port Repeater control logic
- Automatic polarity correction with a status pin to reflect the true receive polarity
- Single +5 volt supply ± 10%
- No clock or crystal required
- Capable of driving 100Ω unshielded twisted pair cable or 150Ω shielded twisted pair cable
- Fully integrated Link Test logic, with Link Test Fail Status pin and enable/disable option
- On-chip Jabber logic, with enable/disable option
- Available in a 20 pin skinny DIP or 28 pin PLCC
- Semi-standard option using Micro Linear's FB3651 LAN Transceiver Tile Array

BLOCK DIAGRAM

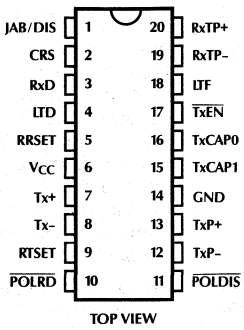


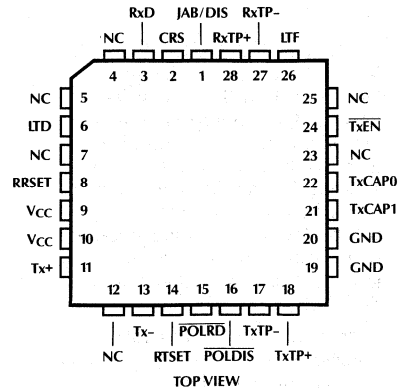
Micro Linear

PIN DESCRIPTION

PIN NO.	NAME	FUNCTION
1	JAB/DIS	Jabber Status Output/Jabber Disable. When this pin is tied to ground, the Jabber function is disabled and the transmitter is allowed to transmit indefinitely. This pin has an internal pullup so that when tied to a TTL input it will be low in the unjab state and high in the jab state. When in the jab state, the transmitter will be disabled.
2	CRS	Carrier Sense. Indicates valid receive data from the twisted pair. TTL output active high.
3	RxD	Receive data output to the local device. TTL levels.
4	LTD	Link Test Disable. When tied high or left to float, link test is disabled. When Link Test is disabled no link pulses are transmitted, and the transmitter and receiver will not be disabled as a result of a loss of receive link pulses. When this pin is grounded, link pulses will be transmitting during idle, and the link test receive logic is enabled.
5	RRSET	A 1% 61.9KΩ resistor tied from this pin to V_{CC} is used for biasing internal nodes.
6	V_{CC}	+5 Volt power input.
7	Tx+	Differential transmit data pair input from the local device, with TTL levels.
8	Tx–	
9	RTSET	When using 100Ω unshielded twisted pair cable, tie a 220Ω resistor between this pin and V_{CC}. When using 150Ω shielded twisted pair cable, tie a 330Ω resistor between this pin and V_{CC}.
10	$\overline{\text{POLRD}}$	Polarity Reversal Detection. This pin reflects the true receive polarity status regardless of the state of the autopolarity logic. A low indicates that RxTP+ and RxTP– are reversed. Open collector TTL output.
11	$\overline{\text{POLDIS}}$	Automatic Polarity Correction Disable. When grounded or left to float this pin will disable automatic polarity correction. The $\overline{\text{POLRD}}$ status pin continues to reflect the status of the receive polarity, even when automatic polarity is disabled. When this pin is tied high, automatic polarity correction is enabled.
12	TxTP–	Pre-equalized differential balanced output driver. These outputs are connected to terminating resistors, a transformer and a balanced transmit output filter. The output current is set with an external resistor connected to RTSET allowing the chip to drive 100Ω unshielded twisted pair, 150Ω shielded twisted pair cables or a range of other characteristic impedances.
13	TxTP+	
14	GND	Ground reference.
15	TxCAP1	An external capacitor of 330pF is tied between these two pins to set the pulse width for the pre-equalization on the transmitter. If these two pins are shorted together, no pre-equalization occurs.
16	TxCAP0	
17	$\overline{\text{TxEn}}$	When this pin is low the transmitter is enabled and transmitting the data received from the Tx+/– input pair. TTL input-active low.
18	LTF	Link Test Fail. Active high. Normally this pin is low, indicating that the link is operational. If the link goes down resulting from the absence of link pulses and frames being received, the chip will go into the Link Test Fail state and bring LTF high. In the Link Test Fail state, both the transmitter and receiver are disabled, however link pulses are still sent. This pin is low when Link Test is disabled.
19	RxTP–	Twisted Pair Receive Data Input. When this signal exceeds the receive squelch requirements the receive data is buffered and sent to the RxD output pin.
20	RxTP+	

PIN CONNECTION





ABSOLUTE MAXIMUM RATINGS
(Note 1)

Power Supply Voltage Range
V_{CC} ..... -0.3 to 6V
Input Voltage Range ..... -0.3 to V_{CC}
Input Current 60mA
Output Current
TxTP+, TxTP- 80mA
Storage Temperature (Tj) ..... 135°C
Lead Temperature (Soldering 10 seconds) ..... 300°C

OPERATING CONDITIONS
(Note 2)

Supply Voltage (V_{CC}) ..... 5V ± 10%
LED on Current 10mA
RRSET ..... 61.9KΩ ± 1%
RTSET ..... 220Ω or 330Ω ± 1%
TxCAP 330pF

ELECTRICAL CHARACTERISTICS
Unless otherwise specified T_A = 0°C to 70°C (Note 3), V_{CC} = 5V ± 10%

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Power Supply Current I_{CC} (Note 4)	V_{CC} = 5V			120	mA
TTL Inputs:					
V_{IL}				.8	V
V_{IH} (LTD, $\overline{TxEN}$)		2			V
TTL Outputs:					
V_{OL}	I_{OL} = 1.6mA			.4	V
V_{OH} (CRS, RxD, LTF)	I_{OH} = -400μA	2.4			V
LED Drivers:					
V_{OL} (JAB/DIS, $\overline{POLRD}$)	R_L = 510Ω (Note 5)			0.8	V
Transmit Peak Output Current	RTSET = 220Ω		42 (Note 6)		mA
Differential Input Voltage (RxTP+, RxTP-)		±0.300		±3.1	V
Receiver Input Resistance		10			KΩ
Receive Squelch Voltage Level (RxTP+, RxTP-)		300	450	585	mVp

Note 1: Absolute maximum ratings are limits beyond which the life of the integrated circuit may be impaired. All voltages unless otherwise specified are measured with respect to ground.
Note 2: Limits are guaranteed by 100% testing, sampling, or correlation with worst-case test conditions.
Note 3: Low Duty cycle pulse testing is performed at T_A.
Note 4: This does not include the current supplied into the transmit pins TxTP+ and TxTP-.
Note 5: LED drivers can sink up to 20mA, but V_{OL} will be higher.
Note 6: This current will result in a 2.5V peak output voltage on unshielded twisted pair cable when connected through an external filter and transformer as shown in Figure 5.

ELECTRICAL CHARACTERISTICS (Continued)

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
Transmit					
t_{TXEN}	Transmit Enable to Data Out			100	ns
t_{TXDIS}	Transmit Disable to Start Slow Decay			50	ns
t_{TXSDY}	Transmit Steady State Prop. Delay		15	100	ns
t_{TXJ}	Transmitter Jitter			±2	ns
Receive					
t_{RXOCR}	Valid Receive Data to CRS Turn-On			500	ns
t_{RXTCR}	Valid Receive Data to CRS Turn-On if Transmit is Active			800	ns
t_{RXSDY}	Receive Steady State Prop. Delay		15	100	ns
t_{RXFCR}	Receive Turn-Off to CRS Inactive	150	230	300	ns
t_{RXJ}	Receiver Jitter			±1.5	ns
t_{AR}	Rx Output Rise Time 20% to 80%		4		ns
t_{AF}	Rx Output Fall Time 20% to 80%		4		ns
Jabber, Link Test and LED Timing					
t_{JAD}	Jabber Activation Delay	20	70	150	ms
t_{JRT}	Jabber Reset Unjab Time	250	450	750	ms
t_{JJAB}	Delay from Outputs Disabled to JAB/DIS Active		-20		ns
t_{LLT}	Link Loss Time	50	95	150	ms
t_{LTN}	Link Test Pulse Minimum Time	2	4.2	7	ms
t_{LTX}	Link Test Pulse Maximum Time	25	70	150	ms
t_{LTPW}	Link Test Pulse Width	85	100	130	ns
t_{TLP}	Link Pulse Repetition Rate	8	16	24	ms

TIMING DIAGRAMS

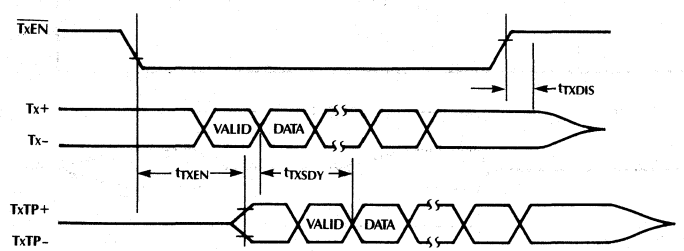


Figure 1. Transmit Timing

TIMING DIAGRAMS (Continued)

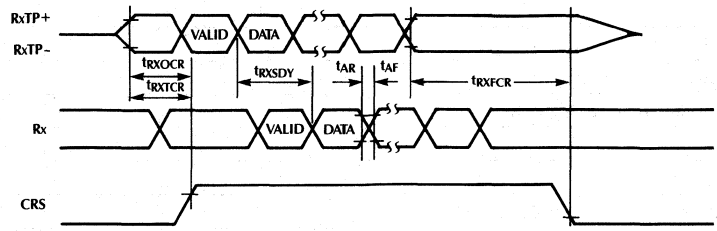


Figure 2. Receive Timing

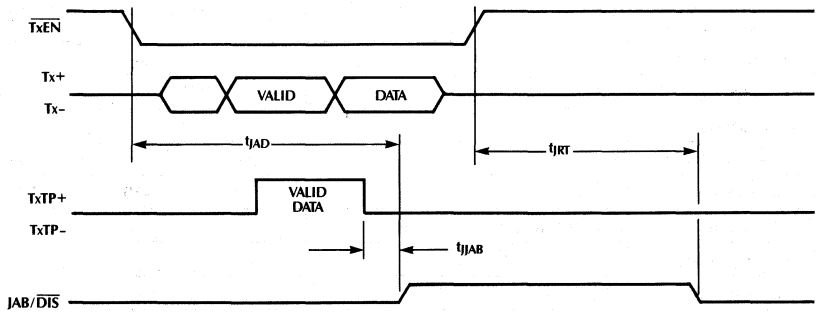


Figure 3. Jabber Timing

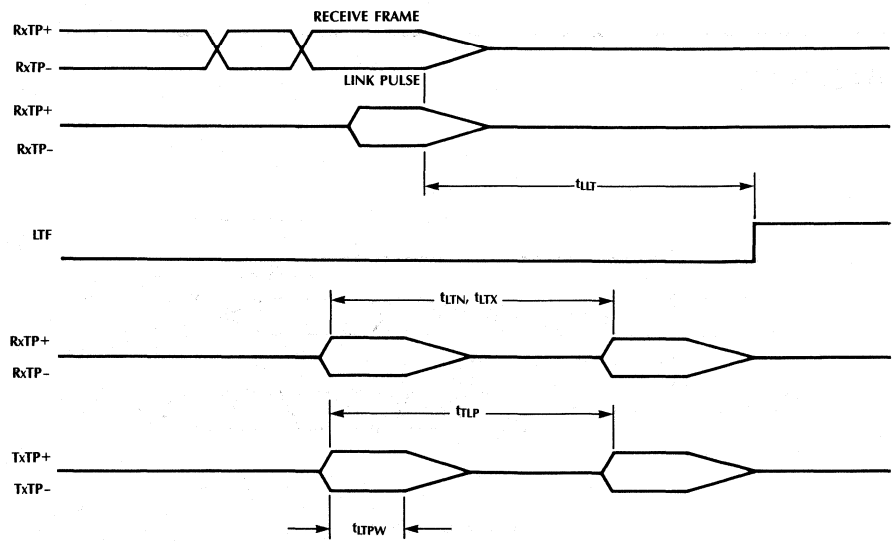


Figure 4. Link Pulse Timing

FUNCTIONAL DESCRIPTION

Figure 5 shows a typical block diagram of the ML4654 in an internal 10BASE-T transceiver interface. On one side of the transceiver is the local controller interface and the other is the twisted pair. The twisted pair side of the transceiver requires external transmit and receive filters, isolation transformer, and termination resistors.

The transmitter sends pre-equalized data through the transmit filters onto the twisted pair. The pre-equalized data uses a standard two step output waveform that lowers the amplitude of the 5MHz component so that at the receiving end both the 5MHz and 10MHz components have the same amplitude. The external transmit filter smooths the edges of the transmitter's output before passing it onto the twisted pair. Figure 6 illustrates the transmit output waveforms at different stages of the system.

The receive pair side of the transceiver accepts the data after it passes through the isolation transformer and the receive low pass filter. Since this is an AC coupled input, an internal DC bias is used to set the proper common mode voltage for the receive inputs.

LOCAL INTERFACE

The local interface consists of transmit, and receive signals which all use TTL levels. The transmit input signals entail a pair of true differential TTL transmit data pins, and an enable signal.

Once the transmitter is enabled, the output on TxTP+, TxTP– is determined by the transmit input pair Tx+, Tx–. The transmit input pair is a true differential TTL input that determines the switching point based on both inputs. Driving this input single ended is also possible by letting Tx– float. After the last bit is transmitted, Tx+ should be held high and Tx– held low for two bit times before TxEn goes high.

During reception the carrier sense pin (CRS) is activated asynchronously to receive data. Receive data is output through the receive data output pin (RxD). At the end of the packet, CRS goes inactive two bit times after the last low to high transition on RxD.

TRANSMISSION

The transmit function consists of enabling the transmitter with TxEn and driving the data onto the transmit twisted pair (Tx+, Tx–). A positive signal on the Tx+ lead relative to the Tx– lead results in a positive signal on the TxTP+ lead of the chip with respect to the TxTP– lead.

At the start of a packet transmission, no more than 1 bit is received from the Tx+, Tx– circuit and not transmitted onto the twisted pair. The difference between start-up delays (bit loss plus steady-state propagation delay) for any two packets that are separated by 9.6μs or less will not exceed 200ns.

The output stage of the transmitter is a current mode switch which develops the output voltage by driving current through the terminating resistor. The transmitter employs a center tap 2:1 transformer where the center tap is tied to V_{CC} (+5V). While one pin of the transmit pair is pulled low, the other pin floats.

The output pins to the twisted pair wires, TxTP+ and TxTP–, drive a 100Ω load, 150Ω load, or a variety of impedances that are characteristic of the twisted pair wire. To select the correct drive current for a characteristic impedance of the twisted pair wire, one must select the appropriate RTSET resistor. The RTSET resistor can be determined as follows:

$$RTSET = (R_L/100) * 220\Omega$$

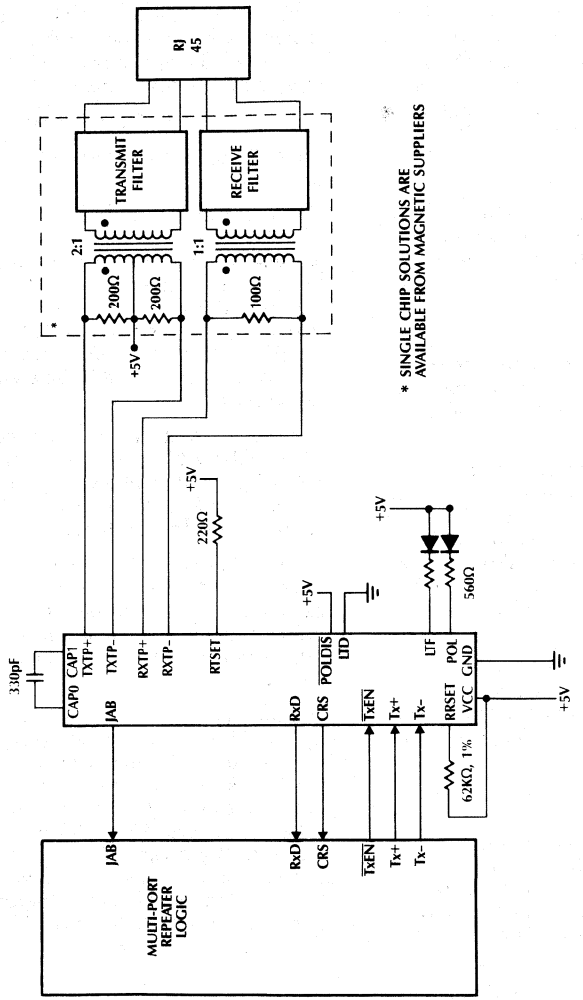
where R_L is the characteristic impedance of the twisted pair cable.

The transmitter incorporates a pre-equalization circuit for driving the twisted pair line. Equalization of the transmit signal is needed to decrease the voltage of the 5MHz component of the Manchester encoded signal. The twisted pair line will decrease the voltage of the 10MHz signal more than the 5MHz signal. Therefore the pre-equalization insures that both the 5 and 10MHz components will have the same amplitude at the far end receiver.

The pre-equalization circuit reduces the output current when a 5MHz bit is being transmitted. After 50ns of a 5MHz bit, the current level is reduced to approximately 2/3 of its peak for the remaining 50ns. Figure 6 illustrates the pre-equalization.

An on-chip one-shot determines the pulse width of the pre-equalized transmit signal. This requires an external capacitor connected to pins TxCAP0 and TxCAP1. The proper value for this capacitor is 330pF. Pre-equalization can be disabled by shorting TxCAP0 and TxCAP1 together.

The transmitter enters the idle state when it is disabled by TxEn. The Tx+ pin should remain high and the Tx– pin should remain low or float for two bit times before the TxEn signal goes high. When this happens, the transmitter maintains a minimum differential output voltage of at least 450mV for two bit times after the last low to high transition. The driver's differential output voltage will then be within 40mV of 0V within 80 bit times. In addition the current into the load will be limited in magnitude to 4mA within 80 bit times.



Magnetics and Filter Supplies:
Pulse Engineering, Inc. (San Diego)
Valor Electronics, Inc. (San Diego)
Coilcraft (Cary, Illinois)
Fil-Mag (San Diego)
Bel Fuse (Jersey City)
TDK (Torrance, CA)

Figure 5. System Block Diagram

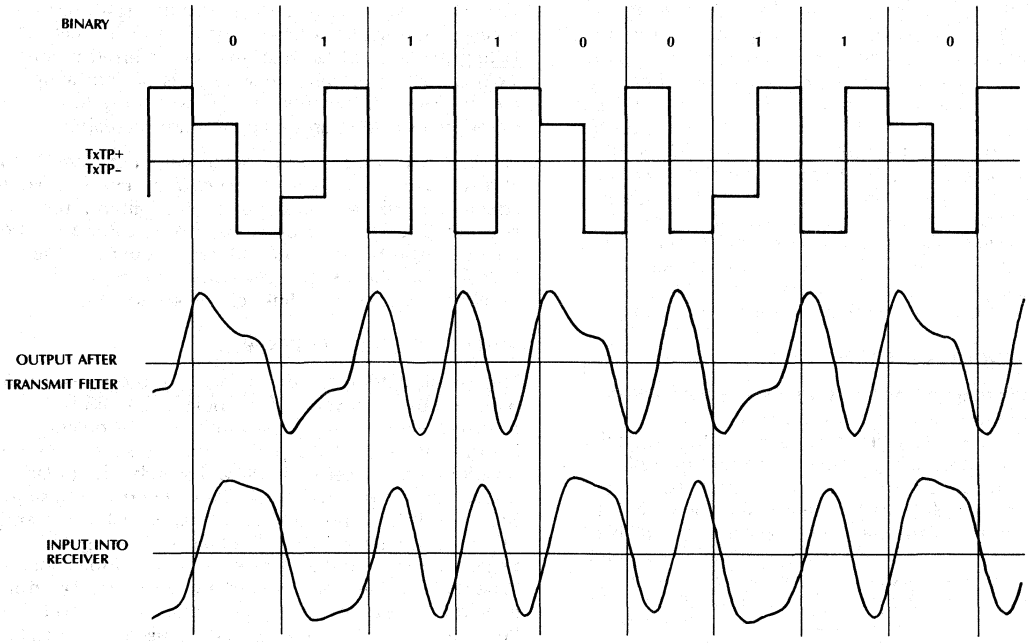


Figure 6. Transmit Output Waveforms

RECEPTION

Before the twisted pair receive data is input into the transceiver it is transformer coupled and low pass filtered. The RxTP+/– input is differential with the common mode voltage set internally at approximately halfway between V_{CC} and GND. At the start of a packet reception from the twisted pair link, no more than 5 bits are received from the twisted pair cable and not transmitted onto the Rx pin. The first bit sent to Rx may contain phase violations or invalid data, but all subsequent bits are valid.

The receive squelch will reject the following differential signals on the RxTP+ and RxTP– inputs:

1. All signals that produce a peak magnitude less than 300mV.
2. All continuous sinusoidal signals of amplitude less than $6.2V_{P-P}$ and frequency less than 2MHz.
3. All single sinusoidal cycles of amplitude less than $6.2V_{P-P}$ and either polarity, where the frequency is between 2MHz and 15MHz. For a period of 4 BT before and after this single cycle, the signal will conform to (1) above.
4. All sinusoidal cycles gated by a 100ns pulse gate of amplitude less than $6.2V_{P-P}$ and either polarity, where the sinusoidal frequency is between 2MHz and 30MHz. The off time of the pulse gate on the sinusoidal signal shall be at least 400ns.

The first three receive squelch criteria are required to conform to the 10BASE-T standard. The forth receive squelch criteria exceeds the 10BASE-T requirements. It enhances the receiver's performance without compromising on conformance to the standard. The additional squelch criteria prevents a false unsquelch from occuring due to cross talk or noise typically coming from the telephone system twisted pair wires.

When the receive squelch is on, the input voltage must exceed ±450mV peak several times before unsquelch occurs. If the transmitter is inactive, the receiver has up to 5 bit times to unsquelch and output the receive data on the Rx+, Rx– pair. If the transmitter is active, the receive squelch extends the time it takes to determine whether to unsquelch. If the receiver unsquelches while the transmitter is active, a collision will result. Therefore the receive squelch uses the additional time to insure that a collision will not be reported as a result of a false receive squelch.

After the receiver is unsquelched, the data detection threshold is lowered to 275mV. Upon passing the receive squelch requirements the receive data propagates to the Rx TTL output. This TTL output has been bolstered to reduce jitter. The addition of jitter through the receive section is no more than ±1.5ns.

While in the unsquelch state, the receive squelch circuit looks for the start of idle signal at the end of the packet. When start of idle is detected, receive squelch is turned on again and the carrier sense pin goes inactive. The proper start of idle occurs when the input signal remains above 300mV for 160ns. Nevertheless if no transitions occur for 160ns, receive squelch is still turned on. In this case however, the polarity may be reversed. A reverse polarity condition will be registered into the autopolarity circuit if the start of idle signal is negative. It will take several reverse polarity start of idle signals and/or reverse polarity link pulses to actually change the polarity on the receive circuit. (See Automatic Polarity Reversal section for more detail)

JABBER FUNCTION REQUIREMENTS

The Jabber function prevents a babbling transmitter from bringing down the network. Within the transceiver is a Jabber timer that starts at the beginning of each transmission and resets at the end of each transmission. If the transmission last longer than 20ms the jabber logic disables the transmitter, and activates the JAB/DIS pin, signaling the controller of the jabber condition. When Tx+ and Tx– finally go idle, a second timer measures 0.5 seconds of idle on Tx+ and Tx– before re-enabling the transmitter and deactivating the JAB/DIS pin. If transmission starts up again before the 0.5 seconds has expired, the timer is reset and measures another 0.5 seconds of idle time. Even though the transmitter is disabled during jabber, Link Pulses are still transmitted.

The Jabber function can be disabled by tying the JAB/DIS pin to ground. This forces the ML4654 into the Unjab state allowing indefinite transmission.

LINK TEST FUNCTION

Transmission — Whenever data is not being delivered to the twisted pair link, the idle signal is used. The idle signal is a sequence of link pulses separated by 16ms of silence. The idle signal starts with a 16ms period of silence after a packet transmission ends. The link test pulse is a single high pulse which meets the amplitude requirements for a pulse of duration BT.

Reception — The transceiver monitors its twisted pair input for packet and link pulse activity. If neither a packet nor a link test pulse is received for 50 to 150ms, the transceiver enters the Link Test Fail state and inhibits transmission and reception. The Hub Controller can determine that the transceiver is in the Link Test Fail state by monitoring the LTF pin. If LTF is low, the link is operational. But if LTF goes high, the ML4654 has entered the Link Test Fail state as a result of a loss of both Link Pulses and Receive Frames.

When a packet, or two consecutive link test pulses is received, the transceiver will exit the link test fail state. Exiting the link test fail state may be deferred if either TxEn is high or the receive squelch is off indicating receive data activity. After the link test fail state is exited, transmission and reception are re-enabled.

Link test pulses that do not occur within at most 25 to 150ms of each other are not considered consecutive. In addition, a Link Test Pulse that occurs within a time between 2 to 7ms of a previous Link Test Pulse will be considered as noise by the link test circuitry. In the Link Test Fail state, such pulses reset the counted number of consecutive link test pulses to zero.

AUTOMATIC POLARITY REVERSAL

This circuit determines the polarity for the receive pair only, and decides whether the polarity should be reversed. After 240ms of consistent reverse polarity information, the POLRD pin will change states and the polarity on the receive circuit will switch. The polarity on the receive pair RxTP+, RxTP– is determined using both Link Pulses and the Start of Idle signal at the end of a receive packet. When the Start of Idle signal is negative, it is treated as a reverse polarity indication. When a Link Pulse begins with a negative transition it is treated as a reverse polarity indication. When both Link Pulses and/or Start of Idle signals consistently indicate a reverse polarity condition for 240ms, the polarity on the receiver will be reversed.

The $\overline{\text{POLRD}}$ pin will reflect the true polarity on the receive pair regardless of the automatic correction circuit. For example if the polarity on the receive pair is reversed, after 240ms the $\overline{\text{POLRD}}$ pin will go low and the data on the RxD pin will have the correct polarity. This condition will remain as long as the polarity stays reversed. If the reverse polarity is then corrected, after 240ms the $\overline{\text{POLRD}}$ pin will go high and the RxD pin will have the correct polarity.

The $\overline{\text{POLDIS}}$ pin will disable the automatic polarity correction but have no affect on the $\overline{\text{POLRD}}$ pin. Therefore when $\overline{\text{POLDIS}}$ pin is tied low and the polarity is reversed on the receive pair, after 240ms the $\overline{\text{POLRD}}$ pin will go low, but the RxD will continue to pass the data on in the reverse polarity condition.

If the ML4654 is powered up with the RxTP+/– polarity reversed, and no data is received, it will go into link test fail. After 240ms of reverse polarity information, the auto-polarity circuit will reverse the polarity. The link test circuitry will then receive two correct polarity link pulses, and exit the link test fail state.

ORDERING INFORMATION

ORDERING NUMBER	PACKAGE	PIN COUNT
ML4654CP	Skinny DIP	20 pins
ML4654CQ	PLCC	28 pins

Micro Linear

ML4661

FOIRL Transceiver

GENERAL DESCRIPTION

The ML4661 FOIRL transceiver combined with the ML4621 or ML4622 fiber optic quantizers provides all of the functionality required to implement both an internal and external IEEE 802.3 FOIRL MAU. The ML4661 offers a standard IEEE 802.3 AU interface that allows it to be directly connected to industry standard manchester encoder/decoder chips or an AUI cable.

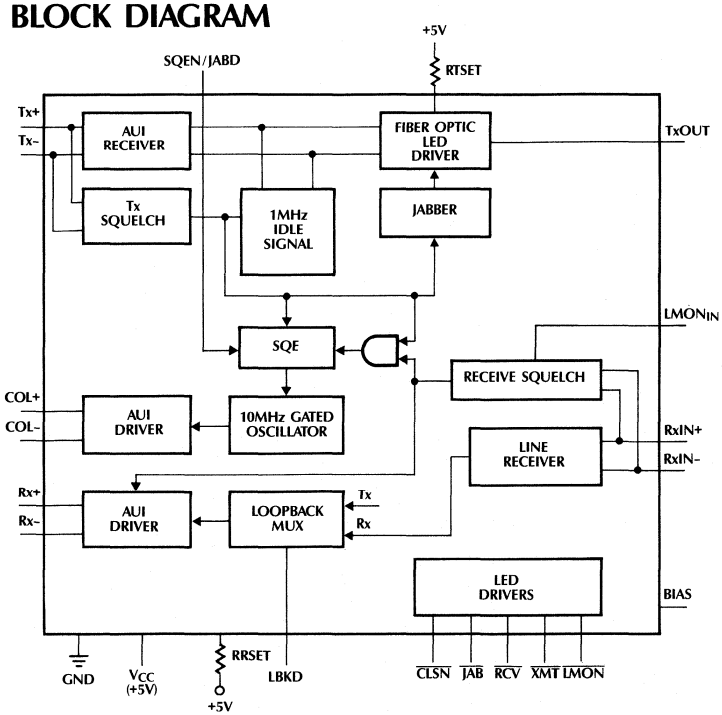
The ML4661 provides a highly integrated solution that requires a minimal number of external components, and conforms to the IEEE 802.3 FOIRL standard. The transmitter offers a current driven output that directly drives a fiber optic LED transmitter. Jabber, 1MHz idle signal, and SQE Test are fully integrated onto the chip.

The receiver accepts an ECL level input coming from the ML4621 or ML4622 fiber optic quantizers. The 1MHz idle signal is removed and the AUI output is activated when the receive squelch criteria is exceeded. A Link Monitor function is also provided for low light detection.

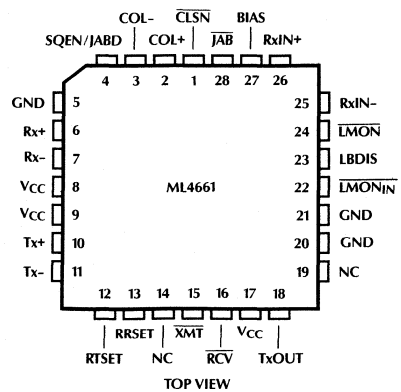
FEATURES

- Combined with the ML4621 or ML4622, offers a complete implementation of an FOIRL Medium Attachment Unit (MAU)
- Incorporates an AU interface for use in an external MAU or an internal MAU
- Single +5 volt supply ± 10%
- No crystal or clock required
- On-chip Jabber, 1MHz idle, and SQE Test with enable/disable option
- Five network status LED outputs
- Available in a 28-pin PLCC package
- Semi-standard option using Micro Linear's FB3651 LAN Transceiver Tile Array

BLOCK DIAGRAM



PIN CONNECTION



PIN DESCRIPTION

PIN #	NAME	FUNCTION
1	$\overline{\text{CLSN}}$	Indicates that a collision is taking place. Active low LED driver, open collector. Event is extended with internal timer for visibility.
2	COL+	Gated 10MHz oscillation used to indicate a collision, SQE test, or jabber. Balanced differential line driver outputs that meet AUI specifications.
3	COL–	
4	SQEN/JABD	SQE Test Enable, Jabber Disable. When tied low, SQE test is disabled, when tied high SQE test is enabled. When tied to BIAS both SQE test and Jabber are disabled.
5	GND	Ground Reference.
6	Rx+	Manchester encoded receive data output to the local device. Balanced differential line driver outputs.
7	Rx–	
8	V_{CC}	+5 Volt power input.
9	V_{CC}	
10	Tx+	Balanced differential line receiver inputs that meet AUI specifications. These inputs may be transformer, AC or DC coupled. When transformer or AC coupled, the BIAS pin is used to set the common mode voltage.
11	Tx–	
12	RTSET	Sets the current driven out of the transmitter.
13	RRSET	A 1% 61.9 KΩ resistor tied from this pin to V_{CC} sets the biasing currents for internal nodes.
14	NC	No Connection.
15	$\overline{\text{XMT}}$	Indicates that transmission is taking place. Active low LED driver, open collector. Event is extended with internal timer for visibility.
16	$\overline{\text{RCV}}$	Indicates that the transceiver is receiving a frame from the optical input. Active low LED driver, open collector. Event is extended with internal timer for visibility.
17	V_{CC}	+5 volt supply.
18	TxOUT	Fiber optic LED driver output.
19	NC	No Connection.
20	GND	Ground Reference.
21	GND	Ground Reference.
22	$\overline{\text{LMON}}_{\text{IN}}$	Link Monitor Input from the ML4621 or ML4622. This input must be low (active) for the receiver to unsquelch.
23	LBDIS	Loopback Disable. When this pin is tied to V_{CC}, the AUI transmit pair data is not looped back to the AUI receive pair. When this pin is tied to GND (normal operation), the AUI transmit pair data is looped back to the AUI receiver pair.
24	$\overline{\text{LMON}}$	Link Monitor LED status output. This pin is pulled low when $\overline{\text{LMON}}_{\text{IN}}$ input is low and there are transitions on RxIN± indicating an idle signal or active data. If either $\overline{\text{LMON}}_{\text{IN}}$ goes high or transitions cease on RxIN±, $\overline{\text{LMON}}$ will go high. Active low LED driver, open collector.
25	RxIN+	Fiber Optic receive pair. This ECL level signal is received from the ML4621 or ML4622 fiber optic quantizer. When this signal exceeds the receive squelch requirements, and the $\overline{\text{LMON}}_{\text{IN}}$ input is low, the receive data is buffered and sent to the AUI receive outputs.
26	RxIN–	
27	BIAS	BIAS output voltage for the AUI Tx+, Tx– inputs when they are AC coupled.
28	$\overline{\text{JAB}}$	Jabber network status LED. When in the Jabber state, this pin will be low and the transmitter will be disabled. In the Jabber "OK" state this pin will be high. Open collector TTL output.

4

ABSOLUTE MAXIMUM RATINGS
(Note 1)

Power Supply Voltage Range
- V_{CC} ..... -0.3 to 6V

Input Voltage Range
- Digital Inputs (SQEN, $LMON_{IN}$, LBDIS) ..... -0.3 to V_{CC}
- Tx+, Tx–, RxIN+, RxIN– ..... -0.3 to V_{CC}

Input Current
- RRSET, RTSET, $\overline{JAB}$, $\overline{CLSN}$, $\overline{XMT}$, $\overline{RCV}$, $\overline{LMON}$ 60mA

Output Current
- TxOUT 80mA

Storage Temperature ..... -65° C to +150°C

Lead Temperature (Soldering 10 seconds) ..... 260°C

OPERATING CONDITIONS
(Note 2)

Supply Voltage (V_{CC}) ..... 5V ± 10%

LED on Current 10mA

RRSET ..... 61.9KΩ ± 1%

RTSET ..... 162Ω ± 1%

ELECTRICAL CHARACTERISTICS
Unless otherwise specified, T_A = -30°C to 85°C, V_{CC} = 5V ± 10% (Note 3)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Power Supply Current I_{CC}: Idle While Transmitting	 V_{CC} = 5V (Note 4)			 170 200	 mA
LED Drivers: V_{OL}	 R_L = 510Ω (Note 5)			 0.8	 V
Transmit Peak Output Current	RTSET = 162Ω		57		mA
Transmit Squelch Voltage Level (Tx+, Tx–)		-140	-170	-190	mV
Common Mode Input Voltage (Tx±, RxIN±)		2		V_{CC} - 0.5	V
Receive Squelch Voltage Level (RxIN+, RxIN–)			±175		mV-p
Differential Output Voltage (Rx±, COL±)		±550		±1200	mV
Common Mode Output Voltage (Rx±, COL±)			4.0		V
Differential Output Voltage Imbalance (Rx±, COL±)				±40	mV
BIAS Voltage			3.2		V
SQE/JABD	SQE Test Disable Jabber Disable Both Enabled	 BIAS - .15 V_{CC} - 0.05		.3 BIAS + .15	V
LBDIS Threshold	Disabled Enabled	V_{CC} -0.10		 1	V

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
Transmit					
t_{TXNPW}	Transmit Turn-On Pulse Width		20		ns
t_{TXFPW}	Transmit Turn-Off Pulse Width from Data to Idle	400		2100	ns
t_{TXLP}	Transmit Loopback Startup Delay			500	ns
t_{TXODY}	Transmitter Turn-On Delay			100	ns
t_{TXIDF}	Transmit Idle Frequency	0.85		1.25	MHz
t_{TXDC}	Transmit Idle Duty Cycle	45		55	%
t_{TXSDY}	Transmit Steady State Propagation Delay		15	50	ns
t_{TXJ}	Transmitter Jitter into 31Ω Load			±1.5	ns
Receive					
t_{RXSFT}	Receive Squelch Frequency Threshold	1.3		4	MHz
t_{RXODY}	Receive Turn-On Delay			350	ns
t_{RXFX}	Last Bit Received to Slow Decay Output	230	800		ns
t_{RXSDY}	Receive Steady State Propagation Delay		15	50	ns
t_{RXJ}	Receiver Jitter			±1.5	ns
t_{AR}	Differential Output Rise Time 20% to 80% (Rx±, COL±)		4		ns
t_{AF}	Differential Output Fall Time 20% to 80% (Rx±, COL±)		4		ns
Collision					
t_{CPSQE}	Collision Present to SQE Assert	0		450	ns
t_{SQEXR}	Time for SQE to Deactivate After Collision	450		700	ns
t_{CLF}	Collision Frequency	8.5		11.5	MHz
t_{CLPDC}	Collision Pulse Duty Cycle	40	50	60	%
t_{SQEDY}	SQE Test Delay (Tx Inactive to SQE)	0.6		1.6	µs
t_{SQETD}	SQE Test Duration	0.5	1.0	1.5	µs
Jabber and LED Timing					
t_{JAD}	Jabber Activation Delay	20	70	150	ms
t_{JRT}	Jabber Reset Unjab Time	250	450	750	ms
t_{JSQE}	Delay from Outputs Disabled to Collision Oscillator On		100		ns
t_{LEDTRC}	$\overline{RCV}$, $\overline{CLSN}$ On Time	20		70	ms
t_{LEDTT}	$\overline{XMIT}$ On Time	8		30	ms
t_{LLPH}	Low Light Present to LMON High	3		6	µs
t_{LLCL}	Low Light Clear to LMON Low	1		6	ms

Note 1: Absolute maximum ratings are limits beyond which the life of the integrated circuit may be impaired. All voltages unless otherwise specified are measured with respect to ground.
Note 2: Limits are guaranteed by 100% testing, sampling, or correlation with worst-case test conditions.
Note 3: Low Duty Cycle pulse testing is performed at T_A.
Note 4: This does not include the current from the AUI pull down resistors, or LED status outputs.
Note 5: LED drivers can sink up to 20mA, but V_{OL} will be higher.

SYSTEM DESCRIPTION

Figure 1 shows a typical block diagram of the ML4661 in an internal or external FOIRL MAU. On one side of the transceiver is the AU interface and the other is the fiber optic interface. The AU interface is AC coupled when used in an external transceiver or can be AC or DC coupled when used in an internal transceiver. The AU interface for an external transceiver includes isolation transformers, some biasing resistors, and a voltage regulator for power.

The fiber optic side of the transceiver requires an external fiber optic transmitter, fiber optic receiver, and the ML4621 or ML4622 fiber optic quantizers. The transmitter uses a current driven output that directly drives the fiber optic transmitter. The receive side of the transceiver accepts the data after passing through the fiber optic receiver and the ML4621/ML4622 fiber optic quantizer.

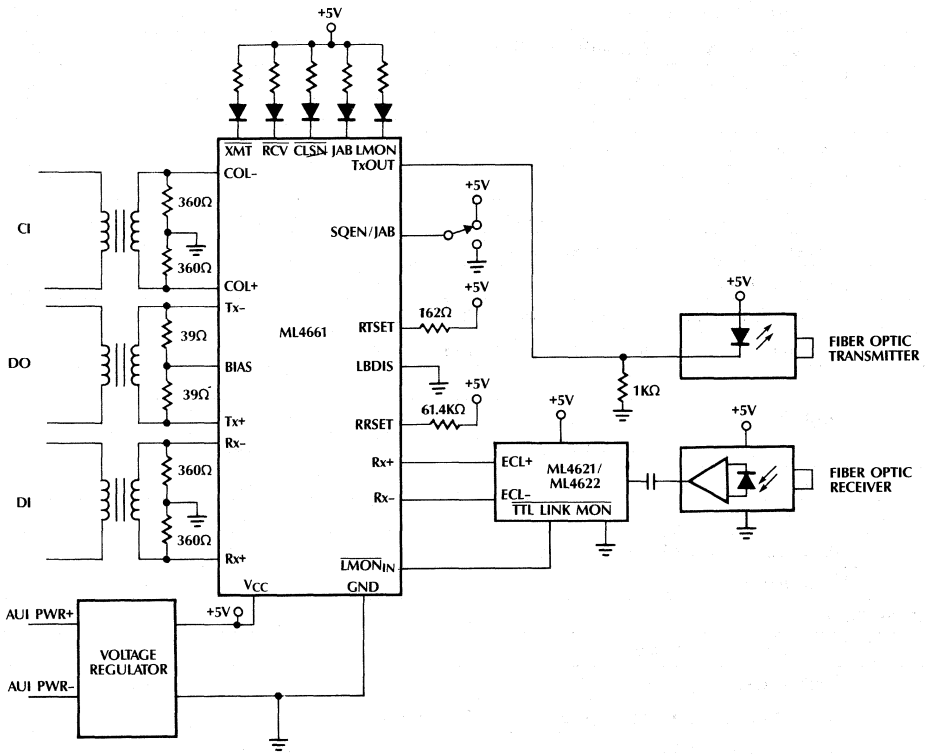


Figure 1. FOIRL System Block Diagram

AUI INTERFACE

The AUI interface consist of 3 pair of signals, DO, CI and DI as shown in figure 1. The DO pair contains transmit data from the DTE which is received by the transceiver and sent out onto the fiber optic cable. The DI pair contains valid data that has been either received from the fiber optic cable or looped back from the DO and output through the DI pair to the DTE. The CI pair indicates whether a collision has occurred. It is an output that oscillates at 10MHz if a collision Jabber or SQE Test has taken place, otherwise it remains idle.

When the transceiver is external, these three pair are AC coupled through isolation transformers, while an internal transceiver may be AC or DC coupled. For the AC coupled interface, DO which is an input must be DC biased (shifted up in voltage) for the proper common mode input voltage. The BIAS pin serves this purpose. When DC coupled, transmit output pair coming from the serial interface provides this common mode voltage and the BIAS pin is not connected.

The two 39Ω 1% resistors tied to the Tx+ and Tx– pins serve two purposes. First they provide a point to connect the common mode bias voltage as discussed above, and they provide the proper matching termination for the AUI cable. The CI and DI pair, which are output from the transceiver to the AUI cable, require 360Ω pull down resistors when terminated with a 78Ω load. However on a DTE card, CI and DI do not need 78Ω terminating resistors. This also means that the pull down resistors on CI and DI can be 1KΩ or greater depending upon the particular manchester encoder/decoder chip used. Using higher value pull down resistors as in a DTE card will save power.

The AUI drivers are capable of driving the full 50 meters of cable length and have a rise and fall time of typically 3ns. In the idle state, the outputs go to the same voltage to prevent DC standing current in the isolation transformers.

TRANSMISSION

The transmit function consists of detecting the presence of data from the AUI DO input (Tx+, Tx–) and driving that data onto the fiber optic LED transmitter. A positive signal on the Tx+ lead relative to the Tx– lead of the DO circuit will result in no current, hence the fiber optic LED is in a low light condition. When Tx+ is more negative than Tx–, the ML4661 will sink current into the chip and the LED will light up.

Before data will be transmitted onto the fiber optic cable from the AUI interface, it must exceed the squelch requirements for the DO pair. The Tx squelch circuit serves the function of preventing any noise from being transmitted onto the twisted pair. This circuit rejects signals with pulse widths less than typically 20ns (negative going), or with levels less than –175mV. Once Tx squelch circuit has unsquelched, it looks for the start of idle signal to turn on the squelch circuit again. The transmitter turns on the squelch again when it receives an input signal at TxIN± that is more positive than –175mV for more than approximately 180ns.

At the start of a packet transmission, no more than 1 bit is received from the DO circuit and not transmitted onto the fiber optic cable. The difference between start-up delays (bit loss plus steady-state propagation delay) for any two packets that are separated by 9.6μs or less will not exceed 200ns.

The output stage of the transmitter is a current mode switch which develops the output light by sinking current through the LED into the TxOUT pin. Once the current requirement for the LED is determined, the RTSET resistor is selected. The following equation is used to select the correct RTSET resistor:

$$RTSET = \left(\frac{42mA}{I_{OUT}} \right) 220\Omega$$

The transmitter enters the idle state when it detects start of idle on Tx+ and Tx– input pins. After detecting the start of idle the transmitter switches to a 1MHz output idle signal.

RECEPTION

The input to the transceiver comes from the ECL outputs of the ML4621 or ML4622. At this point it is a clean digital ECL signal. At the start of packet reception no more than 3.5 bits are received from the twisted pair cable and not transmitted onto the DI circuit. The receive squelch will reject frequencies lower than 1.3MHz and input voltage less than ±175mV. The receive squelch will also reject any receive input if the $\overline{LMON}_{IN}$ pin is high.

While in the unsquelch state, the receive squelch circuit looks for the start of idle signal at the end of the packet. Start of idle occurs when the input signal remains idle for more than 160ns. When start of idle is detected, the receive squelch circuit returns to the squelch state and the start of idle signal is output on the DI circuit (Rx+, Rx–).

COLLISION

Whenever the receiver and the transmitter are active at the same time the chip will activate the collision output. The collision output is a differential square wave matching the AUI specifications and capable of driving a 78Ω load. The frequency of the square wave is 10MHz ± 15% with a 60/40 to 40/60 duty cycle. The collision oscillation turns on no more than 4.5 bit times after the collision condition begins, and turns off between 4.5 and 7 bit times after the collision condition is removed. The collision oscillator also is activated during SQE Test and Jabber.

LOOPBACK

The loopback function emulates an Ethernet (10BASE-5) transceiver whereby the transmit data sent by the DTE is looped back over the AUI receive pair. Some LAN controllers use this loopback information to determine whether a MAU is connected by monitoring the carrier sense while transmitting. The software can use this loopback information to determine whether a MAU is connected to the DTE by checking the status of carrier sense after each packet transmission.

When data is received by the chip while transmitting, a collision condition exits. This will cause the collision oscillator to turn on within 4.5 bit times. The data on the DI pair will remain with the DO pair until DO goes idle. At this point DI will switch to RxIN if it is still active, or DI will go idle if RxIN is idle. After a collision is detected, the collision oscillator will remain on until either DO or RxIN go idle. The exception to this is when DO starts, then RxIN starts, then DO stops, then RxIN stops. In this case the collision oscillator will remain on until RxIN goes idle according to the IEEE FOIRL standard.

Loopback can be disabled by strapping LBDIS to V_{CC}.

SQE TEST FUNCTION (SIGNAL QUALITY ERROR)

The SQE test function allows the DTE to determine whether the collision detect circuitry is functional. After each transmission, during the inter packet gap time, the collision oscillator will be activated for typically 1μs. The SQE test will not be activated if the chip is in the low light state, or the jabber on state.

For SQE to operate, the SQEN pin must tied to V_{CC}. This allows the MAU to be interfaced to a DTE. The SQE test can be disabled by tying the SQEN pin to ground, for a repeater interface.

JABBER FUNCTION REQUIREMENTS

The Jabber function prevents a babbling transmitter from bringing down the network. Within the transceiver is a Jabber timer that starts at the beginning of each transmission and resets at the end of each transmission. If the transmission last longer than 20ms the jabber logic disables the transmitter, and turns on the collision signal COL+, COL–. When Tx+ and Tx– finally go idle, a second timer measures 0.5 seconds of Even though the transmitter is disabled during jabber, the 1MHz idle signal is still transmitted.

LED DRIVERS

The ML4661 has five LED drivers. The LED driver pins are active low, and the LEDs are normally off. The LEDs are tied to their respective pins through a 500Ω resistor to 5 Volts.

The $\overline{XMT}$, $\overline{RCV}$ and $\overline{CLSN}$ pins have pulse stretchers on them which enables the LEDs to be visible. When transmission or reception occurs, the LED $\overline{XMT}$, $\overline{RCV}$ or $\overline{CLSN}$ status pins will activate low for several milliseconds. If another transmit, receive or collision conditions occurs before the timer expires, the LED timer will reset and restart the timing. Therefore rapid events will leave the LEDs continuously on. The JAB and LTF LEDs do not have pulse stretchers on them since their conditions occur long enough for the eye to see.

LOW LIGHT CONDITION

The $\overline{LMON}$ LED output is used to indicate a low light condition. LMON is activated low when both $LMON_{IN}$ is low and there are transitions on RxIN± less than 3μs apart. If either one of these conditions do not exist, LMON will go high.

TIMING DIAGRAMS

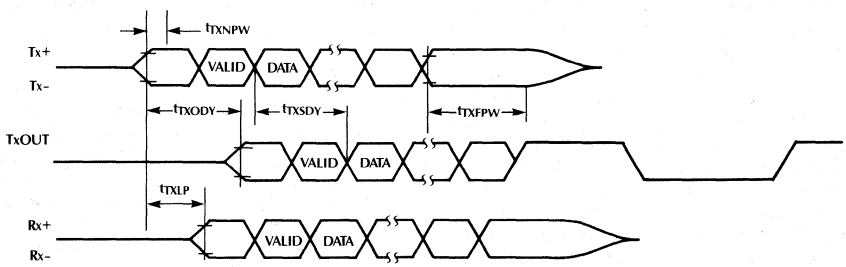


Figure 2. Transmit and Loopback Timing

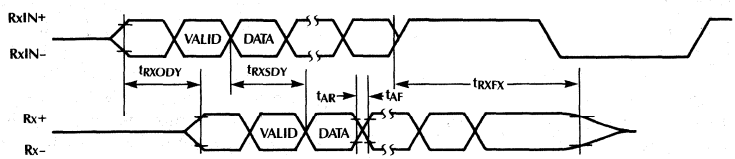


Figure 3. Receive Timing

TIMING DIAGRAMS (Continued)

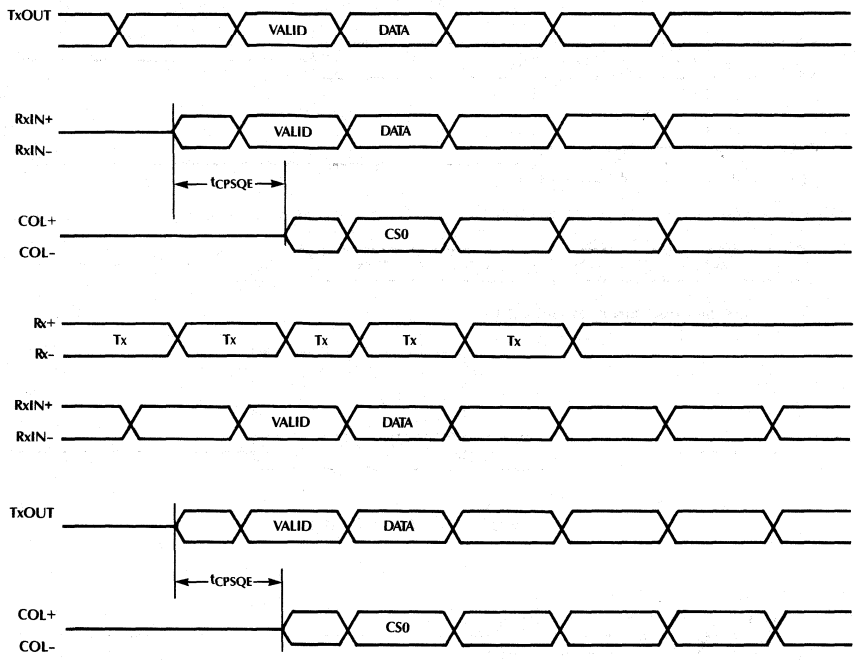
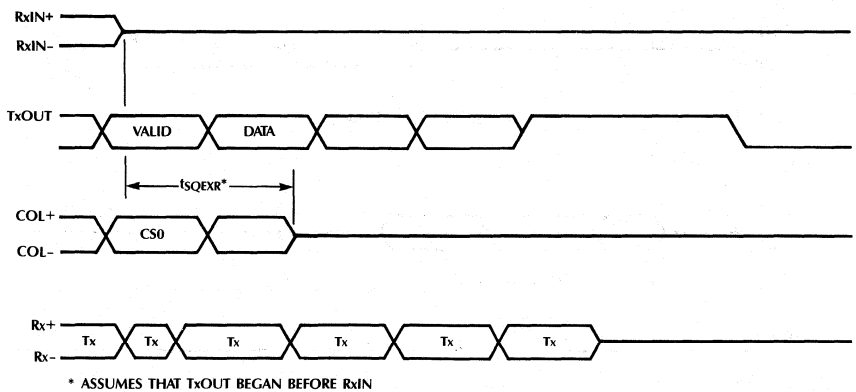


Figure 4. Collision Timing



* ASSUMES THAT TxOUT BEGAN BEFORE RxIN

Figure 5. Collision Timing

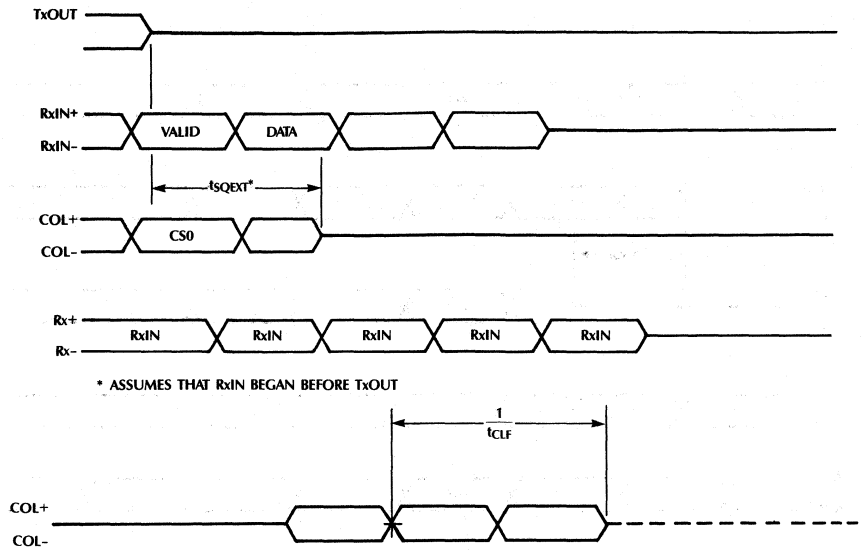


Figure 6. Collision Timing

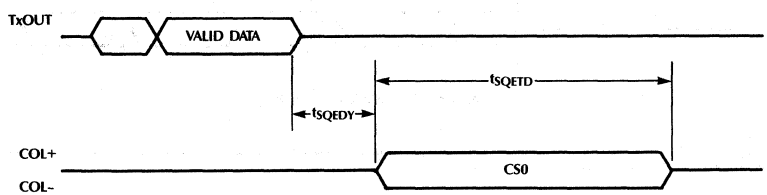


Figure 7. SQE Timing

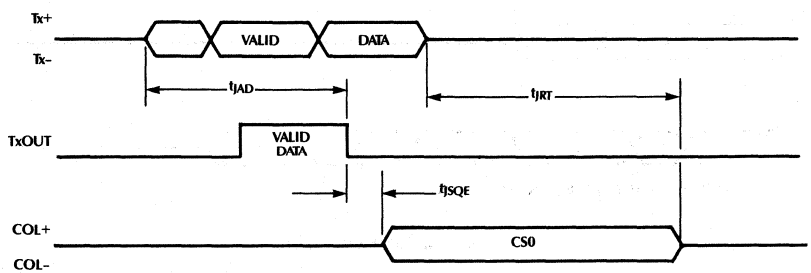


Figure 8. Jabber Timing

TIMING DIAGRAMS (Continued)

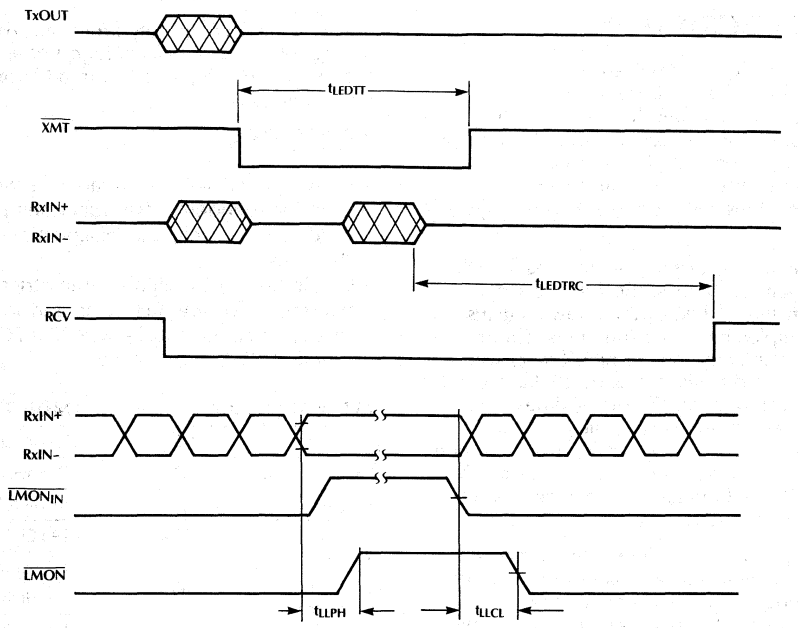


Figure 9. LED Timing

ORDERING INFORMATION

PART NUMBER	PIN COUNT	PACKAGE
ML4661CQ	28 Pins	Molded PCC

LAN Transceiver Array

GENERAL DESCRIPTION

The FB3651 is an application focused tile array intended for local area network transceiver applications. This array was developed using Micro Linear's proprietary mini tile architecture. This mini tile approach combined with our 12 volt, 1 GHz technology allows high complexity and high speed, cost effective LAN Transceiver circuits to be easily integrated.

The array consists of two distinct sections each with different component groupings, the first section, situated mostly in the middle of the array, contains custom cells to implement timer functions. These custom cells can implement up to nine timers with outputs that span from milliseconds up to 1/2 second with no external components. The long times are accomplished by generating very small yet stable currents that charge on chip capacitors. The remainder of the die area has general purpose mini-tiles for the other analog and digital circuit functions common to LAN transceiver applications.

The design of the FB3651 LAN Transceiver array is optimized for the circuit building blocks required to implement the function of a local area network transceiver. Examples of the types of circuits possible are: high speed transmitters and receivers, transmit and receive squelch, oscillators, diagnostic and fault protection circuits, LED drivers, and other similar type circuits.

This very high complexity array can realize up to 12 analog functional blocks, 6 high frequency/digital blocks, and 150 digital gates, in addition to the nine timer functions.

FEATURES

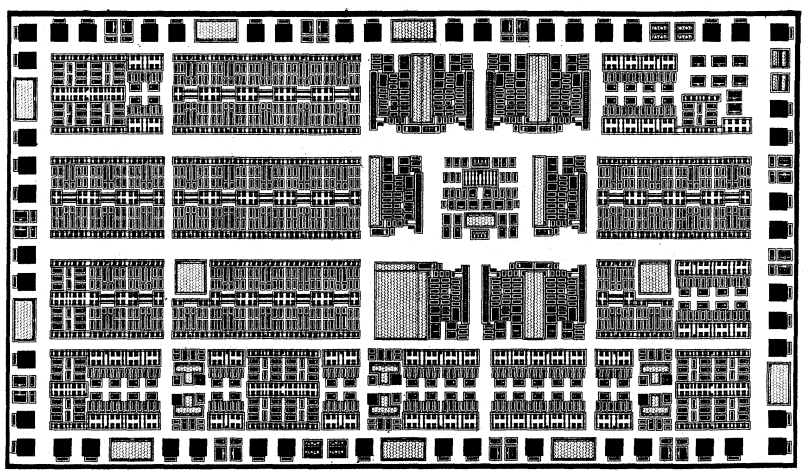
- Array optimized for local area network transceivers
- Nine independent timer functions possible for deadman, squelch, and diagnostic functions (1–500ms)
- Can implement a highly symmetrical current driven transmitter for low RFI noise and low jitter
- 18 analog circuit blocks with 150 ECL gates
- 12 volt, 1 GHz technology

ARRAY SUMMARY

NPN Transistors	1424
PNP Transistors	152
Schottky Transistors	20
Total Diffused Resistance	1020K
Total Implant Resistance	5432K
Total MOS Capacitance	310pF
Total Components	4242
Bond Pads	50

MINI TILE SUMMARY

T1 General	58
T2 Specialized	6
T7 High Frequency	17
T9 ECL Logic	50
T12 Schottky Peripheral	10
T13 High Frequency	3
Timer Cells	9
Timer Bias	1



FB3651 — LAN Transceiver Array

Disk Drive ICs

Section 5

Disk Drive Component Selection Guide

1. Read/Write Amplifiers

Part Number	Number of Channels	Head Type	Max Input Noise (nV/√Hz)	Write Current Range (mA)	Key Feature	Package Options
ML117	2, 4 or 6	Ferrite	2.1	10 to 50	Write Current Disable Function	PDIP-18, 22, 28; SO-18, 24; PCC-28
ML117R	2, 4 or 6	Ferrite	2.1	10 to 50	Internal Damping Resistors	PDIP-18, 22, 28; SO-18, 24; PCC-28
ML501	6 or 8	Ferrite	1.5	10 to 50	Enhanced Write Stability	PDIP-28, 40; SO-32; PCC-28, 44
ML501R	6 or 8	Ferrite	1.5	10 to 50	ML501 with Internal Damping Res.	PDIP-28, 40; SO-28, 32; PCC-28, 44
ML502	6 or 8	Thin Film	1.5	10 to 50	Enhanced Write Stability	PDIP-28, 40; SO-32; PCC-28, 44
ML502R	6, 7 or 8	Thin Film	1.5	10 to 50	ML502 with Internal Damping Res.	PDIP-28, 40; SO-32; PCC-28, 44
ML511	4, 6 or 8	Ferrite	1.5	10 to 40	Improved Write Stability	SO-24; PCC-28, 44
ML511R	4, 6, 7 or 8	Ferrite	1.5	10 to 40	ML511 with Internal Damping Res.	SO-24; PCC-28, 44
ML4415	15	Ferrite	1.5	10 to 40	Improved Write Current Stability	PCC-44
ML4416	14	Ferrite	1.5	10 to 40	Chip Select Input	PCC-44

2. Read/Write Signal Processing

Part Number	Function	Key Feature	Package Options
ML4025	Data Separator for RLL (1, 7) Code	33 MBits/sec Data Rate	PDIP-24, PCC-28
ML4041	Read Data Processor	Fast AGC Recovery, 1 ns Pulse Pairing	PDIP-24, SO-24, PCC-28
ML4042	ML4041 with Undervoltage Detector	Fast AGC Recovery, 1 ns Pulse Pairing	PDIP-28, SO-28, PCC-28
ML4417, ML4427	Zone Bit Recording IC	100 MHz VCO	SO-16, PDIP-16
ML4568	Pulse Detector with Embedded Servo	5 V Only; 1 ns Pulse Pairing	PCC-28
ML541	Read Data Processor	15 MBit/s Data Rate	PDIP-24, CerDIP-24, PCC-28, SO-24
ML8464B	Pulse Detector	DP8464B Second Source	PDIP-24, PCC-28
ML8464C	Pulse Detector	1 ns Pulse Pairing	PDIP-24, PCC-28

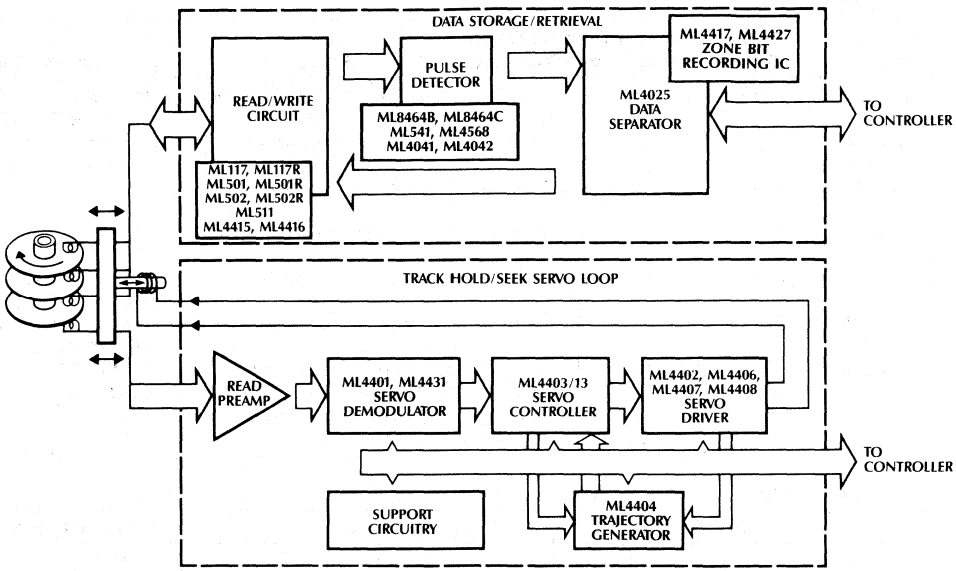
3. Servo Control ICs

Part Number	Function	Key Feature	Package Options
ML4401	Servo Demodulator	ECL Output VCO	PDIP-28, PCC-28
ML4402	Servo Driver, External Power Drive	Low Offset (±5 mV)	PDIP-20, PCC-20
ML4403	Servo Controller	On-Chip Interpolation Function	PDIP-20, PCC-20
ML4404	Analog Trajectory Generator	User-Defined Trajectory, 2 DACs	PDIP-28, PCC-28
ML4406	Servo Driver, Internal Power Drive	Internal Threshold Reference	PCC-20
ML4407	Servo Driver, Internal Power Drive	External Threshold Reference	PCC-20
ML4408	Low Voltage Drop Servo Driver	5 V only or 12 V Operation	SO-24
ML4413	Servo Controller	ML4403 with Ext. Amp. Nulling	PDIP-24, PCC-28
ML4431	Servo Demodulator	Enhanced ML4401; TTL Output	PCC-32

4. Spindle Motor Control ICs

Part Number	Function	Key Feature	Package Options
ML4410	Sensorless Spindle Motor Control	Back-EMF-Commutation	PCC-28

Hard Disk Drive Data Path and Servo Control Diagram



Micro Linear provides a full set of Winchester Hard Disk Drive support chips including the data path and the head servo positioning path. Micro Linear supports both dedicated and embedded servo disk drives with read-write preamps, pulse detectors, data separators, servo demodulators, controllers and drivers, and 8- and 10-bit data converters for digital servo systems.

ML117, ML117R

2, 4, or 6-Channel Read/Write Circuits

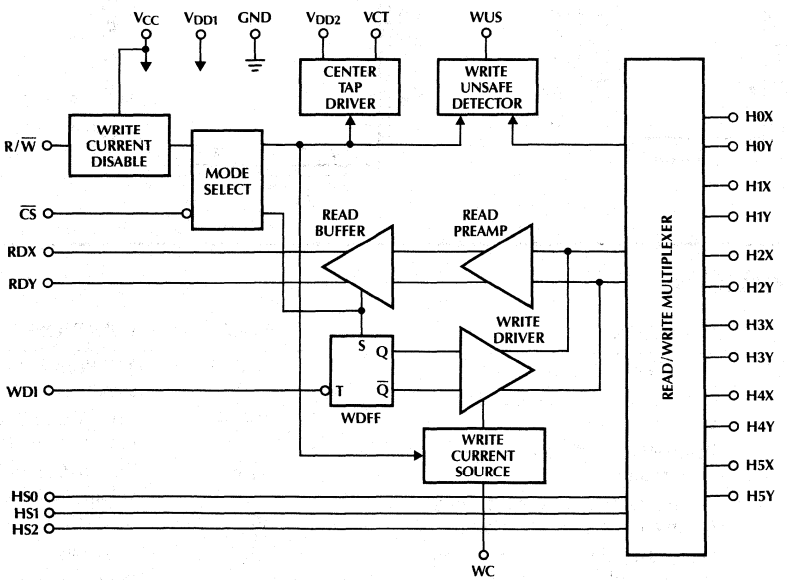
GENERAL DESCRIPTION

The ML117 devices are bipolar monolithic integrated circuits designed for use with center-tapped ferrite recording heads. They provide a low noise read path, write current control, and data protection circuitry for as many as six channels. The ML117 requires +5V and +12V power supplies and is available in 2, 4, or 6-channel versions with a variety of packages. The ML117 contains exclusive circuitry that inhibits write current during device power-up, thereby eliminating power-up "glitches" common to similar read/write circuits. The ML117R differs from the ML117 by having internal damping resistors.

FEATURES

- Exclusive write current disable during power-up
- Replacement for SSI 32R117/117R
- +5V, +12V power supplies
- Single or multi-platter Winchester drives
- Designed for center-tapped ferrite heads
- Programmable write current source
- Available in 2, 4, or 6 channels
- Easily multiplexed for larger systems
- Includes write unsafe detection
- TTL compatible control signals

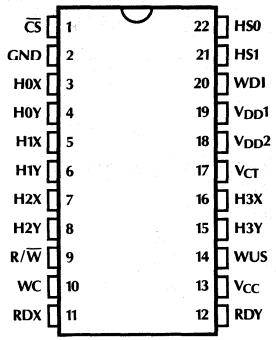
BLOCK DIAGRAM



5

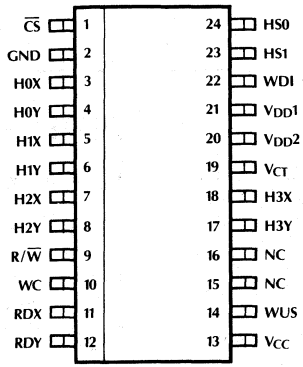
PIN CONNECTIONS

ML117-4 OR ML117R-4
4 Channels
22-PIN DIP



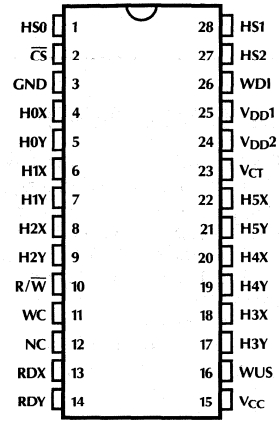
TOP VIEW

ML117-4 OR ML117R-4
4 Channels
24-PIN SOIC



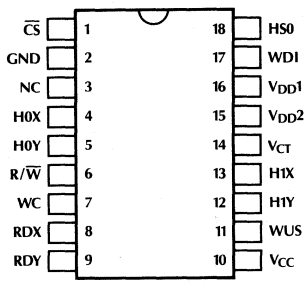
TOP VIEW

ML117-6 OR ML117R-6
6 Channels
28-PIN DIP



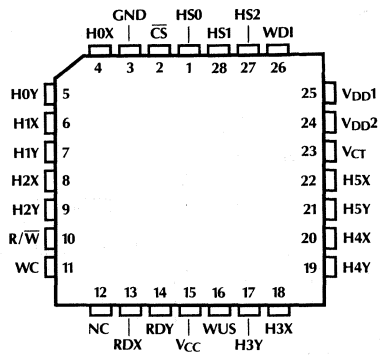
TOP VIEW

ML117-2 OR ML117R-2
2 Channels
18-PIN SOIC AND DIP



TOP VIEW

ML117-6 OR ML117R-6
6 Channels
28-PIN PCC



TOP VIEW

PIN DESCRIPTION

NAME	FUNCTION
HS0–HS2	Head Select (six heads)
$\overline{CS}$	Chip Select (low level enables chip)
R/$\overline{W}$	Read/Write (high level selects Read mode)
WUS	Write Unsafe, open collecter output (high level indicates alarm)
WDI	Write Data In (negative transition toggles head current direction)
H0X–H5X	X head connections
H0Y–H5Y	Y head connections

NAME	FUNCTION
RDX, RDY	X, Y Read Data (differential read signal out)
WC	Write Current (used to set the write current magnitude)
V_{CT}	Voltage Center Tap (center tap voltage source)
V_{CC}	+5 volts
$V_{DD}1$	+12 volts
$V_{DD}2$	Positive supply for center tap
GND	Ground

ABSOLUTE MAXIMUM RATINGS

(Note 1)

Power Supply Voltage Range
- $V_{DD}1$ ..... −0.3 to 14 V_{DC}
- $V_{DD}2$ ..... −0.3 to 14 V_{DC}
- V_{CC} ..... −0.3 to 6 V_{DC}

Input Voltage Range
- Digital Inputs ($\overline{CS}$, R/$\overline{W}$, HS, WDI) ..... −0.3 to V_{CC} +0.3 V_{DC}
- Head Ports (H0X–H5X, H0Y–H5Y) .... −0.3 to $V_{DD}1$ +0.3 V_{DC}
- Write Unsafe (WUS) ..... −0.3 to 14 V_{DC}

Write Current (I_W) ..... 60 mA

Output Current
- Read Data (RDX, RDY) ..... −10 mA
- Center Tap Current (I_{CT}) ..... −60 mA
- Write Unsafe (WUS) ..... 12 mA

Storage Temperature ..... −65°C to 150°C

Junction Temperature (T_J) ..... 125°C

Lead Temperature (Soldering 10 sec.) ..... 300°C

OPERATING CONDITIONS

Supply Voltage
- $V_{DD}1$ ..... 12 V ± 10%
- V_{CC} ..... 5 V ± 10%
- $V_{DD}2$ ..... 6.5 to $V_{DD}1$

Head Inductance (L_H) ..... 5 to 15 µH

Damping Resistor (R_D, ML117 only) ..... 500 to 2000 Ω

RCT Resistor (1/2 Watt) ..... 130 Ω ± 5%

Write Current (I_W) ..... 25 to 50 mA

ELECTRICAL CHARACTERISTICS

Unless otherwise specified $V_{DD}1 = 12\,V \pm 10\%$, $V_{CC} = 5\,V \pm 10\%$, $0°C \leq T_A \leq 70°C$ (Notes 2 and 3).

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
DC OPERATING CHARACTERISTICS						
POWER SUPPLY						
I_{CC}	V_{CC} Supply Current	Read or Idle Mode			25	mA
		Write Mode			30	mA
I_{DD}	V_{DD} Supply Current	Read Mode			50	mA
		Write Mode			$30 + I_W$	mA
		Idle Mode			25	mA
P_D	Power Dissipation	Read Mode			600	mW
		Write Mode $I_W = 50\,mA$, $R_{CT} = 130\,\Omega$			700	mW
		Write Mode $I_W = 50\,mA$, $R_{CT} = 0\,\Omega$			1050	mW
		Idle Mode			400	mW
DIGITAL INPUTS ($\overline{CS}$, R/$\overline{W}$, HS, WDI)						
V_{IH}	High Voltage		2		$V_{CC}+0.3$	V_{DC}
V_{IL}	Low Voltage		−0.3		0.8	V_{DC}
I_{IH}	High Current	$V_{IH} = 2.0\,V$			100	µA
I_{IL}	Low Current	$V_{IL} = 0.8\,V$	−0.4			mA
WUS OUTPUT						
V_{OL}	Output Low Voltage	$I_{OL} = 8\,mA$ (Safe)			0.5	V_{DC}
I_{OH}	Output High Current	$V_{OH} = 5\,V$ (Unsafe)			100	µA
CENTER TAP VOLTAGES						
V_{CT}	Read Mode	Read Mode		4		V_{DC}
V_{CT}	Write Mode	Write Mode		6		V_{DC}

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ELECTRICAL CHARACTERISTICS (Continued)

Unless otherwise specified $V_{DD}1 = 12V \pm 10\%$, $V_{CC} = 5V \pm 10\%$, $I_W = 45mA$, $L_H = 10\mu H$, $R_D = 750\Omega$, $f_{DATA} = 5MHz$, C_L (RDX, RDY) $\leq 20pF$, $0°C \leq T_A \leq 70°C$ (Notes 2 and 3) (V_{IN} is referenced to V_{CT} for Read Mode Characteristics).

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
WRITE MODE CHARACTERISTICS						
I_{WR}	Write Current Range	$I_W = K/R_{WC}$	10		50	mA
K	Write Current Constant		133		147	V
V_{HD}	Differential Head Voltage Swing		8			V_{PK}
I_{HU}	Unselected Head Transient Current				2	mA_{PK}
C_{OD}	Differential Output Capacitance				15	pF
R_{OD}	Differential Output Resistance	ML117	10k			Ω
		ML117R	562		938	Ω
f_{WDI}	WDI Transition Frequency	WUS = Low	250			kHz
A_I	I_{WS} to Head Current Gain			20		A/A
I_L	Unselected Head Leakage	Sum of X & Y Side Leakage Current			85	μA
READ MODE CHARACTERISTICS						
A_V	Differential Voltage Gain	$V_{IN} = 1mV_{P-P}$ @ 300kHz, R_L (RDX, RDY) = 1kΩ	80		120	V/V
DR	Dynamic Range	DC Input Voltage (V_i) Where Gain Falls 10%, $V_{IN} = V_i + 0.5mV_{P-P}$ @ 300kHz	−3		+3	mV
BW	Bandwidth (−3dB)	$\lvert Z_S \rvert < 5\Omega$, $V_{IN} = 1mV_{RMS}$	30			MHz
e_{IN}	Input Noise Voltage	BW = 15MHz, $L_H = 0$, $R_H = 0$			2.1	$nV/\sqrt{Hz}$
C_{IN}	Differential Input Capacitance				20	pF
R_{IN}	Differential Input Resistance	ML117	2k			Ω
		ML117R	390		810	Ω
I_{IN}	Input Bias Current				45	μA
CMRR	Common-Mode Rejection Ratio	$V_{CM} = V_{CT} + 100mV_{P-P}$ @ f = 5MHz	50			dB
PSRR	Power Supply Rejection Ratio	$100mV_{P-P}$ @ 5MHz on $V_{DD}1$, $V_{DD}2$, or V_{CC}	45			dB
CS	Channel Separation	Unselected Channels: $V_{IN} = 100mV_{P-P}$ @ 5MHz and Selected Channel: $V_{IN} = 0mV_{P-P}$	45			dB
V_{OS}	Output Offset Voltage		−480		+480	mV
V_{OCM}	Common-Mode Output Voltage	Read Mode	5		7	V
		Write or Idle Mode		4.3		V
R_{OUT}	Single-Ended Output Resistance	f = 5MHz			30	Ω
I_L	Leakage Current, RDX, RDY	RDX, RDY = 6V Write or Idle Mode	−100		+100	μA
I_O	Output Current	AC Coupled Load, RDX to RDY	2			mA

ELECTRICAL CHARACTERISTICS (Continued)

Unless otherwise specified $V_{DD}1 = 12V \pm 10\%$, $V_{CC} = 5V \pm 10\%$, $I_W = 45mA$, $L_H = 10\mu H$, $R_D = 750\Omega$, $f_{DATA} = 5MHz$, $0°C \leq T_A \leq 70°C$ (Notes 2 and 3).

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
SWITCHING CHARACTERISTICS						
t_{RW}	R/$\overline{W}$ to Write Switching Delay	To 90% of Write Current Output			1	µS
t_{WR}	R/$\overline{W}$ to Read Switching Delay	To 90% of 100mV, 10MHz Read Signal Envelope or to 90% Decay of Write Current			1	µS
t_{IW} or t_{IR}	$\overline{CS}$ to Select Switching Delay	To 90% of Write Current or to 90% of 100mV, 10MHz Read Signal Envelope			1	µS
t_{WI} or t_{RI}	$\overline{CS}$ to Select Switching Delay	To 90% Decay of 100mV, 10MHz Read Signal Envelope or to 90% Decay of Write Current			1	µS
t_{HS}	Head Select Switching Delay	To 90% of 100mV, 10MHz Read Signal Envelope			1	µS
tD1	Safe to Unsafe Write Unsafe Delay	$I_W = 50mA$	1.6		8	µS
tD2	Unsafe to Safe Write Unsafe Delay	$I_W = 50mA$			1	µS
tD3	Head Current Prop. Delay	$L_H = 0$, $R_H = 0$ From 50% points			25	nS
tD3	Head Current Asymmetry	WDI has 50% Duty Cycle and 1nS Rise/Fall Time			2	nS
	Time Head Current Rise/Fall	10% and 90% Points			20	nS

Note 1: Absolute maximum ratings are limits beyond which the life of the integrated circuit may be impaired. All voltages unless otherwise specified are measured with respect to ground.

Note 2: Limits are guaranteed by 100% testing, sampling, or correlation with worst-case test conditions.

Note 3: Maximum junction temperature (T_J) should not exceed 125°C.

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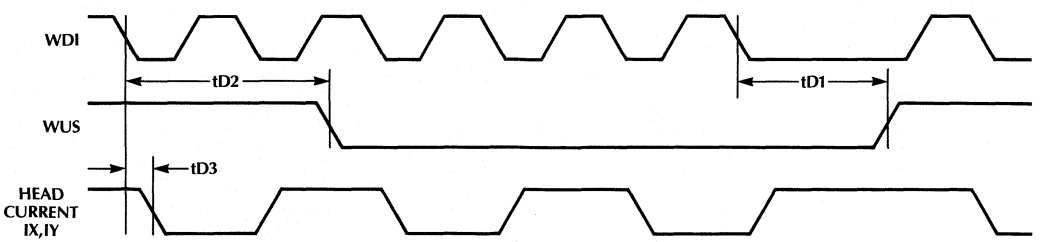
TIMING DIAGRAMS



Write Mode Timing Diagram

FUNCTIONAL DESCRIPTION

CIRCUIT OPERATION

The ML117, ML117R functions as a write driver or as a read amplifier for the selected head. Head selection and mode control are described in *Tables 1 & 2*. Both R/$\overline{W}$ and $\overline{CS}$ have internal pull-up resistors for the prevention of an accidential write condition.

READ MODE

In the Read Mode the ML117, ML117R is configured as a low noise differential amplifier, the write current source and the write unsafe detector are deactivated, and the write data flip-flop is set. The RDX and RDY outputs are driven by emitter followers and are in phase with the "X" and "Y" head ports.

The internal write current source is deactivated for both the Read and the Chip Deselect modes which eliminates the need for external gating of the write current source.

WRITE MODE

The Write mode configures the ML117, ML117R as a current switch and activates the Write Unsafe Detector. The head current is toggled between the X- and Y-side of the recording head on the falling edges of WDI, Write Data Input. A preceding read operation initializes the Write Data Flip-Flop, WDFF, to pass current through the X-side of the head. The magnitude of the write current, given by:

$I_W = K/R_{WC}$, where K = Write Current Constant

is set by the external resistor, R_{WC}, connected from pin WC to GND.

Any of the following conditions will be indicated as a high level on the Write Unsafe, WUS, open collector output.

- Head open
- Head center tap open
- WDI frequency too low
- Device in Read mode
- Device not selected
- No write current

Two negative transitions on WDI are required to clear WUS after the fault condition is removed.

Table 1.

Head Select

HS2	HS1	HS0	HEAD
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	X	NONE

0 = Logic Level Low
1 = Logic Level High
X = Don't Care

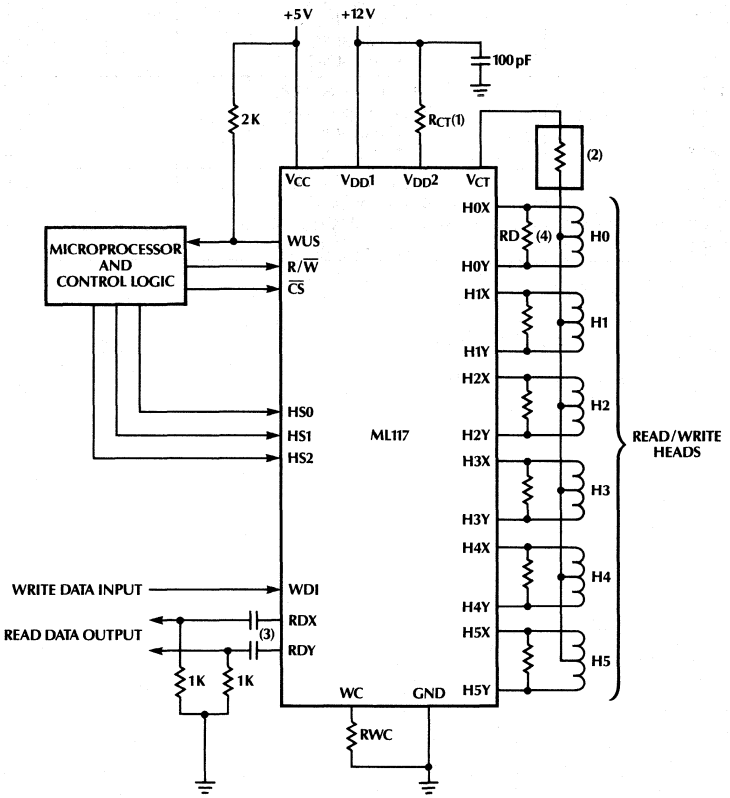
Table 2.

Mode Select

$\overline{CS}$	R/$\overline{W}$	MODE
0	0	Write
0	1	Read
1	X	Idle

0 = Logic Level Low
1 = Logic Level High
X = Don't Care

TYPICAL APPLICATION



NOTES:

1. RCT is optional and is used to limit internal power dissipation (Otherwise connect $V_{DD}1$ to $V_{DD}2$).
   RCT (1/2 Watt) = 130 ($55/I_W$) ohms
   where I_W = Write Current, in mA
2. Ferrite bead optional: used to suppress write current overshoot and ringing. Recommend Ferroxcube 3659065/4A6.
3. RDX and RDY load capacitance 20 pF maximum. RDX and RDY output current must be limited to 100 μA.
4. Damping resistors not required on ML117R.

THERMAL CHARACTERISTICS

28-Lead	
PDIP	80°C/W
PCC	60°C/W
24-Lead	
SOIC	60°C/W
22-Lead	
PDIP	100°C/W
18-Lead	
PDIP	115°C/W
SOIC	85°C/W

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ORDERING INFORMATION

PART NUMBER	PACKAGE	NUMBER OF CHANNELS
ML117-2CP	18-Lead Molded DIP	2
ML117R-2CP	18-Lead Molded DIP	2
ML117-2CS	18-Lead SOIC	2
ML117R-2CS	18-Lead SOIC	2
ML117-4CP	22-Lead Molded DIP	4
ML117R-4CP	22-Lead Molded DIP	4
ML117-4CS	24-Lead SOIC	4
ML117R-4CS	24-Lead SOIC	4
ML117-6CP	28-Lead Molded DIP	6
ML117R-6CP	28-Lead Molded DIP	6
ML117-6CQ	28-Lead PCC	6
ML117R-6CQ	28-Lead PCC	6

ML501, ML501R, ML502, ML502R, ML502S–Series

6, 7, or 8-Channel Read/Write Circuits

GENERAL DESCRIPTION

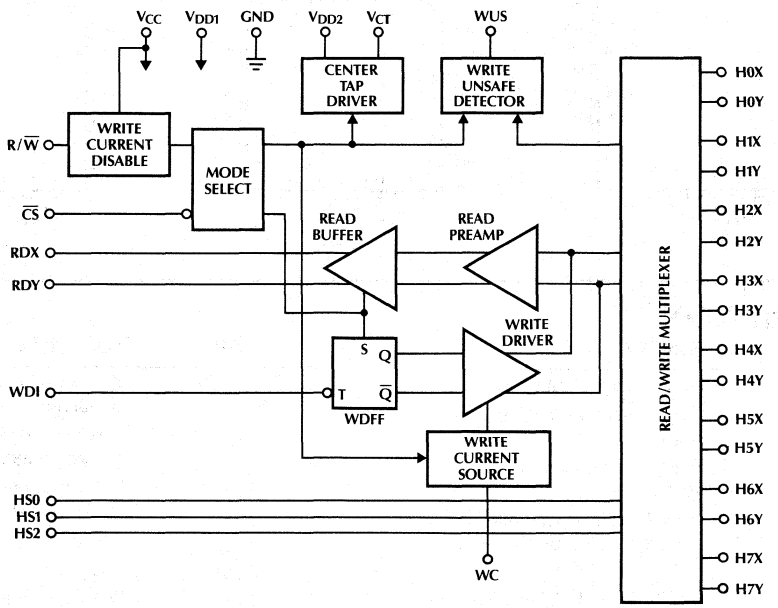
The ML501, ML502 family of devices are bipolar monolithic read/write circuits designed for use with fixed disk center-tapped recording heads. The ML501 and ML501R are designed for use with ferrite recording heads while the ML502, ML502R and ML502S are designed for thin film or composite heads. The R and S designation in the part number indicate that these parts have internal head damping resistors.

The ML501, ML502 family provides up to eight multiplexed read/write data channels. These circuits exhibit features not found in similar read/write circuits such as improved write current stability and the elimination of write current "glitches" during power-up. The exclusive ML502 is identical to the ML501 except that the write unsafe detect circuitry is designed to operate with lower head inductance.

FEATURES

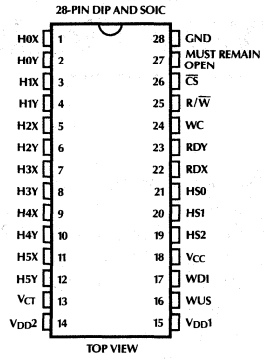
- Exclusive write current disable during power-up
- Enhanced write current stability
- ML501, ML501R is replacement for SSI 32R501/501R and is designed for center-tapped ferrite heads
- ML502, ML502R, and ML502S are designed for center-tapped thin film or composite heads
- Single or multi-platter Winchester drives
- Easily multiplexed for larger systems
- Available in 6, 7 or 8 channels
- TTL compatible control signals
- Programmable write current source
- Includes write unsafe detection
- Available in a selection of packages
- +5V, +12V power supplies

BLOCK DIAGRAM

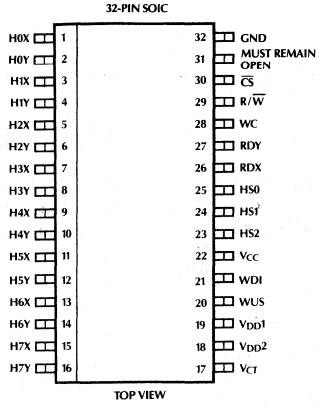


PIN CONNECTIONS

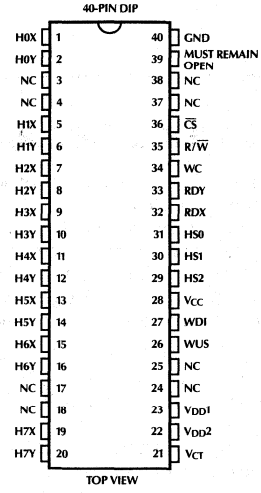
ML501-6 OR ML501R-6 OR ML502-6 OR ML502R-6 6 Channels



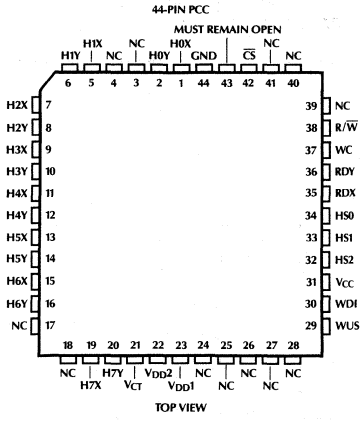
ML501-8 OR ML501R-8 OR ML502-8 OR ML502R-8 8 Channels



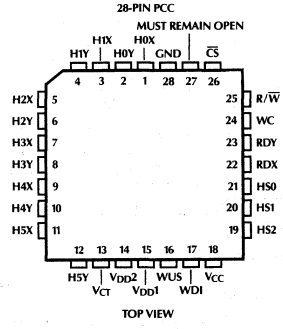
ML501-8 OR ML501R-8 OR ML502-8 OR ML502R-8 8 Channels



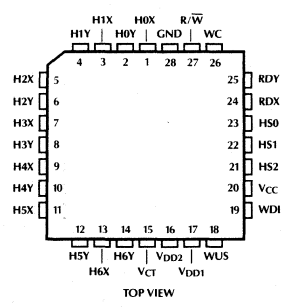
ML501-8 OR ML501R-8 OR ML502-8 OR ML502R-8 OR ML502S-8 8 Channels



ML501-6 OR ML501R-6 OR ML502-6 OR ML502R-6 OR ML502S-6 6 Channels



ML502S-7CQ ML502R-7CQ



PIN DESCRIPTION

NAME	FUNCTION
HS0–HS2	Head Select (eight heads)
$\overline{CS}$	$\overline{\text{Chip Select}}$ (low level enables chip)
R/$\overline{W}$	Read/$\overline{\text{Write}}$ (high level selects Read mode)
WUS	Write Unsafe, open collecter output (high level indicates an unsafe writing condition)
WDI	Write Data In (negative transition toggles head current direction)
H0X–H7X	X head connections
H0Y–H7Y	Y head connections

NAME	FUNCTION
RDX, RDY	X, Y Read Data (differential read signal out)
WC	Write Current (used to set the write current magnitude)
V_{CT}	Voltage Center Tap (center tap voltage source)
V_{CC}	+5 volts
$V_{DD}1$	+12 volts
$V_{DD}2$	Positive supply for center tap
GND	Ground

ABSOLUTE MAXIMUM RATINGS

(Note 1)

Power Supply Voltage Range
- $V_{DD}1$ ..... −0.3 to 14 V_{DC}
- $V_{DD}2$ ..... −0.3 to 14 V_{DC}
- V_{CC} ..... −0.3 to 6 V_{DC}

Input Voltage Range
- Digital Inputs ($\overline{CS}$, R/$\overline{W}$, HS, WDI) ..... −0.3 to V_{CC} +0.3 V_{DC}
- Head Ports (H0X–H7X, H0Y–H7Y .... −0.3 to $V_{DD}1$ +0.3 V_{DC}
- Write Unsafe (WUS) ..... −0.3 to 14 V_{DC}

Write Current (I_W) ..... 60 mA

Output Current
- Read Data (RDX, RDY) ..... −10 mA
- Center Tap Current (I_{CT}) ..... −60 mA
- Write Unsafe (WUS) ..... 12 mA

Storage Temperature ..... −65°C to 150°C

Junction Temperature (T_J) ..... 135°C

Lead Temperature (Soldering 10 sec.) ..... 300°C

OPERATING CONDITIONS

Supply Voltage
- $V_{DD}1$ ..... 12 V ± 10%
- V_{CC} ..... 5 V ± 10%

Head Inductance
- L_H, ML501 or ML501R only ..... 5 to 15 µH
- L_H, ML502, ML502R, ML502S only ..... 400 to 1000 nH

Damping Resistor (R_D, ML501 only) ..... 500 to 2000 Ω

RCT Resistor (1/2 Watt) ..... 120 Ω ± 5%

Write Current (I_W) ..... 22 to 50 mA

ELECTRICAL CHARACTERISTICS

Unless otherwise specified $V_{DD}1 = 12\,V \pm 10\%$, $V_{CC} = 5\,V \pm 10\%$, $R_{CT} = 120\,\Omega \pm 5\%$, $I_W = 45\,mA$, $0°C \leq T_A \leq 70°C$ (Notes 2 and 3).

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
DC OPERATING CHARACTERISTICS						
POWER SUPPLY						
I_{CC}	V_{CC} Supply Current	Read or Idle Mode			25	mA
		Write Mode			25	mA
I_{DD}	V_{DD} Supply Current	Read Mode			48	mA
		Write Mode			25 + I_W	mA
		Idle Mode			20	mA
P_D	Power Dissipation	Read Mode			770	mW
		Write Mode $I_W = 50\,mA$			830	mW
		Write Mode $I_W = 50\,mA$, $R_{CT} = 0\,\Omega$			1125	mW
		Idle Mode			400	mW
DIGITAL INPUTS ($\overline{CS}$, R/$\overline{W}$, HS, WDI)						
V_{IH}	High Voltage		2			V_{DC}
V_{IL}	Low Voltage				0.8	V_{DC}
I_{IH}	High Current	$V_{IH} = 2.0\,V$			100	µA
I_{IL}	Low Current	$V_{IL} = 0.8\,V$	−0.4			mA
WUS OUTPUT						
V_{OL}	Output Low Voltage	$I_{OL} = 8\,mA$ (Safe)			0.5	V_{DC}
I_{OH}	Output High Current	$V_{OH} = 5\,V$ (Unsafe)			100	µA
CENTER TAP VOLTAGES						
V_{CT}	Read Mode	Read Mode		4		V_{DC}
V_{CT}	Write Mode	Write Mode		6		V_{DC}

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ELECTRICAL CHARACTERISTICS (Continued)

Unless otherwise specified $V_{DD}1 = 12V \pm 10\%$, $V_{CC} = 5V \pm 10\%$, $R_{CT} = 120\Omega \pm 5\%$, $I_W = 45mA$, $L_H = 10\mu H$ (ML501, ML501R), $L_H = 600nH$ (ML502, ML502R, ML502S), $R_D = 750\Omega$ (ML501), $f_{DATA} = 5MHz$, C_L (RDX, RDY) $\leq 20pF$, $0°C \leq T_A \leq 70°C$ (Notes 2 and 3) (V_{IN} is referenced to V_{CT} for Read Mode Characteristics).

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
WRITE MODE CHARACTERISTICS						
I_{WR}	Write Current Range	$I_W = K/R_{WC}$	10		50	mA
K	Write Current Constant		129		151	V
V_{HD}	Differential Head Voltage Swing		7.5			V_{PK}
I_{HU}	Unselected Head Transient Current				2	mA_{PK}
C_{OD}	Differential Output Capacitance				15	pF
R_{OD}	Differential Output Resistance	ML501, ML502	10k			Ω
		$T_J = 25°C$ ML501R, ML502S/ML502R	560/180		940/300	Ω
f_{WDI}	WDI Transition Frequency	WUS = Low	250			kHz
A_I	I_{WC} to Head Current Gain			20		A/A
I_L	Unselected Head Leakage	Sum of X & Y Side Leakage Current			85	μA
READ MODE CHARACTERISTICS						
A_V	Differential Voltage Gain	$V_{IN} - 1mV_{P-P}$ @ 300kHz, R_L (RDX, RDY) = 1kΩ	80		120	V/V
DR	Dynamic Range	DC Input Voltage (V_I) Where Gain Falls 10%, $V_{IN} = V_I + 0.5mV_{P-P}$ @ 300kHz	−3		+3	mV
BW	Bandwidth (−3dB)	$\|Z_S\| < 5\Omega$, $V_{IN} = 1mV_{P-P}$	30			MHz
e_{IN}	Input Noise Voltage	BW = 15MHz, $L_H = 0$, $R_H = 0$			1.5	$nV/\sqrt{Hz}$
C_{IN}	Differential Input Capacitance	f = 5MHz			23	pF
R_{IN}	Differential Input Resistance	f = 5MHz, $T_J = 25°C$ ML501, ML502	2k			Ω
		$V_{IN} = 6mV_{P-P}$ ML501R, ML502S/ML502R	530/180		790/300	Ω
I_{IN}	Input Bias Current (1 side)				100	μA
CMRR	Common-Mode Rejection Ratio	$V_{CM} = V_{CT} + 100mV_{P-P}$ @ f = 5MHz	50			dB
PSRR	Power Supply Rejection Ratio	$100mV_{P-P}$ @ 5MHz on $V_{DD}1$, $V_{DD}2$, or V_{CC}	45			dB
CS	Channel Separation	Unselected Channels: $V_{IN} = 100mV_{P-P}$ @ 5MHz and Selected Channel: $V_{IN} = 0mV_{P-P}$	45			dB
V_{OS}	Output Offset Voltage		−480		+480	mV
V_{OCM}	Common-Mode Output Voltage	Read Mode	5		7	V
		Write or Idle Mode		4.3		V
R_{OUT}	Single-Ended Output Resistance	f = 5MHz			30	Ω
R_L	External Resistive Load (AC Coupled to Output)	Per Side to GND	100			Ω
I_L	Leakage Current, RDX, RDY	$3V < (RDX, RDY) < 8V$ Write or Idle Mode	−50		50	μA
Z_O	Center Tap Output Impedance	$0MHz \leq f \leq 5MHz$			150	Ω
I_O	Output Current	AC Coupled Load, RDX to RDY	2			mA

ELECTRICAL CHARACTERISTICS (Continued)

Unless otherwise specified $V_{DD}1 = 12V \pm 10\%$, $V_{CC} = 5V \pm 10\%$, $R_{CT} = 120\Omega \pm 5\%$, $I_W = 45mA$, $L_H = 10\mu H$ (ML501, ML501R), $L_H = 600nH$ (ML502, ML502R, ML502S), $R_D = 750\Omega$ (ML501), $f_{DATA} = 5MHz$, $0°C \leq T_A \leq 70°C$ (Notes 2 and 3).

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
SWITCHING CHARACTERISTICS						
t_{RW}	R/$\overline{W}$ to Write Switching Delay	To 90% of Write Current Output			600	ns
t_{WR}	R/$\overline{W}$ to Read Switching Delay	To 90% of 100mV, 10MHz Read Signal Envelope or to 90% Decay of Write Current			600	ns
t_{IW} or t_{IR}	$\overline{CS}$ to Select Switching Delay	To 90% of Write Current or to 90% of 100mV, 10MHz Read Signal Envelope			600	ns
t_{WI} or t_{RI}	$\overline{CS}$ to Unselect Switching Delay	To 90% Decay of 100mV, 10MHz Read Signal Envelope or to 90% Decay of Write Current			600	ns
t_{HS}	Head Select Switching Delay	To 90% of 100mV, 10MHz Read Signal Envelope			600	ns
tD1	Safe to Unsafe Write Unsafe Delay	$I_W = 50mA$	1.6		8	us
tD2	Unsafe to Safe Write Unsafe Delay	$I_W = 20mA$			1	us
tD3	Prop. Delay Head Current	$L_H = 0$, $R_H = 0$ From 50% points		25	40	ns
tD3	Asymmetry Head Current	WDI has 50% Duty Cycle and 1nS Rise/Fall Time			2	ns
	Rise/Fall Head Current	10% and 90% Points			20	ns

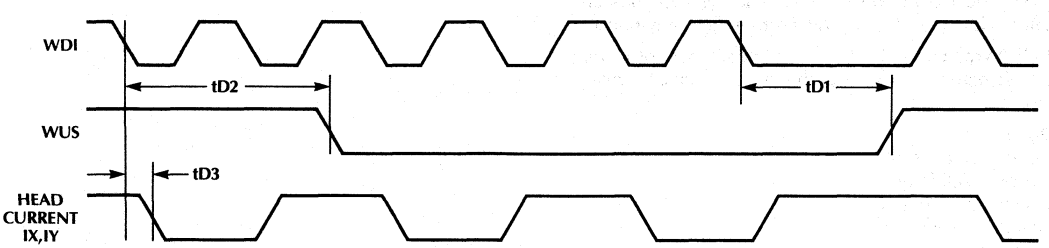
Note 1: Absolute maximum ratings are limits beyond which the life of the integrated circuit may be impaired. All voltages unless otherwise specified are measured with respect to ground.

Note 2: Limits are guaranteed by 100% testing, sampling, or correlation with worst-case test conditions.

Note 3: Maximum junction temperature (T_J) should not exceed 135°C.

5

TIMING DIAGRAM



Write Mode Timing Diagram

FUNCTIONAL DESCRIPTION

CIRCUIT OPERATION

For any selected head, the ML501, ML502 functions as a read amplifier when in the Read mode, or as a write current switch when in the Write mode. Pins $\overline{HS0}$, HS1 and HS2 determine head selection while pin R/$\overline{W}$ controls the Read/Write mode. A detected "write-unsafe" condition is indicated by pin WUS.

READ MODE

When the ML501, ML502 is in the Read Mode, it operates as a low-noise differential amplifier on the selected channel. In Read mode the write data flip-flop is set and both the write unsafe detector and the write current source are deactivated. The center tap voltage is also lowered. Pins RDX and RDY provide differential emitter follower outputs which are in phase with the X and Y head input pins.

Note that during the Read or Chip Deselect mode the internal write current is deactivated, thus making external write current gating unnecessary.

WRITE MODE

The ML501, ML502 operates as a write-current switch when in the Write mode. Write current magnitude is determined by the following relationship:

$I_W = K/R_{WC}$

Where: K = Write Current Constant

R_{WC} = Resistance connected between pin WC and GND.

The head current is toggled between the X and Y side of the selected head by a negative transition on WDI (Write Data Input). When switching the ML501, ML502 to write mode, the WDFF (Write Data Flip-Flop) is initialized to pass write current through the X-side of the head.

The ML501, ML502 exhibit enhanced write current stability, compared to similar read/write circuits, which reduces the problem of oscillation. This is a result of increased internal write current compensation. Also, write current "glitches" during power-up, common in similar read/write circuits, are eliminated with an exclusive write current disabling function.

The WUS (Write Unsafe) pin is an open collector output that gives a logic high level for any of the following unsafe write conditions:

- Open head
- Open head center-tap
- Too low WDI frequency
- Read mode selected
- Device not selected
- No write current

Two negative transitions on WDI are required to clear WUS after the fault condition is removed.

The ML502, ML502R, ML502S differ from the ML501, ML501R by having write unsafe detect circuitry that is designed to operate with lower amplitude write pulse voltages, which result from the lower head inductance of thin film or composite heads.

Table 1.

Head Select

HS2	HS1	HS0	HEAD
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

0 = Logic Level Low
1 = Logic Level High
X = Don't Care

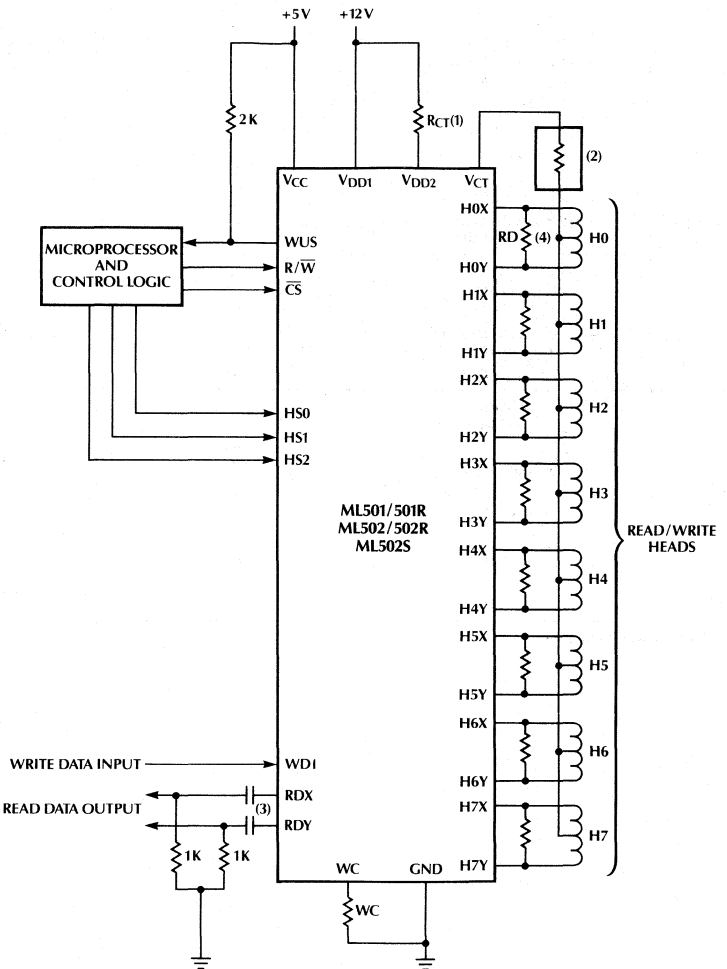
Table 2.

Mode Select

$\overline{CS}$	R/$\overline{W}$	MODE
0	0	Write
0	1	Read
1	X	Idle

0 = Logic Level Low
1 = Logic Level High
X = Don't Care

TYPICAL APPLICATION



NOTES:

1. RCT is optional and is used to limit internal power dissipation (Otherwise connect $V_{DD}1$ to $V_{DD}2$).
   RCT (1/2 Watt) = 120 (50/I_W) ohms
   where I_W = Write Current, in mA
2. Ferrite bead optional: used to suppress write current overshoot and ringing. Recommend Ferroxcube 3659065/4A6.
3. RDX and RDY load capacitance 20 pF maximum. RDX and RDY output current must be limited to 100 μA.
4. Damping resistors not required on ML501R or ML502R.

ORDERING INFORMATION

PART NUMBER	PACKAGE	NUMBER OF CHANNELS	TRANSDUCER HEAD TYPE
ML501-6CP	28-Lead Molded DIP	6	Ferrite Heads
ML501-6CQ	28-Lead PCC	6	
ML501-6CS	28-Lead SOIC	6	
ML501-8CP	40-Lead Molded DIP	8	
ML501-8CQ	44-Lead PCC	8	
ML501-8CS*	32-Lead SOIC	8	
ML501R-6CP	28-Lead Molded DIP	6	Ferrite Heads
ML501R-6CQ	28-Lead PCC	6	
ML501R-6CS	28-Lead SOIC	6	
ML501R-8CP	40-Lead Molded DIP	8	
ML501R-8CQ	44-Lead PCC	8	
ML501R-8CS*	32-Lead SOIC	8	
ML502-6CP	28-Lead Molded DIP	6	Thin Film or Composite Heads
ML502-6CQ	28-Lead PCC	6	
ML502-6CS	28-Lead SOIC	6	
ML502-8CP	40-Lead Molded DIP	8	
ML502-8CQ	44-Lead PCC	8	
ML502-8CS*	32-Lead SOIC	8	
ML502R-6CP	28-Lead Molded DIP	6	Thin Film or Composite Heads
ML502R-6CQ	28-Lead PCC	6	
ML502R-6CS	28-Lead SOIC	6	
ML502R-7CQ	28-Lead PCC	7	
ML502R-8CP	40-Lead Molded DIP	8	
ML502R-8CQ	44-Lead PCC	8	
ML502R-8CS*	32-Lead SOIC	8	
ML502S-6CQ	28-Lead PCC	6	Thin Film or Composite Heads
ML502S-7CQ	28-Lead PCC	7	
ML502S-8CQ	44-Lead PCC	8	

* This package is available as a special order only.

Micro Linear

ML511, ML511R-Series

4, 6, 7, or 8-Channel Ferrite Read/Write Circuits

GENERAL DESCRIPTION

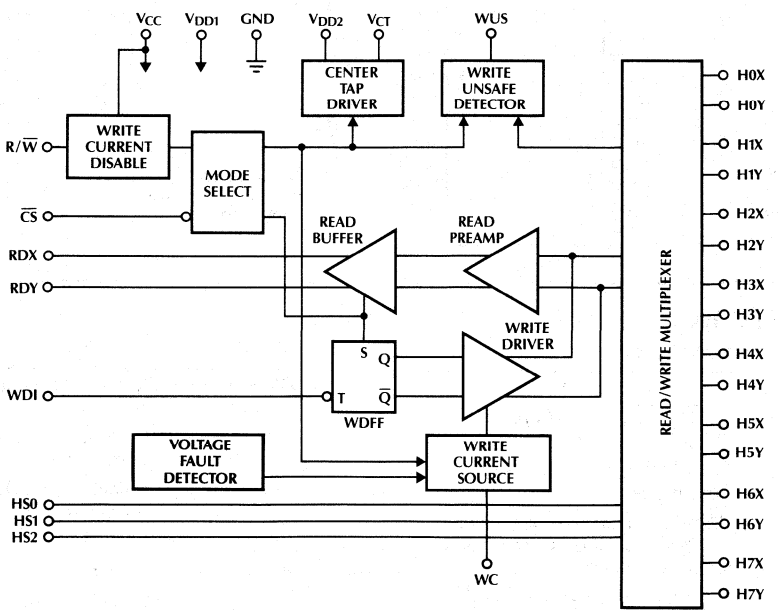
The ML511 is a bipolar monolithic read/write circuit designed for use with center-tapped ferrite recording heads. The ML511 and ML511R are performance upgrades from the ML501 and ML501R. The R designation in the part number indicates that this part has internal head damping resistors.

The ML511 provides up to eight multiplexed read/write data channels. These circuits exhibit features not found in similar read/write circuits such as improved write current stability and the elimination of write current "glitches" during power-up. The ML511 also provides a low noise read data path, and data protection circuitry for all of the channels.

FEATURES

- Enhanced write current stability
- ML511, ML511R is replacement for SSI 32R511/511R and is designed for center-tapped ferrite heads
- Single or multi-platter Winchester drives
- Easily multiplexed for larger systems
- Power supply fault protection
- 1.5nV/ $\sqrt{Hz}$ maximum input noise voltage
- TTL compatible control signals
- Programmable write current source
- Includes write unsafe detection
- Available in a selection of packages
- +5V, +12V power supplies

BLOCK DIAGRAM



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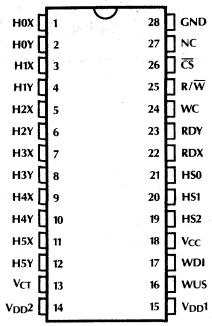
PIN CONNECTIONS

ML511-6 OR ML511R-6
6 Channels

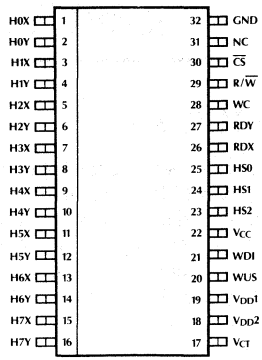
28-PIN DIP AND SOIC



TOP VIEW

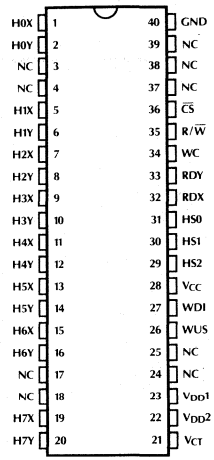
ML511-8 OR ML511R-8
8 Channels

32-PIN SOIC



ML511-8 OR ML511R-8
8 Channels

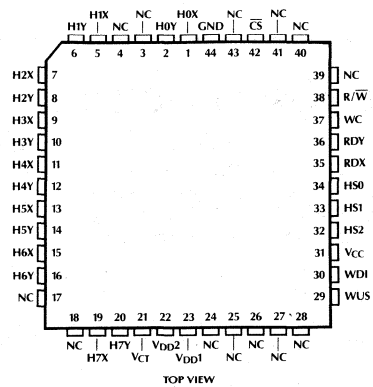
40-PIN DIP



TOP VIEW

ML511-8 OR ML511R-8
8 Channels

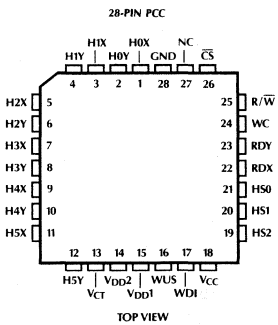
44-PIN PCC



TOP VIEW

ML511-6 OR ML511R-6
6 Channels

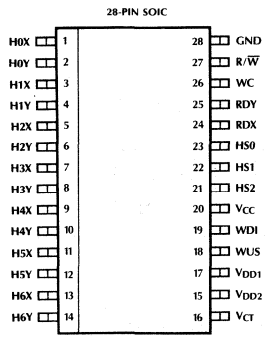
28-PIN PCC



TOP VIEW

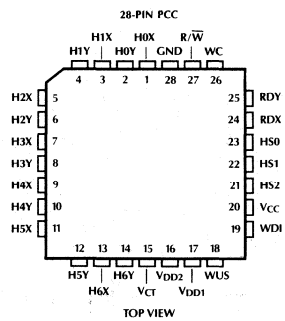
ML511R-7CS
28-Lead SOIC

28-PIN SOIC



ML511R-7CQ
28-Lead PCC

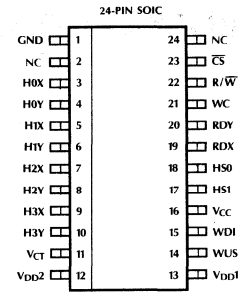
28-PIN PCC



TOP VIEW

ML511-4 OR ML511R-4
4 Channels

24-PIN SOIC



PIN DESCRIPTION

NAME	FUNCTION
HS0–HS2	Head Select (eight heads)
$\overline{CS}$	$\overline{Chip\ Select}$ (low level enables chip)
R/$\overline{W}$	Read/$\overline{Write}$ (high level selects Read mode)
WUS	Write Unsafe, open collecter output (high level indicates an unsafe writing condition)
WDI	Write Data In (negative transition toggles head current direction)
H0X–H7X	X head connections
H0Y–H7Y	Y head connections

NAME	FUNCTION
RDX, RDY	X, Y Read Data (differential read signal out)
WC	Write Current (used to set the write current magnitude)
V_{CT}	Voltage Center Tap (center tap voltage source)
V_{CC}	+5 volts
$V_{DD}1$	+12 volts
$V_{DD}2$	Positive supply for center tap
GND	Ground

ABSOLUTE MAXIMUM RATINGS

(Note 1)

Power Supply Voltage Range
- $V_{DD}1$ ..... −0.3 to 14 V_{DC}
- $V_{DD}2$ ..... −0.3 to 14 V_{DC}
- V_{CC} ..... −0.3 to 6 V_{DC}

Input Voltage Range
- Digital Inputs ($\overline{CS}$, R/$\overline{W}$, HS, WDI) ..... −0.3 to V_{CC} +0.3 V_{DC}
- Head Ports (H0X–H7X, H0Y–H7Y .... −0.3 to $V_{DD}1$ +0.3 V_{DC}
- Write Unsafe (WUS) ..... −0.3 to 14 V_{DC}

Write Current (I_W) ..... 60 mA

Output Current
- Read Data (RDX, RDY) ..... −10 mA
- Center Tap Current (I_{CT}) ..... −60 mA
- Write Unsafe (WUS) ..... 12 mA

Storage Temperature ..... −65°C to 150°C

Junction Temperature (T_J) ..... 135°C

Lead Temperature (Soldering 10 sec.) ..... 300°C

OPERATING CONDITIONS

Supply Voltage
- $V_{DD}1$ ..... 12 V ± 10%
- V_{CC} ..... 5 V ± 10%

Head Inductance
- L_H, ML511 or ML511R ..... 5 to 15 µH

Damping Resistor (R_D, ML511 only) ..... 500 to 2000 Ω

RCT Resistor (1/4 Watt) ..... 120 Ω ± 5%

Write Current (I_W) ..... 10 to 40 mA

ELECTRICAL CHARACTERISTICS

Unless otherwise specified $V_{DD}1 = V_{DD}2 = 12\,V \pm 10\%$, $V_{CC} = 5\,V \pm 10\%$, $R_{CT} = 120\,\Omega \pm 5\%$, $I_W = 40\,mA$, $0°C \leq T_A \leq 70°C$ (Notes 2 and 3).

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
DC OPERATING CHARACTERISTICS						
POWER SUPPLY						
I_{CC}	V_{CC} Supply Current	Read or Idle Mode			35	mA
		Write Mode			30	mA
I_{DD}	V_{DD} Supply Current	Read Mode			35	mA
		Write Mode			20+I_W	mA
		Idle Mode			20	mA
P_D	Power Dissipation	Read Mode			655	mW
		Write Mode $I_W = 40\,mA$, $R_{CT} = 0\,\Omega$			960	mW
		Idle Mode			455	mW
DIGITAL INPUTS ($\overline{CS}$, R/$\overline{W}$, HS, WDI)						
V_{IH}	High Voltage		2			V_{DC}
V_{IL}	Low Voltage				0.8	V_{DC}
I_{IH}	High Current	$V_{IH} = 2.0V$			100	µA
I_{IL}	Low Current	$V_{IL} = 0.8V$	−0.4			mA
WUS OUTPUT						
V_{OL}	Output Low Voltage	$I_{OL} = 8\,mA$ (Safe)			0.5	V_{DC}
I_{OH}	Output High Current	$V_{OH} = 5V$ (Unsafe)			100	µA
CENTER TAP VOLTAGES						
V_{CT}	Read Mode	Read Mode		4		V_{DC}
V_{CT}	Write Mode	Write Mode		6		V_{DC}

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ELECTRICAL CHARACTERISTICS (Continued)

Unless otherwise specified $V_{DD}1 = 12\,V \pm 10\%$, $V_{CC} = 5\,V \pm 10\%$, $R_{CT} = 120\,\Omega \pm 5\%$, $I_W = 35\,mA$, $L_H = 10\,\mu H$, $R_D = 750\,\Omega$ (ML511), $f_{DATA} = 5\,MHz$, C_L (RDX, RDY) $\leq 20\,pF$, $0°C \leq T_A \leq 70°C$ (Notes 2 and 3) (V_{IN} is referenced to V_{CT} for Read Mode Characteristics).

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
WRITE MODE CHARACTERISTICS						
I_{HCW}	Head Current (per side)	Write Mode $0 \leq V_{CC} \leq 3.7\,V$ $0 \leq V_{DD}1 \leq 8.7\,V$	−200		200	µA
I_{WR}	Write Current Range	$I_W = K/R_{WC}$	10		40	mA
K	Write Current Constant		2.375		2.625	
V_{HD}	Differential Head Voltage Swing		7.0			V_{PK}
I_{HU}	Unselected Head Transient Current				2	mA_{PK}
C_{OD}	Differential Output Capacitance				15	pF
R_{OD}	Differential Output Resistance	ML511	10k			Ω
		$T_J = 25°C$ ML511R	600		960	Ω
f_{WDI}	WDI Transition Frequency	WUS = Low	250			kHz
A_I	I_{WC} to Head Current Gain			0.99		mA/mA
I_L	Unselected Head Leakage	Sum of X & Y Side Leakage Current			85	µA
READ MODE CHARACTERISTICS						
A_V	Differential Voltage Gain	$V_{IN} = 1\,mV_{P-P}$ @ 300 kHz, R_L (RDX, RDY) = 1kΩ	85		115	V/V
DR	Dynamic Range	DC Input Voltage (V_I) Where Gain Falls 10%, $V_{IN} = V_I + 0.5\,mV_{P-P}$ @ 300 kHz	−3		+3	mV
BW	Bandwidth (−3 dB)	$\lvert Z_S \rvert < 5\,\Omega$, $V_{IN} = 1\,mV_{P-P}$	30			MHz
e_{IN}	Input Noise Voltage	BW = 15 MHz, $L_H = 0$, $R_H = 0$			1.5	$nV/\sqrt{Hz}$
C_{IN}	Differential Input Capacitance	f = 5 MHz			20	pF
R_{IN}	Differential Input Resistance	f = 5 MHz, $T_J = 25°C$ ML511	2k			Ω
		$V_{IN} = 6\,mV_{P-P}$ ML511R	460		860	Ω
I_{HCR}	Head Current (per side)	Read or Idle Mode $0 \leq V_{CC} \leq 5.5\,V$ $0 \leq V_{DD}1 \leq 13.2\,V$	−200		200	µA
I_{IN}	Input Bias Current (1 side)				45	µA
CMRR	Common-Mode Rejection Ratio	$V_{CM} = V_{CT} + 100\,mV_{P-P}$ @ f = 5 MHz	50			dB
PSRR	Power Supply Rejection Ratio	$100\,mV_{P-P}$ @ 5 MHz on $V_{DD}1$, $V_{DD}2$, or V_{CC}	45			dB
CS	Channel Separation	Unselected Channels: $V_{IN} = 100\,mV_{P-P}$ @ 5 MHz and Selected Channel: $V_{IN} = 0\,mV_{P-P}$	45			dB
V_{OS}	Output Offset Voltage	Read Mode	−460		+460	mV
		Write or Idle Mode	−20		+20	mV
V_{OCM}	Common-Mode Output Voltage	Read Mode	4.5		6.5	V
		Write or Idle Mode		5.3		V
R_{OUT}	Single-Ended Output Resistance	f = 5 MHz			30	Ω
I_L	Leakage Current, RDX, RDY	(RDX, RDY) = 6 V Write or Idle Mode	−100		100	µA
I_O	Output Current	AC Coupled Load, RDX to RDY	±2.1			mA

ELECTRICAL CHARACTERISTICS (Continued)

Unless otherwise specified $V_{DD}1 = 12V \pm 10\%$, $V_{CC} = 5V \pm 10\%$, $R_{CT} = 120\Omega \pm 5\%$, $I_W = 35mA$, $L_H = 10\mu H$, $R_D = 750\Omega$ (ML511), $f_{DATA} = 5MHz$, $0°C \leq T_A \leq 70°C$ (Notes 2 and 3).

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
SWITCHING CHARACTERISTICS						
t_{RW}	R/$\overline{W}$ to Write Switching Delay	To 90% of Write Current Output			1	µs
t_{WR}	R/$\overline{W}$ to Read Switching Delay	To 90% of 100mV, 10MHz Read Signal Envelope or to 90% Decay of Write Current			1	µs
t_{IW} or t_{IR}	$\overline{CS}$ to Select Switching Delay	To 90% of Write Current or to 90% of 100mV, 10MHz Read Signal Envelope			1	µs
t_{WI} or t_{RI}	$\overline{CS}$ to Unselect Switching Delay	To 90% Decay of 100mV, 10MHz Read Signal Envelope or to 90% Decay of Write Current			1	µs
t_{HS}	Head Select Switching Delay	To 90% of 100mV, 10MHz Read Signal Envelope			1	µs
tD1	Safe to Unsafe Write Unsafe Delay	$I_W = 35mA$	1.6		8	us
tD2	Unsafe to Safe Write Unsafe Delay	$I_W = 35mA$			1	us
tD3	Prop. Delay Head Current	$L_H = 0$, $R_H = 0$ From 50% points			25	ns
	Asymmetry Head Current	WDI has 50% Duty Cycle and 1nS Rise/Fall Time			2	ns
	Rise/Fall Head Current	10% and 90% Points			20	ns

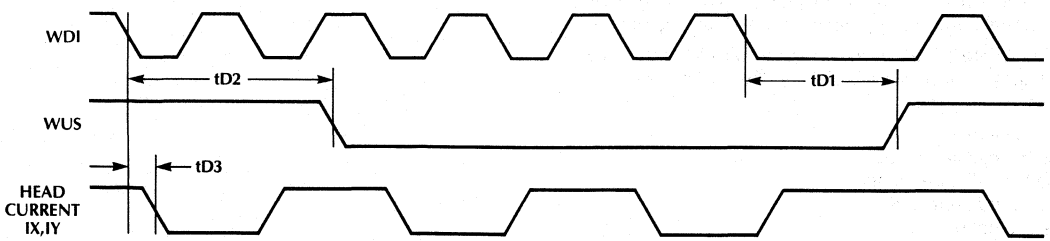
Note 1: Absolute maximum ratings are limits beyond which the life of the integrated circuit may be impaired. All voltages unless otherwise specified are measured with respect to ground.

Note 2: Limits are guaranteed by 100% testing, sampling, or correlation with worst-case test conditions.

Note 3: Maximum junction temperature (T_J) should not exceed 135°C.

5

TIMING DIAGRAM



Write Mode Timing Diagram

FUNCTIONAL DESCRIPTION

CIRCUIT OPERATION

For any selected head, the ML511 functions as a read amplifier when in the Read mode, or as a write current switch when in the Write mode. Pins HS0, HS1 and HS2 determine head selection while pin R/$\overline{W}$ controls the Read/Write mode. A detected "write-unsafe" condition is indicated by pin WUS.

READ MODE

When the ML511 is in the Read Mode, it operates as a low-noise differential amplifier on the selected channel. In Read mode the write data flip-flop is set and both the write unsafe detector and the write current source are deactivated. The center tap voltage is also lowered. Pins RDX and RDY provide differential emitter follower outputs which are in phase with the X and Y head input pins.

Note that during the Read or Chip Deselect mode the internal write current is deactivated, thus making external write current gating unnecessary.

WRITE MODE

The ML511 operates as a write-current switch when in the Write mode. Write current magnitude is determined by the following relationship:

$I_W = K/R_{WC}$

Where: K = Write Current Constant

R_{WC} = Resistance connected between pin WC and GND.

The head current is toggled between the X and Y side of the selected head by a negative transition on WDI (Write Data Input). When switching the ML511 to write mode, the WDFF (Write Data Flip-Flop) is initialized to pass write current through the X-side of the head.

The ML511, ML511R exhibit enhanced write current stability, compared to similar read/write circuits, which reduces the problem of oscillation. This is a result of increased internal write current compensation. Also, write current "glitches" during power-up, common in similar read/write circuits, are eliminated with an exclusive write current disabling function.

The WUS (Write Unsafe) pin is an open collector output that gives a logic high level for any of the following unsafe write conditions:

- Open head
- Open head center-tap
- Too low WDI frequency
- Read mode selected
- Device not selected
- No write current

Two negative transitions on WDI are required to clear WUS after the fault condition is removed.

The ML511 also offers a voltage fault detection circuit that prevents write current during power-loss or power-up.

Table 1.

Head Select

HS2	HS1	HS0	HEAD
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

0 = Logic Level Low
1 = Logic Level High
X = Don't Care

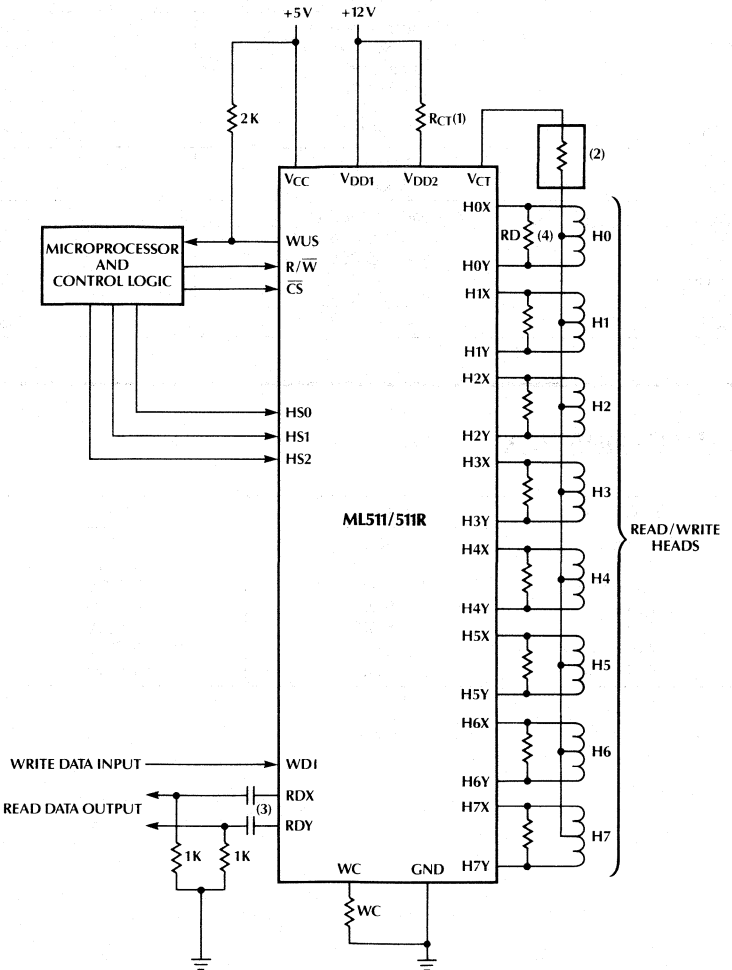
Table 2.

Mode Select

$\overline{CS}$	R/$\overline{W}$	MODE
0	0	Write
0	1	Read
1	X	Idle

0 = Logic Level Low
1 = Logic Level High
X = Don't Care

TYPICAL APPLICATION



NOTES:

1. RCT is optional and is used to limit internal power dissipation (Otherwise connect $V_{DD}1$ to $V_{DD}2$).
   RCT (1/2 Watt) = 120 (40/I_W) ohms
   where I_W = Write Current, in mA
2. Ferrite bead optional: used to suppress write current overshoot and ringing. Recommend Ferroxcube 3659065/4A6.
3. RDX and RDY load capacitance 20 pF maximum. RDX and RDY output current must be limited to 100 μA.
4. Damping resistors not required on ML511R.

ORDERING INFORMATION

PART NUMBER	PACKAGE	NUMBER OF CHANNELS
ML511-4CS	24-Lead SOIC	4
ML511R-4CS	24-Lead SOIC	4
ML511-6CP	28-Lead Molded DIP	6
ML511R-6CP	28-Lead Molded DIP	6
ML511-6CQ	28-Lead PCC	6
ML511R-6CQ	28-Lead PCC	6
ML511-6CS	28-Lead SOIC	6
ML511R-6CS	28-Lead SOIC	6
ML511R-7CS	28-Lead SOIC	7
ML511R-7CQ	28-Lead PCC	7
ML511-8CP	40-Lead Molded DIP	8
ML511R-8CP	40-Lead Molded DIP	8
ML511-8CQ	44-Lead PCC	8
ML511R-8CQ	44-Lead PCC	8
ML511-8CS	32-Lead SOIC	8
ML511R-8CS	32-Lead SOIC	8

THERMAL CHARACTERISTICS

PIN COUNT	PACKAGE	θ_{ja}
24-Lead	SOIC	75°C/W
28-Lead	PDIP	55°C/W
28-Lead	PCC	65°C/W
28-Lead	SOIC	70°C/W
32-Lead	SOIC	60°C/W
44-Lead	PCC	60°C/W
40-Lead	PDIP	45°C/W

Read Data Processor

GENERAL DESCRIPTION

The ML541 is a monolithic bipolar integrated circuit for use in a disk drive system to detect analog pulse peaks generated by the recording head during a Read operation. Connected to the read/write amplifier output, it detects valid data and provides a TTL output to the data separator for further processing. It contains both analog and digital circuitry and supports the reading of MFM and RLL encoded data at rates up to 15 megabits/second.

The primary functional blocks within the device include an AGC amplifier, a level detector, a slope detector, and output logic. Operating modes Read, Write, and Hold are selectable with input logic signals. Read mode is used for pulse peak detection during a Read operation. Write mode disables the device's ouput during a Write operation, while Hold mode holds the AGC gain constant during recovery of embedded servo information.

By using both level and slope detection, accurate pulse validation and peak time detection is acheived. The ML541 performance can be adjusted to fit particular needs through external component selection.

The ML541 is available both in a 24-pin PDIP and 28-pin PCC.

FEATURES

- Second source for SSI 541
- Data rates up to 15 megabits/second
- Supports MFM and RLL encoded read data
- 25MHz wide-bandwidth AGC amplifier
- Fast AGC region for fast transient recover
- Slow AGC region for minimum zero crossing distortion
- Write to read transient suppression
- Supports embedded servo decoding
- +5V, +12V power supplies

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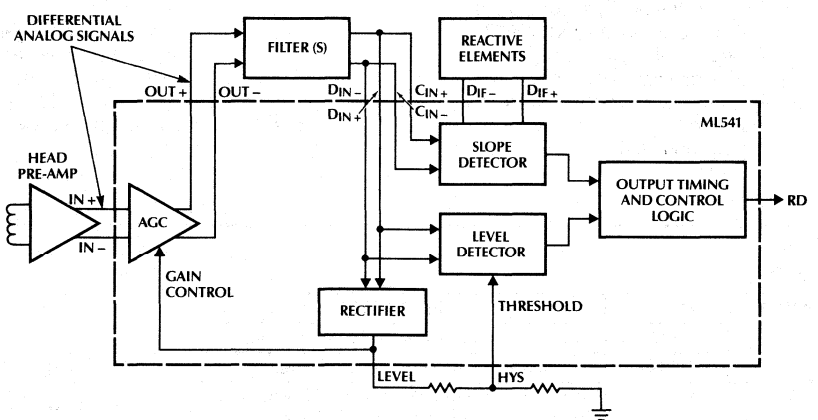
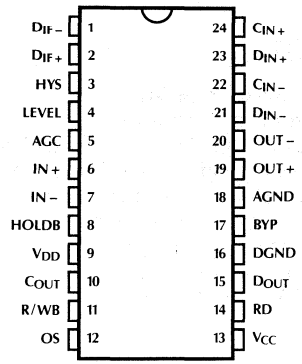
SIMPLIFIED BLOCK DIAGRAM



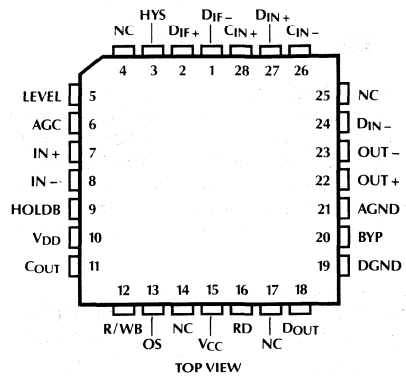
PIN CONNECTIONS

24-Pin DIP and SOIC Package



TOP VIEW

28-Pin PCC Package



TOP VIEW

PIN DESCRIPTION

NAME	FUNCTION
V_{CC}	+5V
V_{DD}	+12V
AGND	Analog Ground.
DGND	Digital Ground.
R/WB	TTL compatible Read/Write Control pin.
IN+, IN–	Analog Signal Input pins
OUT+, OUT–	AGC Amplifier Output pins
BYP	The AGC timing capacitor C_{AGC} is tied between this pin and AGND.
HOLDB	TTL compatible pin that holds the AGC gain when pulled low.
AGC	Reference input voltage level for the AGC circuit.
D_{IN+}, D_{IN-}	Analog input to the hysteresis comparator.

NAME	FUNCTION
HYS	Input for setting hysteresis level of the hysteresis comparator.
LEVEL	Provides rectified signal level for input to the hysteresis comparator.
D_{OUT}	Buffered test point for monitoring D input of the flip-flop.
C_{IN+}, C_{IN-}	Analog input to the differentiator.
D_{IF+}, D_{IF-}	External differentiating network connection pins.
C_{OUT}	Buffered test point for monitoring the clock input to the flip-flop.
OS	Connection for read output pulse width setting capacitor C_{OS}.
RD	TTL compatible read output.

TABLE 1 MODE SELECT

R/WB	HOLDB	MODE	DESCRIPTION
1	1	READ	AGC amp section active, Digital section active.
1	0	HOLD	AGC gain constant, Digital section active.
0	X	WRITE	AGC gain maximum, Digital section inactive, Input common mode resistance reduced.

0 = Logic level low
1 = Logic level high
X = Don't care

ABSOLUTE MAXIMUM RATINGS

(Note 1)

Power Supply Voltage Range
- V_{CC} ..... −0.3 to 6 V_{DC}
- V_{DD} ..... −0.3 to 14 V_{DC}

Terminal Voltage Range
- R/WB, IN+, IN−, HOLDB ..... −0.3 V to V_{CC} +0.3 V
- RD ..... −0.3 V to V_{CC} +0.3 V or +12 mA
- All others ..... −0.3 V to V_{DD} +0.3 V

Storage Temperature Range ..... −65°C to +150°C

Junction Temperature (T_J) ..... +135°C

Lead Temperature (Soldering, 10 sec) ..... 260°C

OPERATING CONDITIONS

Supply Voltage
- V_{CC} ..... 5 V ± 10%
- V_{DD} ..... 12 V ± 10%

$V_{(CIN+}-C_{IN-)}$, $V_{(DIN+}-D_{IN-)}$ ..... 1 V_{P-P}

V_{HYS} ..... 1.0 V

C_{OS} ..... 50 to 200 pF

Typical Component Values (Refer to Typical Applications)
- C_{IN} ..... 0.001 µF
- C_S ..... 0.01 µF
- C_{OUT} ..... 0.0047 µF
- R_{OUT} ..... 400 Ω
- C_{AGC1} ..... 220 pF
- C_{AGC2} ..... 2000 pF
- R_{AGC} ..... 2.21 kΩ
- C_{LEVEL} ..... 150 pF
- R_{LEVEL1} ..... 1.54 kΩ
- R_{LEVEL2} ..... 6.49 kΩ
- C_{OS} ..... 50 pF

ELECTRICAL CHARACTERISTICS

The following specifications apply over the recommended operating conditions of V_{CC} = 5 V ± 10%, V_{DD} = 12 V ± 10%, 0°C < T_A < 70°C and external components as specified under recommended operating conditions unless otherwise specified. (See Note 2.)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP NOTE 5	MAX	UNITS
DC Characteristics						
I_{CC}	V_{CC} Supply Current	Outputs unloaded			14	mA
I_{DD}	V_{DD} Supply Current	Outputs unloaded			70	mA
P_D	Power Dissipation	Outputs unloaded, T_A = 70°C			930	mW
Digital Inputs Characteristics (HOLDB, R/WB)						
V_{IH}	High Voltage		2			V
V_{IL}	Low Voltage				0.8	V
I_{IH}	High Current	V_{IH} = 2.4 V			100	µA
I_{IL}	Low Current	V_{IL} = 0.4 V	−0.4			mA
Digital Outputs Characteristics (C_{OUT}, RD)						
V_{OL}	Output Low Voltage	I_{OL} = 4 mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} = 400 µA	2.4			V
WRITE AND HOLD MODE CHARACTERISTICS						
Mode Control						
t_{RW}	Read to Write Transition Time				1	µs
t_{WR}	Write to Read Transition Time	AGC settling not included, time to high input resistance	1.2		3	µs
t_{RH}	Read to Hold Transition Time				1	µs
Write Mode						
Z_{IC}	Common Mode Input Impedance (both sides)	R/WB pin = low		250		Ω

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ELECTRICAL CHARACTERISTICS (Continued)

The following specifications apply over the recommended operating conditions of $V_{CC} = 5V \pm 10\%$, $V_{DD} = 12V \pm 10\%$, $0°C \leq T_A \leq 70°C$, IN+ and IN− AC coupled, OUT+ and OUT− differentially loaded with $>600\Omega$ and each side loaded with $<10pF$ to GND, $C_{BYP} = 2000pF$, OUT+ and OUT− AC coupled to D_{IN+} and D_{IN-} respectively, $V_{AGC} = 2.2V$ unless otherwise specified. (See Note 2.)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP NOTE 5	MAX	UNITS
READ MODE CHARACTERISICS						
AGC Amplifier						
R_{ID}	Differential Input Resistance	$V_{(IN+-IN-)} = 100mV_{P-P}$ @ 2.5MHz		5		kΩ
C_{ID}	Differential Input Capacitance	$V_{(IN+-IN-)} = 100mV_{P-P}$ @ 2.5MHz			10	pF
Z_{IC}	Common Mode Input Impedance (both sides)	R/WB pin high		1.8		kΩ
		R/WB pin low		0.25		kΩ
A_{VR}	Gain Range	$1V_{P-P} \leq V_{OUT\ diff} < 2.5V_{P-P}$	4		83	V/V
e_N	Input Noise Voltage	Gain set to maximum			30	nV/ $\sqrt{Hz}$
BW	Bandwidth	Gain set to maximum, −3dB point	25			MHz
V_{OP}	Maximum Output Voltage Swing	Set by V_{AGC}	3			V_{P-P}
I_{OD}	OUT+ to OUT− Pin Current	No DC path to GND, See Note 3	±3.2			mA
R_O	Output Resistance			20	30	Ω
C_O	Output Capacitance			12		pF
V_{IP} / V_{AGC}	$(D_{IN+} - D_{IN-})$ Input Voltage Swing VS AGC Input Level	$30mV_{P-P} \leq V_{(IN+-IN-)} \leq 550mV_{P-P}$, $1.5V \leq V_{AGC} \leq 3.75V$		0.48		V_{P-P}/V
V_{IP}	$(D_{IN+} - D_{IN-})$ Input Voltage Swing Variation	$30mV_{P-P} < V_{(IN+-IN-)} < 550mV_{P-P}$, AGC Fixed, over supply and temp.			+8	%
t_D	Gain Decay Time	See Figure 1a; $V_{IN} = 300mV_{P-P}$ then $>150mV_{P-P}$ at 2.5MHz, V_{OUT} to 90% of final value.		50		µs
t_A	Gain Attack Time	See Figure 1b; from Write to Read transition to V_{OUT} at 110% of final value, $V_{IN} = 400mV_{P-P}$ @ 2.5MHz		4		µs
I_{AGCfc}	Fast AGC Capacitor Charge Current	$V_{(D_{IN+}-D_{IN-})} = 1.6V$, $V_{AGC} = 3.0V$		1.5		mA
I_{AGCsc}	Slow AGC Capacitor Charge Current	$V_{(D_{IN+}-D_{IN-})} = 1.6V$, Vary V_{AGC} until slow discharge begins		0.17		mA
	Fast to Slow Attack Switchover Point	$V_{(D_{IN+}-D_{IN-})}$		1.25		–
		$V_{(D_{IN+}-D_{IN-})}$ Final				
I_{AGCD}	AGC Capacitor Discharge Current	$V_{(D_{IN+}-D_{IN-})} = 0.0V$ Read Mode		4.5		µA
		Hold Mode	−0.2		+0.2	µA
CMRR	CMRR (Input Referred)	$V_{IN+} = V_{IN-} = 100mV_{P-P}$ @ 5MHz, gain at max.	40			dB
PSRR	PSRR (Input Referred)	V_{CC} or $V_{DD} = 100mV_{P-P}$ @ 5MHz, gain at max.	30			dB
Hysteresis Comparator						
V_{IP}	Input Signal Range				1.5	V_{P-P}
R_{ID}	Differential Input Resistance	$V_{(D_{IN+}-D_{IN-})} = 100mV_{P-P}$ @ 2.5MHz	5		15	kΩ
C_{ID}	Differential Input Capacitance	$V_{(D_{IN+}-D_{IN-})} = 100mV_{P-P}$ @ 2.5MHz			6.0	pF
Z_{IC}	Common Mode Input Impedance	(both sides)		2.0		kΩ
V_{IO}	Comparator Offset Voltage	HYS pin at −0.5V, ≤1.5kΩ across D_{IN+}, D_{IN-}		5		mV

ELECTRICAL CHARACTERISTICS (Continued)

The following specifications apply over the recommended operating conditions of $V_{CC} = 5V \pm 10\%$, $V_{DD} = 12V \pm 10\%$, $0°C \leq T_A \leq 70°C$, IN+ and IN− AC coupled, OUT+ and OUT− differentially loaded with >600Ω and each side loaded with <10pF to GND, $C_{BYP} = 2000pF$, OUT+ and OUT− AC coupled to D_{IN+} and D_{IN-} respectively, $V_{AGC} = 2.2V$ unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
READ MODE CHARACTERISICS (Continued)						
Hysteresis Comparator (Continued)						
V_{HYSP} V_{HYS}	Peak Hysteresis Voltage vs HYS pin voltage (input referred)	$1V < V_{HYS} < 3V$		0.21		V/V
I_I	HYS Pin Input Current	$1V < V_{HYS} < 3V$	0		−20	µA
I_O	LEVEL Pin Max Output Current		3			mA
R_O	LEVEL Pin Output Resistance	$I_{LEVEL} = 0.5mA$		180		Ω
V_{OL}	D_{OUT} Pin Output Low Voltage	$T_A = 70°C$	$V_{DD} - 4.0$		$V_{DD} - 2.5$	V
V_{OH}	D_{OUT} Pin Output High Voltage	$T_A = 70°C$	$V_{DD} - 2.2$		$V_{DD} - 1.5$	V
V_{OL}	D_{OUT} Pin Output Low Voltage	$T_A = 25°C$	$V_{DD} - 4.0$		$V_{DD} - 2.8$	V
V_{OH}	D_{OUT} Pin Output High Voltage	$T_A = 25°C$	$V_{DD} - 2.5$		$V_{DD} - 1.6$	V
Active Differentiator						
V_{IP}	Input Signal Range				1.5	V_{P-P}
R_{ID}	Differential Input Resistance	$V_{(C_{IN+}-C_{IN-})} = 100mV_{P-P}$ @ 2.5MHz	5		15	kΩ
C_{ID}	Differential Input Capacitance	$V_{(C_{IN+}-C_{IN-})} = 100mV_{P-P}$ @ 2.5MHz			6	pF
Z_{IC}	Common Mode Input Impedance	(both sides)		2.0		kΩ
I_{OD}	D_{IF+} to D_{IF-} Pin Current	Differentiator Imped must be set so as not to clip signal at this current level	±1.3			mA
V_{IO}	Comparator Offset Voltage	D_{IF+}, D_{IF-} AC Coupled		5		mV
V_{OL}	C_{OUT} Pin Output Low Voltage	$0 \leq I_{OH} \leq 0.5mA$		$V_{DD} - 3$		V
V_{PO}	C_{OUT} Pin Output Pulse Voltage	$0 \leq I_{OH} \leq 0.5mA$		0.4		V
PW_0	C_{OUT} Pin Output Pulse Width	$0 \leq I_{OH} \leq 0.5mA$		30		ns

The following specifications apply over the recommended operating conditions of $V_{CC} = 5V \pm 10\%$, $V_{DD} = 12V \pm 10\%$, $0°C \leq T_A \leq 70°C$, $V_{(C_{IN+}-C_{IN-})} = V_{(D_{IN+}-D_{IN-})} = 1.0V_{P-P}$ AC coupled sine wave at 2.5MHz, $R_{D_{IF}} = 100Ω$, $C_{D_{IF}} = 65pF$, $V_{HYS} = 1.8V$, $C_{OS} = 60pF$, 4kΩ to V_{CC} and 10pF to GND on pin RD unless otherwise specified.

Output Data Characteristics (Refer to Figure 2)						
t_{D1}	D-Flip-Flop Set Up Time	Min delay from $V_{(D_{IN+}-D_{IN-})}$ exceeding threshold to $V_{(D_{IF+}-D_{IF-})}$ reaching a peak	0			ns
t_{D3}	Propagation Delay				110	ns
t_{D5}	Output Data Pulse Width	$T_A = 25°C$, $V_{CC} = 5V$, $V_{DD} = 12V$		±15%		
t_{D5}	Output Data Pulse Width Variation	$C_{OS} = 60pF$, See Note 4	30		80	ns
t_{D3}-t_{D4}	Logic Skew (Pulse Pairing)				3	ns
t_R	Output Rise Time	$V_{OH} = 2.4V$			18	ns
t_F	Output Fall Time	$V_{OL} = 0.4V$			14	ns

Note 1: Absolute maximum ratings are limits beyond which the life of the integrated circuit may be impaired. All voltages unless otherwise specified are measured with respect to ground.

Note 2: Limits are guaranteed by 100% testing, sampling, or correlation with worst-case test conditions.

Note 3: AGC amplifier output current may be increased as in Figure 4.

Note 4: $t_{D5} \cong 770\ (C_{OS})$, $50pF < C_{OS} < 150pF$.

Note 5: Typicals are parametric norm at 25°C

FUNCTIONAL DESCRIPTION

Operating Modes

The ML541 has three definitive operation modes which are: Read mode, Write mode and Hold mode. These modes are defined by input pins HOLDB and R/WB as shown in Table 1. Read mode, the mode used normally for pulse detection, is assumed in the following sections unless otherwise noted.

AGC Amplifier Section

The purpose of the AGC amplifier is to provide a constant read signal level for both the level and slope detectors. Full differential processing of the read signal is used to minimize noise and distortion in the analog signal. A wide gain range is required due to large signal variation when moving the recording head from an inside to outside data track or variations in media.

The differential output voltage level V_{OUT} from the AGC amp is determined by voltage V_{AGC} present at pin AGC. V_{OUT} is full wave rectified and compared against V_{AGC} to create charge/discharge current for capacitor C_{BYP} connected at pin BYP. Voltage V_{BYP} across C_{BYP} controls the gain in the AGC amplifier.

Two distinct values of I_{BYP} are possible which determine a fast and slow AGC gain response attack rate. When V_{OUT} is more than 125% of the set level a high value of I_{BYP} is sourced which provides a fast AGC attack rate. When V_{OUT} is within 100% to 125% of the set level a reduced value of I_{BYP} is sourced which provides a slower attack rate. The fast-slow gain response attack rates provides for an initial quick system response and then minimum zero crossing distortion of the analog signal once the gain is within working range. V_{AGC} should be set so that the differential input voltage V_{DIN} into the level comparator is $1V_{P\text{-}P}$ at nominal Read signal conditions. The AGC amp section gain is given by:

$$\frac{A_{V2}}{A_{V1}} = \exp \frac{V_{BYP2} - V_{BYP1}}{5.8 \times V_T}$$

Where: A_{V1}, A_{V2} are initial and final amplifier gain values corresponding to initial and final V_{BYP} values.

$V_T = (KT)/Q = 26\,mV$ at room temperature.

The AGC amp's differential inputs must be AC coupled to the read amplifier (ML117, ML501, etc.) differential outputs. Similarly, AC coupling must be used at the AGC amp outputs.

AGC Amp During Write Mode — When the ML541 is put into write mode, the AGC amp's input impedance is lowered to allow a faster dampening of the Write to Read transient from the head pre-amp. The AGC gain is also set to maximum gain so that fast AGC attack will occur when changing back to the Read mode. Internal device timing is controlled so that settling occurs prior to Read mode activation. Minimal value input coupling capacitors should be chosen to reduce settling time, however, bandwidth requirements also need to be considered.

AGC Amp During Hold Mode — During the Hold mode, the charge/discharge current driving pin BYP is internally disconnected. AGC compensation capacitor C_{AGC} will then hold the present gain setting. The amplitude of V_{OUT} will therefore not affect the AGC gain and gain will remain constant.

Hold mode is used so that AGC gain will not be adjusted when embedded servo information is read. This prevents loosing the pulse peak amplitude information needed during position decoding, or creating additional gain settling time when again reading data. Embedded servo pulses are normally taken at outputs D_{IF-} and D_{IF+}, as shown in the typical application.

External Filter Network

Filtering for the level and slope detectors can be performed with a single filter or two separate filters. If separate filters are used, care must be used to insure that time delays are matched. A multi-pole Bessell filter is recommended due to the group delay and linear phase characteristics.

Level Detector

The full wave rectified V_{OUT} is buffered and available at pin LEVEL. The level detector uses a hysteresis comparator to compare the processed read signal amplitude against a reference voltage derived from voltage V_{LEVEL} output from pin LEVEL. Using V_{LEVEL} provides a feed-forward function that allows valid level detection to be performed prior to AGC amp gain settling. The level detector hysteresis value is set in a way that will only allow relatively large read pulse peaks (negative or positive) to be detected.

Slope Detector

The slope detector uses an external reactive component network to produce a voltage signal proportional to the differential of the read signal. By using a hysteresis comparator to detect zero slope of the read signal, the time occurrence of positive or negative read pulse peak values can be determined.

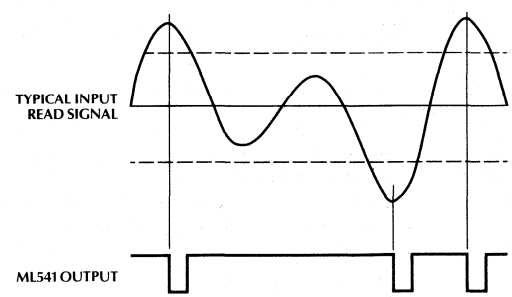
An external reactive network, shown in the Typical Application, is used between the D_{IF+} and D_{IF-} pins to provide the differential function given by:

$$A_V = \frac{-2000Cs}{LCs^2 + (R + 92)\,Cs + 1}$$

Where: C = External capacitor (20 pF to 150 pF)
L = External inductor
R = External resistor
$s = j\omega = j2\pi f$

Output Logic

The output logic provides a negative TTL pulse at pin RD which begins at the peak of a valid read pulse, as shown below.

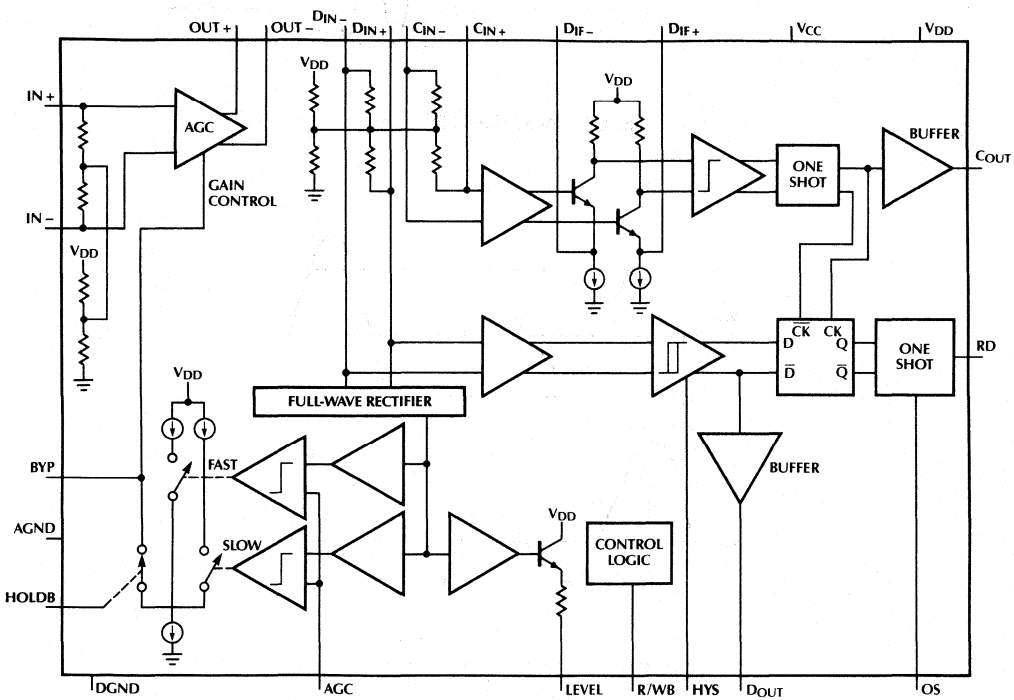


Pin R/WB must be high for the output logic to be active. The key element in the output logic is the D flip-flop. The flip-flop is clocked by the slope detector at the time of a zero crossing, which loads data from level detector. The flip-flop inputs only change state when the level detector detects a peak amplitude of a polarity opposite to the previous valid peak. Thus, through the output logic the slope detector determines output timing and the level detector determines pulse validity.

Layout Considerations

As with any high gain, wide bandwidth analog circuitry, care needs to be exercised in PC layout. Power supply and ground lines should be bypassed and well isolated from other circuitry. A ground plane is recommended, as is keeping analog lines short and well balanced to prevent interaction with nearby circuitry in the disk drive.

BLOCK DIAGRAM



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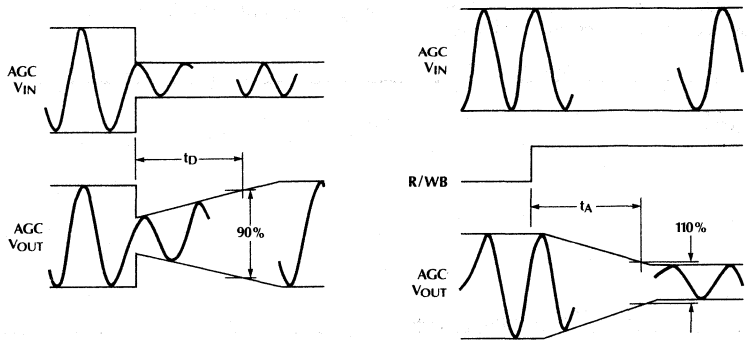


Figure 1. AGC Timing Diagram

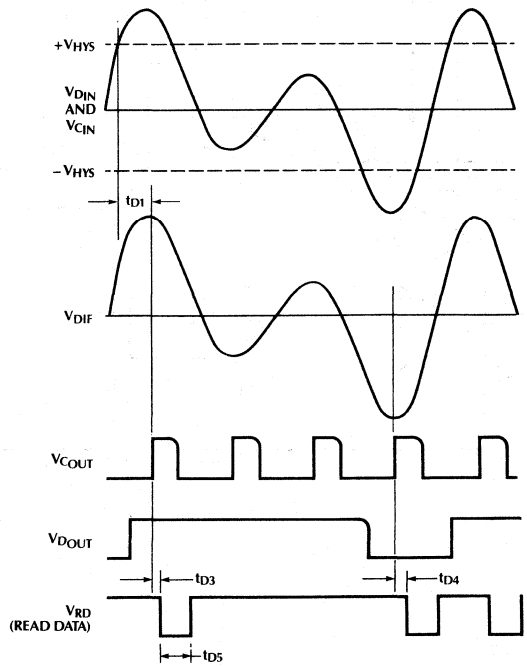


Figure 2. Output Logic Timing Diagram

TYPICAL APPLICATIONS

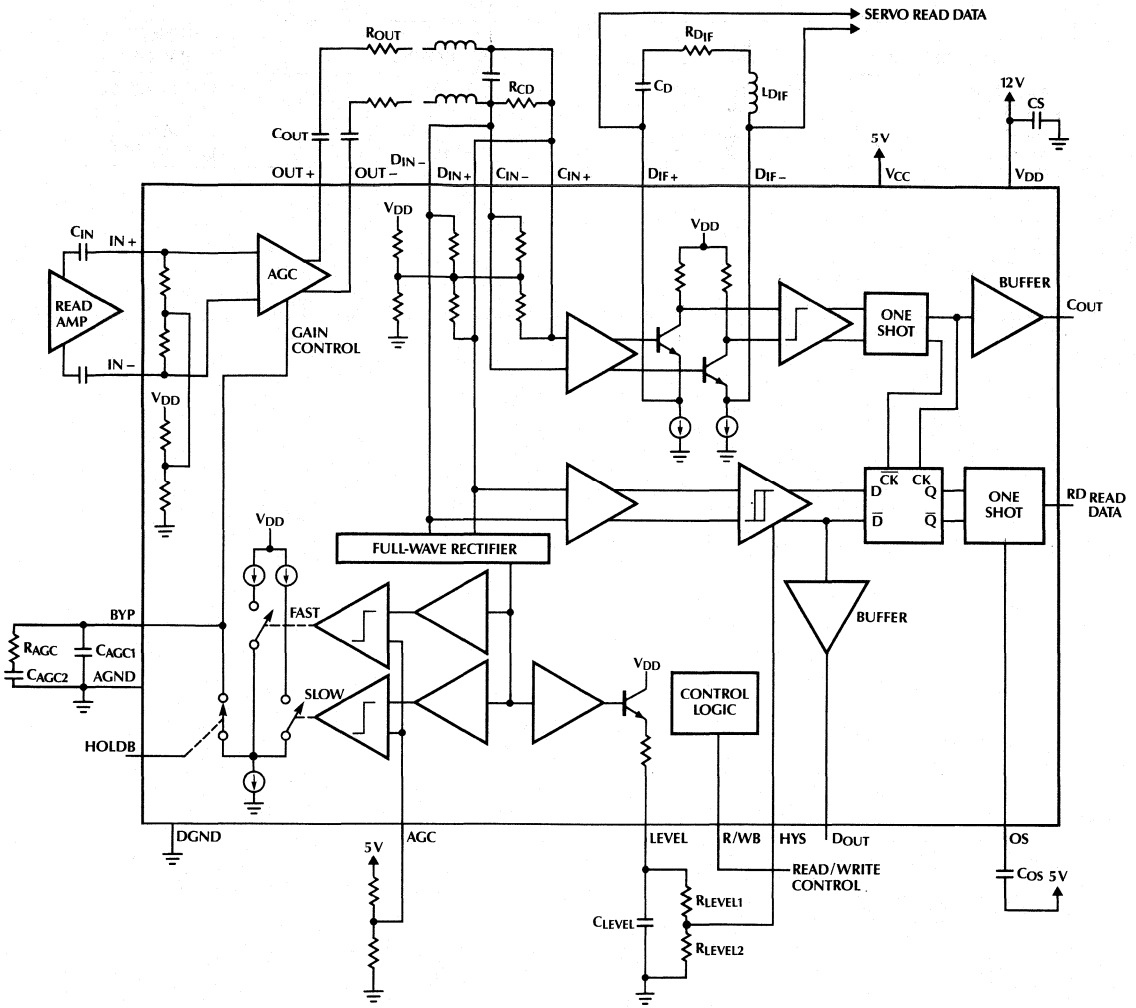


Figure 3. Typical Application Diagram

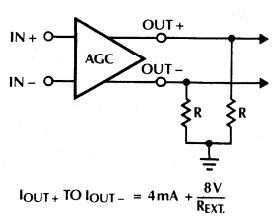


Figure 4. Modification of AGC Amplifier Output to Drive Low Impedance Filters

ORDERING INFORMATION

PART NUMBER	PACKAGE	PIN COUNT	TEMPERATURE RANGE
ML541CP	Plastic DIP	24 PINS	0°C to +70°C
ML541CJ	Ceramic DIP	24 PINS	0°C to +70°C
ML541CQ	Plastic PCC	28 PINS	0°C to +70°C
ML541CS	SOIC	24 PINS	0°C to +70°C

Micro Linear

ML4025

Data Separator

GENERAL DESCRIPTION

The ML4025 provides the data separator function for RLL encoded magnetic or optical disk drive systems. Its primary function is to extract the clock information from a serial bitstream, and use this clock signal to synchronize the bitstream and clock it into an external decoder. This data and clock separation is achieved with a special function phase lock loop (PLL) circuit.

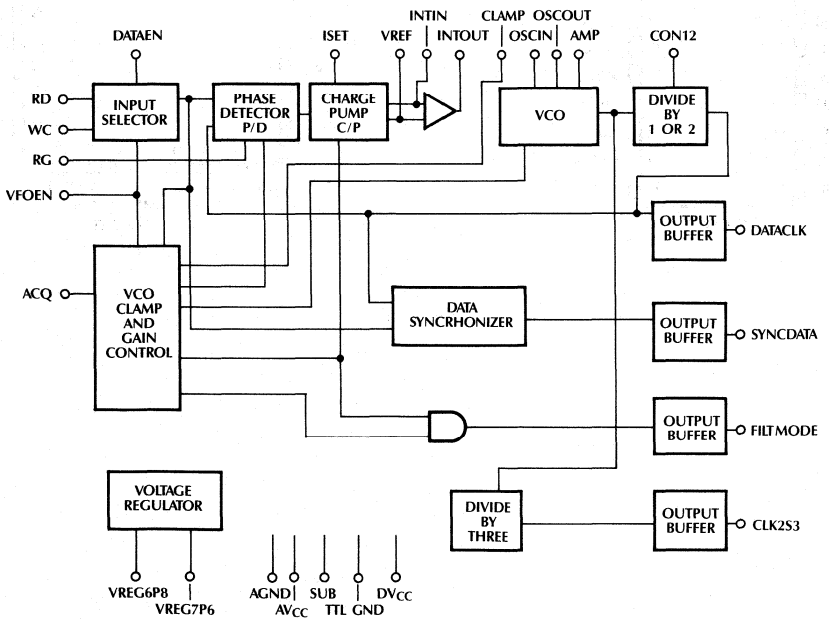
In addition, the ML4025 provides a 2/3 clock output for use with RLL (1, 7) codes. This eliminates the external circuitry that is required when using other similar data separators.

The special function PLL consists of a dual mode phase detector, a charge pump, a buffer amplifier, a voltage controlled oscillator (VCO), and an external loop filter. The PLL operates in two distinct modes, high gain for rapid acquisition, and low gain for minimum jitter after lock.

FEATURES

- Data rates up to 33 Mbits/sec
- No adjustments necessary
- Compatible with all drives and controllers
- Provides 2/3 rate clock on chip for RLL(1, 7) codes
- Eliminates false glitches on data clock output during read to write transitions
- Utilizes ECL technology for lower noise and phase jitter
- Precision high Q oscillator with external LC for low phase noise
- Zero phase error startup of VCO

BLOCK DIAGRAM



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GENERAL DESCRIPTION (Continued)

In addition to the PLL the ML4025 has an input selector, VCO clamp and restart sequencer, gain control, voltage regulator, data synchronizer, clock divide, and output buffers.

The VCO clamp and restart sequencer is used to stop the oscillator and then restart it in-phase with the bitstream. This provides a zero phase error startup mode for consistent and optimum phase acquisition. This circuit also eliminates the possibility of short pulse widths that might otherwise occur on the data clock during write to read transitions.

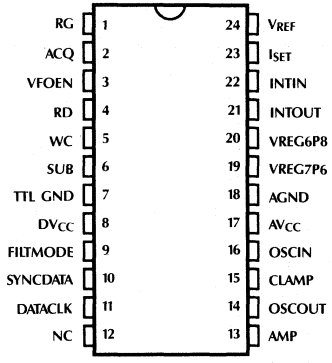
Low phase jitter operation is achieved by utilizing ECL logic which minimizes noise coupling into the sensitive analog circuits. In addition, the on board voltage reference rejects power supply noise to further enhance the low phase jitter operation. This reference provides stable device operation over the full temperature and power supply range.

External components set the center frequency and dynamic range of the voltage controlled oscillator. This allows the system engineer to achieve an optimum configuration for virtually any drive application. Performance can be even further optimized by using the FILTMODE output to modify the external loop filter components for maximum performance in both high and low gain modes.

The ML4025 implements the complete high performance data separator function in SCSI, ESDI, SMD, and ST506 type interfaces and drives.

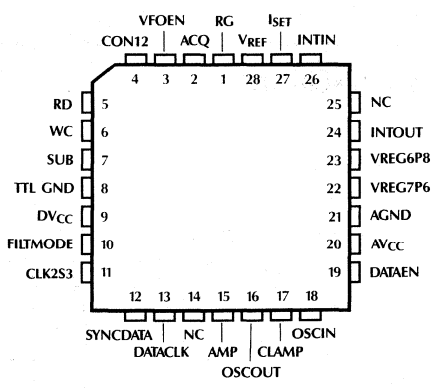
PIN CONFIGURATIONS

ML4025
24-Pin DIP
(Prototypes Only)



TOP VIEW

ML4025
28-Pin PCC



TOP VIEW

PIN DESCRIPTION

NAME	FUNCTION
RG	READ GATE: Selects the phase or frequency mode of the phase detector. RG may be tied to VFOEN input when VFOEN is used in the level mode. RG should preferably be set at, or prior to, a change in VFOEN. Logic 1 allows the phase detector to run in the phase mode (data read) or to progress sequentially from the frequency mode to the phase mode. Logic 0 forces the phase detector to run in the frequency mode.
ACQ	ACQUIRE: Controls the high/low gain state of the charge pump. Logic 1 allows the charge pump to switch to high gain with a change in VFOEN and to synchronously switch to low gain after approximately 37 pulses at the selected input; i.e., either RD or WC. If the charge pump is in high gain, switching to logic 0 immediately terminates the internal pulse count and causes the charge pump to synchronously switch to low gain. Tying ACQ to RG provides a means for enabling high gain acquisition in the phase mode only. Logic 0 forces a low gain charge pump.
VFOEN	VFO ENABLE: Used to select RD or WC as the input channel. The transition from 1 to 0, or 0 to 1, initiates the oscillator clamp, zero-phase error startup sequence, as well as the charge pump gain change sequence (if allowed, via the ACQ input). A positive or negative pulse of width 1 to 3 oscillator periods may be used as the VFOEN input. In this mode, the RD and WC inputs must be tied together with an external data selector. Logic 1 selects the RD input. Logic 0 selects the WC input.
RD	READ DATA: The raw encoded data from the drive read channel. The ML4025 is triggered by the rising edge of the data on the RD input when VFOEN is in the logic 1 state.
WC	WRITE CLOCK: This is a 50% duty-cycle input which is at the frequency of the oscillator used to write data onto the drive or, alternately, an oscillator at the appropriate frequency generated from a clock track on the disk drive. This input is used to allow the PLL to track the nominal data frequency when RD is not available. The ML4025 is falling edge triggered by the signal at the WC input when VFOEN is in the logic 0 state.
SUB	SUBSTRATE AND ECL GROUND: All three ground pins, SUB, TTL GND, and AGND should be tied together.

NAME	FUNCTION
TTL GND	OUTPUT DIGITAL GROUND (common external ground): See SUB pin.
DV_{CC}	DIGITAL SUPPLY.
FILTMODE	FILTER MODE: The FILTMODE output is logic 1 when the phase detector is in the phase mode and the charge pump is in low gain. Otherwise, it is logic 0. The FILTMODE output may be used to modify the PLL filter when switching from high to low gain at the transition from acquisition to tracking (data read) mode.
SYNCDATA	SYNCHRONIZED DATA: This is the synchronized (standardized) data output.
DATACLK	DATA CLOCK: The falling edge of this output clocks SYNCDATA.
AMP	OSCILLATOR AMPLITUDE: Oscillator AGC loop rate capacitor.
OSCOUT	OSCILLATOR OUT: Oscillator current drive.
CLAMP	OSCILLATOR CLAMP: Oscillator clamp voltage source.
OSCIN	OSCILLATOR IN: Oscillator input.
DATAEN	DATA ENABLE (Coast): A low forces the charge pump to ignore incoming data. This pin defaults high.
AV_{CC}	ANALOG SUPPLY.
AGND	ANALOG GROUND (common external ground): See SUB pin.
VREG7P6	VREG 7.6V: Internally regulated supply, brought out for filter capacitor only.
VREG6P8	VREG 6.8V: Internally regulated supply, brought out for filter capacitor and to set the charge pump bias current.
INTOUT	INTEGRATOR OUTPUT: Output of buffer amplifier.
INTIN	INTEGRATOR INPUT: Inverting input to buffer amplifier.
I_{SET}	CURRENT SET: Charge pump bias current set by external resistor.
V_{REF}	VOLTAGE REFERENCE: Internally generated reference for integrator, brought out for filter capacitor only.
CON12	CONTROL INPUT: Selects the divide by ratio of the divide by one/divide by two circuit. Selects the divide by two when connected to DV_{CC} and selects divide by one or pass through when connected to SUB. When used as divide by two the oscillator frequency should be twice the incoming data rate. This pin defaults low.
CLK2S3	2/3 CLOCK OUTPUT: When the oscillator is set to twice the data rate and CON12 is logic 0, a 2/3 rate clock output is provided for RLL (1, 7) coding.

5

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage, AV_{CC} 14V
Power Supply Voltage, DV_{CC} 7V
Input Voltage Range Positive ..... DV_{CC} + 0.2V
Input Voltage Range Negative ..... –0.2V
Voltage Difference SUB to TTL GND ..... ±0.3V
Storage Temperature Range ..... –65° to +150°
Junction Temperature (T_J) ..... TBD (Note 1)
Lead Temperature (Soldering, 10 sec) ..... 260°

OPERATING CONDITIONS

Temperature Range ..... 0° to +70°
Supply Voltage, DV_{CC} ..... 5V ± 5%
Supply Voltage, AV_{CC} ..... 9.5V to 12.6V

Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied. (All voltages referenced to SUB unless otherwise specified.)

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, AV_{CC} = 12V, DV_{CC} = 5V, T_A = Room

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
AV_{CC}	Analog Supply Voltage		9.5	12.0	12.6	V
AI_{CC}	Analog Supply Current			35		mA
DV_{CC}	Digital Supply Voltage		4.75	5.0	5.25	V
DI_{CC}	Digital Supply Current			95		mA
	Analog to TTL Ground Diff		–0.2		0.2	V
f_{MAX}	Maximum Operating Frequency		66			MHz
f_{OMAX}	Maximum Oscillator Frequency	Appropriate External Components	100			MHz
OA	Oscillator Amplitude		400	500	600	mV_{P-P}
V_{IL}	Input Low Voltage				0.8	V
V_{IH}	Input High Voltage		2.0			V
I_{IL}	Input Low Current	DV_{CC} = 5.25V, V_I = 0.4V			–0.4	mA
I_{IH}	Input High Current	DV_{CC} = 5.25V, V_I = 2.4V			20	µA
V_{OL}	Output Low Voltage	I_{CL} = 3.2mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} = 400µA	3.4			V
CPL	Charge Pump Rate	Low Gain Charging Low Gain Discharging	300 600	325 650	335 670	µA µA
CPH	Charge Pump Rate	High Gain	1.20	1.30	1.34	mA
CPE	Clamp Release Phase Error	Phase Mode, t_{OSC} = OSC Period (ns)	–2		+2	ns
LRPDCP	Phase Detector Charge Pump Linear Range		$-\pi$		$+\pi$	rad
PEPD	Phase Detector Phase Discrimination Error		$-4\pi/t_{OSC}$		$+4\pi/t_{OSC}$	rad
V_{OLB}	Buffer, Integrator Output Low Voltage		.3	.6	.8	V
V_{OLH}	Buffer, Integrator Output High Voltage		6.1	6.4	6.8	V
BW_B	Buffer, Integrator Bandwidth		5.0			MHz
I_{IB}	Buffer Input Bias Current		.1			µA
UDS	Data Sep. Uncertainty	$t_{OSC} = 1/f_{OSC}$		$.05 \times t_{OSC}$		
SDLDC	SYNCDATA Leading DATACLK	f_{OSC} = 30MHz	10.0	19.0	25.0	ns

Note 1: The supply currents (AI_{CC} and DI_{CC}) exhibit a negative TC; preliminary calculations suggest a maximum T_J of 133°C.

FUNCTIONAL DESCRIPTION

The ML4025 extracts the clock from a serial bitstream and uses that clock to synchronize the bitstream into a decoder like the AIC-270. This is accomplished by phase locking the voltage controlled oscillator (VCO) to the incoming data. The VCO is synchronized to the average incoming frequency of the bitstream. The VCO frequency is equivalent to the clock frequency of the data. The unsynchronized data is gated with this clock signal to create synchronized data.

The following is a description of the functional blocks of the ML4025.

INPUT SELECTOR

This block directs either the Read Data (RD) or the Write Clock (WC) signal to the phase detector block depending on the level of the control signal VFOEN. If VFOEN is low the Write Clock is selected and if VFOEN is high then the Read Data is selected. The selected signal is synchronized to the rising edge of the VFOEN signal and supplied to the gain control block.

If an external input selector is used or the input selector function is not required, the RD and WC inputs should be tied together.

PHASE DETECTOR

This block compares the phase of the incoming signal with the phase of the VCO and outputs a signal to the charge pump block which is proportional to this difference. In the phase mode, the phase detector provides a window, which is set by the oscillator, and leads the oscillator by ½ period. This establishes a balanced ±180 degree phase detection window and eliminates the need for delay lines used in alternative designs.

CHARGE PUMP

The charge pump converts the phase difference error signal from the phase detector to a bidirectional current at the INTIN pin. This output current is proportional to the phase difference between the oscillator and the input data. The charge pump block has two possible gain settings which are set by a signal from the gain control block.

AMPLIFIER

This buffer stage between the charge pump and the external filter circuit is configured with an external capacitor network as an integrator. It filters the pulse variations of the charge pump. It also provides a lower impedance output to drive the oscillator filter connector. This operational amplifier has a very low input bias current to minimize the discharge current loading on the loop filter. The amplifier has internal frequency compensation for stable operation.

GAIN CONTROL

This block provides the timing control signals to the phase detector and the charge pump circuits for selecting between the high and low gain modes. When a VFOEN transition occurs with a logic high at ACQ the high gain mode of the charge pump is set. This high gain is maintained for approximately 37 pulses of the RD or WR input signals. After this time period the gain control resets the charge pump to the low gain mode.

VCO

The voltage controlled oscillator (VCO) is a gain controlled feedback oscillator with the center frequency set by an external LC network. The capacitance portion of this network consists of a varactor and a fixed capacitor. The external components set the oscillator dynamic range and therefore the PLL capture range as well as center frequency.

VCO CLAMP AND RESTART

The clamp circuitry stops the oscillator when the VFOEN signal changes state. The oscillator is then restarted in-phase with the input clock after a 3 bit time period.

DATA SYNCHRONIZER

This block synchronizes the incoming data to the clock information extracted by the PLL circuitry. The data and the clock information are both provided as outputs with the edges synchronized.

DIVIDE BY TWO/ONE

This block can be controlled to be a divide by two or a pass through (divide by one) function. When the divide by two mode is selected the VCO nominal frequency should typically be set to twice the nominal data rate. This assures that the data clock and the feedback signal to the phase detector have a 50% duty cycle. This is an additional block not provided in the AIC6225.

DIVIDE BY THREE

This divide by three function is provided to supply a 2/3 rate clock signal (when used with the VCO running at twice the nominal speed) that can be used with RLL (1, 7) coding schemes. This is an additional block not provided in the AIC6225.

OUTPUT BUFFERS

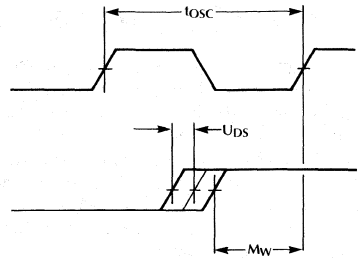
These blocks are TTL compatible buffers for the DATACLK, SYNCDATA, FILTMODE, and CLK2S3 output signals.

VOLTAGE REFERENCE

This block generates the required internal references including 6.8 volt and 7.6 volt outputs that are used with an external resistor to set the reference current for the charge pump. The voltage reference utilizes an accurate bandgap circuit to provide a stable bias voltages and increased power supply rejection for the circuits on the chip.

DATA SEPARATOR UNCERTAINTY AND AVAILABLE WINDOW MARGIN

Data Separator Uncertainty characterizes the maximum error which may exist in a device from a particular speed group. Data Separator Uncertainty includes DC offset and one standard deviation total jitter, assuming normally distributed jitter. It is measured in a "dynamic" environment, emulating worst-case bit-shift of alternating "early" and "late" data bits from a disk drive, representing the true data recovery capability of the device. In the ML4025, the Data Separator Uncertainty is less than 5% of the oscillator period. (See Figure 1)



t_{OSC} = OSCILLATOR PERIOD
M_W = AVAILABLE WINDOW MARGIN
U_{DS} = DATA SEPARATOR UNCERTAINTY
$M_W = t_{OSC}/2 - U_{DS}$

Figure 1.

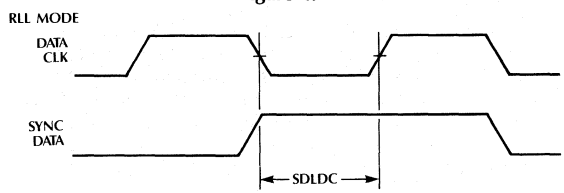


Figure 2. Data Clock Output Timing

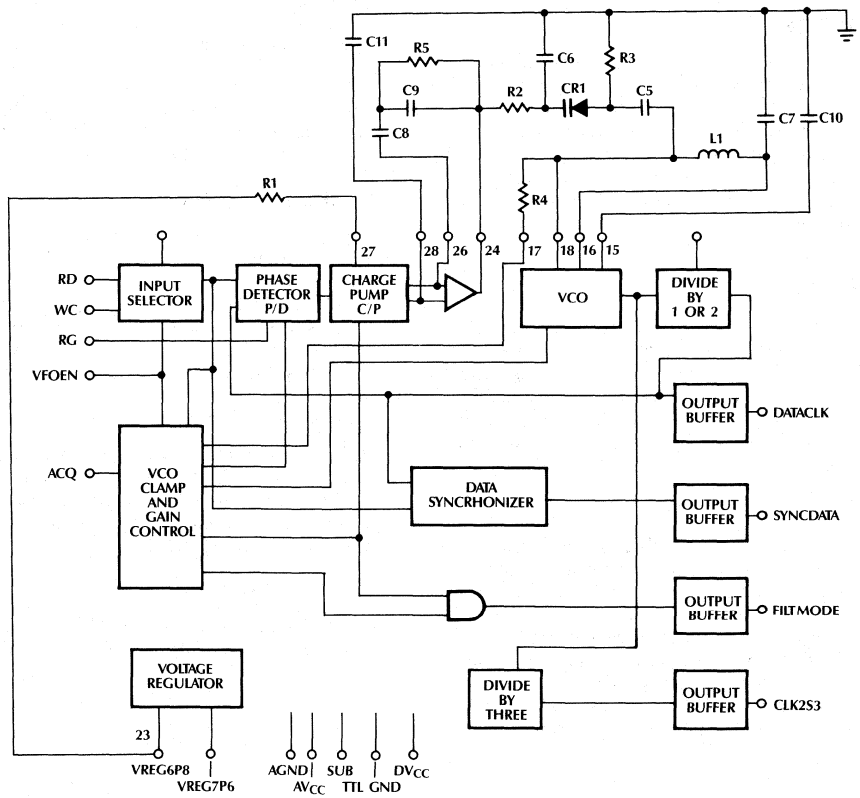


Figure 3. Typical Passive Component Connections

COMPONENT SELECTION GUIDE

COMPONENT SELECTION (See Figure 3)

I. VCO Tank Circuit

A range of VCO frequencies $f_{MAX} - f_{MIN}$ can be determined from zone frequencies, and component tolerances. From this we can solve for $C_{56} = C_5 \parallel C_6$.

$$C_{56} = \frac{C_{MIN}\, C_{MAX} \left(\left(\frac{f_{MAX}}{f_{MIN}} \right) - 1 \right)}{C_{MAX} - \left(\frac{f_{MAX}}{f_{MIN}} \right)^2 C_{MIN}}$$

Where C_{MIN} and C_{MAX} are the minimum and maximum capacitance values for the varactor diode over the range of integrator output voltages. For a MVAM109, C_{MIN} = 70pF, C_{MAX} = 500pF.

For a 50MHz clock rate ± 20%,

$$C_{56} = \frac{(70)\,(500) \left(\left(\frac{60}{40} \right)^2 - 1 \right)}{500 - \left(\frac{60}{40} \right)^2 70} = 128\text{pF}$$

R_2 can be maximized for optimum isolation of amplifier by making C_6 small.

Chosing C_6 = 150pF, C_5 = 910pF, C_{56} = 129pF, the value of L_1, can be found by:

$$L_1 = \frac{C_{56} + C_{MAX}}{4\pi^2\, f_{MIN}^2\, C_{56}\, C_{MAX}} = 0.15\mu\text{H}$$

R_2 can be chosen such that $\frac{1}{R_2\, C_6}$ places a pole near the bandwidth of the amplifier. This will help to roll off high frequency components without distorting the loop filter.

$$R_2 = \frac{1}{(5\text{MHz})\,(150\text{pF})} = 1.33\text{K, use } 1.3\text{K}$$

VCO gain can now be found by

$$K_O = \left[\frac{1}{2\pi\sqrt{LC_{EQMIN}}} - \frac{1}{2\pi\sqrt{LC_{EQMAX}}} \right] / 6.1$$

Where $C_{EQMIN} = C_5 \parallel C_6 \parallel C_{MIN}$ and

$C_{EQMAX} = C_5 \parallel C_6 \parallel C_{MAX}$

We find K_O = 3.3 MHz/V

II. LOOP FILTER

In a (2, 7) coding scheme:

N_{MAX} = 8

N_{MIN} = 3

and if $N_{PREAMBLE}$ = 3

we can select δ Preamble = 0.90, such that

$$\delta_{MIN} = 0.9 \sqrt{\frac{N_{MIN}}{N_{MAX}}}$$

$\delta_{MAX} = 0.9$ $\delta_{MIN} = 0.90 \sqrt{3/8} = 0.55$,

in this manner δ is between 0.5 and 1.0 for all data patterns. This is useful as $\delta > 1$ will tend to be oscillatory. $\delta < 0.5$ may acquire signals too slowly.

For an 8 byte preamble,

$$t = \left(\frac{1}{25\text{M}} \frac{\text{s}}{\text{bit}} \right) \left(8 \frac{\text{bits}}{\text{byte}} \right) (8 \text{ bytes})$$

$t = 2.56\ \mu\text{sec}$

One of three system constraints will likely dominate in the selection at the natural frequency of the loop ω_N.

1. At the end of an 8 byte preamble, the residual phase error should be less than 2ns. This is the specification for the ML4025 zero phase start up error. However, frequency variations may occur between the reference clock and data stream due to errors in disk rotational velocity. If we expect a 1% frequency step error

   $$\Delta\omega = (0.01)\,(25\text{M})\,(2\pi) = 1.57\ \text{Mr/s}$$

   Residual phase error is given by Gardner[1] to be

   $$\theta_e(t) = \frac{\Delta\omega}{\omega_n} \left[\frac{1}{(1-\delta^2)^{1/2}} \sin\left(1-\delta^2\right)^{1/2} \omega_n t \right] e^{-\delta\, \omega_n t}$$

   δ = 0.9, t = 2.56 μsec as shown before.

   We want $\theta_e(t) \leq$ 2ns $(2\pi/40\text{ns})$ = 0.314 rads

   We can find that if ω_n = 1.1 Mr/s that

   $$\theta e\ (2.56\ \mu\text{sec}) = 0.241\ \text{rads} = 1.54\ \text{ns}$$

2. The loop must be able to lock onto this frequency step, to ensure this the lock range should be 1.5X the step.

   Since $\Delta\omega_L = 2\delta\omega_n$,

   $$\omega_n = \frac{\Delta\omega_L}{2\delta} = \frac{(1.5)(0.01)(25\text{M})(2\pi)}{2(0.9)} = 2.6\ \text{Mr/s}$$

3. ω_n should be on the order of 10X the maximum mechanical vibration frequency of 10 KHz, therefore

   $$\omega_n \geq (10\text{K})(10)(2\pi) = 628\ \text{kr/sec}$$

   From the above we see that criterion #2 dominates, and ω_n = 2.6 Mr/sec.

   The impedance of the loop filter is

   $$R_5 \parallel \left(\frac{1}{SC_9} + \frac{1}{SC_8} \right)$$

$$\text{and } F(S) = \frac{R_5\,SC_8 + R_5\,SC_9 + 1}{R_5\,S^2\,C_8\,C_9 + SC_8}$$

if we let $C_8 >> C_9$,

$$F(S) = \frac{R_5\,SC_8 + 1}{(R_5\,SC_9 + 1)SC_8}$$

For all phase lock loops

$$\frac{\theta_O(S)}{\theta_I(S)} = b(S) = \frac{K_O\,K_D\,F(S)}{S + K_O\,K_D\,F(S)}$$

if we let $K' = K_O\,K_D$

$$\text{then } G(S) = \frac{K'\,(R_5\,SC_8 + 1)\,/C_8}{S^3\,R_5\,C_9 + S^2 + SK'\,R_5 + K'\,/C_8}$$

if $C_8 >> C_9$

$$G(S) = \frac{K'\,(R_5\,SC_8 + 1)\,/C_8}{S^2 + SK'\,R_5 + K'\,/C_8}$$

$$\text{but}^{(2)},\ G(S) = \frac{2\delta\omega_n\,S + \omega_n{}^2}{S^2 + 2\delta\omega_n\,S + \omega_n{}^2}$$

Solving:

$$\omega_n{}^2 = \frac{K'}{C_8} \rightarrow \omega_n = \left(\frac{K_O\,K_D}{C_8}\right)^{1/2}$$

$$K'\,R_5 = 2\delta\omega_n{}^2 \rightarrow \delta = \frac{K'\,R_5}{2\omega_n}$$

$$\text{but } K' = C_8\,\omega_n{}^2 \rightarrow \delta = \frac{C_8\,\omega_n\,R_5}{2}$$

$$\text{So } C_8 = \frac{K_O\,K_D}{\omega_n{}^2} \text{ and } R_5 = \frac{2\delta}{C_8\,\omega_n}$$

We know K_O = 3.3 MHz/V and ω_n = 2.6 Mr/s

In the fast acquisition mode, using R_{SET} = 4.99K (This value results in optimized internal swings), the phase comparator gain is

$$K_D = \frac{1.3\text{ mA}}{2\pi}$$

$$C_8 = \frac{(3.3\text{M})(2\pi)\left(\frac{1.3\text{ mA}}{2\pi}\right)}{(2.6\text{ Mr/s})^2} = 634\text{ pF}$$

We can use 680pF.

$$C_9 << C_8 = \frac{680}{15} = 45\text{pF, use } 47\text{pF.}$$

$$R_5 = \frac{2\delta}{C_8\,\omega_n} = \frac{2(0.9)}{(680\text{pF})\,(2.6\text{M})} = 1\text{K}$$

SELECTING R4 (CLAMP RESISTOR)

The value of R4 should be selected such that the resulting clamp release error (CRE) is zero. This ensures that the device starts up in phase with a data field, and helps the data separator recover from any frequency steps between the data and reference clock. To set the CRE to zero, the RD and OSCIN pins should be monitored. While DATACLK output is often more accessible than the OSCIN pin, it is undesirable to monitor DATACLK as charge storage effects in the TTL driver skews the first clock pulse from later pulses. The OSCIN pin can be observed while minimizing the effect on the tank circuit by placing a small (3-5pF) capacitor in series with a scope proble. The observed amplitude is reduced, but is still sufficient.

A potentiometer set initially at 100 ohms makes a good starting point in determining R4, as long as the leads to the pot are kept short. As in figure 4, the 4th RD pulse following a VFOEN and RG rising edge can be seen to start the oscillator. The delay time t1 can be measured between a RD rising edge, and the OSCIN rising edge. (This is true whether the VCO is 1x or 2x the clock rate). The delay time t2 can be measured in the same fashion for a later RD pulse where all phase corrections have been made. To ensure that all phase corrections have been made, observe the INTOUT pin to make sure its value is no longer changing. The difference between t1 and t2 is the clamp release error. To make this error zero, simply adjust the pot downward in value until t1 = t2. A fixed resistor near this value can now be substituted. This value of R4 will keep the start up phase error below 2ns for all ML4025 devices over temperature and supply variations.

References:

(1) Phaselock Techniques 2nd Edition, Floyd M. Gardner, Wiley-Interscience, '79 page 48

(2) ibid page 11

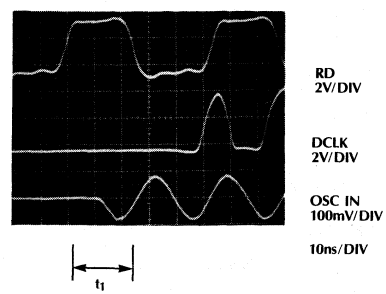


Figure 4.

ORDERING INFORMATION

PART NUMBER	PACKAGE
ML4025CP	24-Leaded Molded DIP (Prototypes only)
ML4025CQ	28-Lead PCC

ML4041, ML4042

Read Data Processor

GENERAL DESCRIPTION

The ML4041, ML4042 is a monolithic bipolar integrated circuit used in disk drive systems to detect amplitude peaks generated by the recording heads during a Read operation. Connected to the read/write amplifier output, it detects valid data and provides a TTL output to the data separator. Containing both analog and digital circuitry, it supports the reading of MFM and RLL encoded data at rates up to 24 megabits/second.

Operating modes Read, Write, and Hold are selectable with input logic signals. Read mode is used for pulse peak detection during a Read operation. Write mode disables the device's output during a Write operation, while Hold mode holds the AGC gain constant during recovery of embedded servo information.

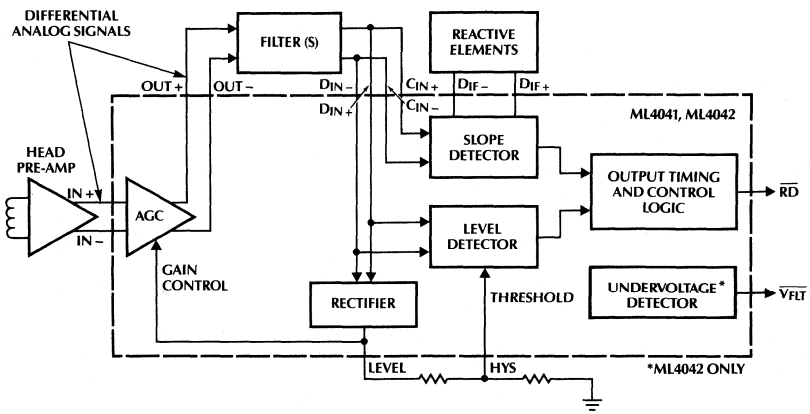
By using both level and slope detection, accurate pulse validation and peak time detection is achieved. The ML4041, ML4042 characteristics can be modified to fit particular needs through external component selection. The ML4041, ML4042 has a swift Write to Read recovery time of 2μs (10μs max) allowing for better format efficiency with faster access times. Pulse pairing of 1ns max reduces data decoding errors by allowing tighter specs for the clock recovery circuit.

FEATURES

- Fully compatible with industry standard read data processor
- Write to Read recovery time — 2μs typical, 10μs max
- Pulse pairing — 1ns max
- Data rates up to 24 megabits/second
- Supports MFM and RLL encoded read data
- 30MHz wide-bandwidth AGC amplifier
- Fast AGC region for fast transient recover
- Slow AGC region for minimum zero crossing distortion
- +5V and +12V undervoltage fault detection (ML4042 only)
- Write to read transient suppression
- Hold pin supports embedded servo decoding

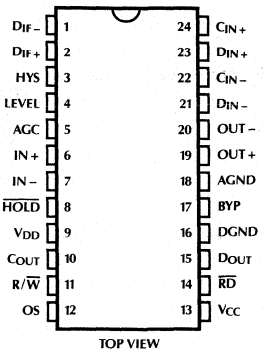
The ML4042 is identical to the ML4041 but in addition it includes a +5V and +12V undervoltage detector. The ML4041 is available in a 24-pin PDIP, 24-pin SOIC, or a 28-pin PCC, while the ML4042 is available in a 28-pin PDIP, 28-pin SOIC, or a 28-pin PCC.

SIMPLIFIED BLOCK DIAGRAM

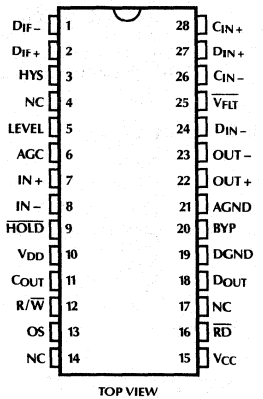


PIN CONNECTIONS

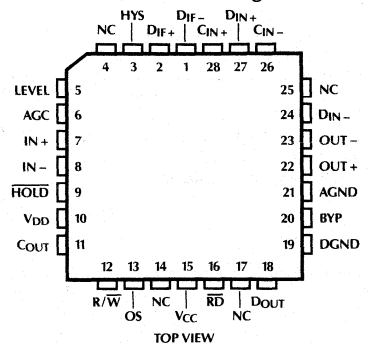
ML4041
24-Pin DIP and SOIC Package



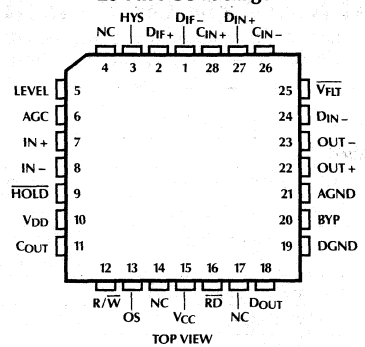
ML4042
28-Pin DIP and SOIC Package



ML4041
28-Pin PCC Package



ML4042
28-Pin PCC Package



PIN DESCRIPTION

NAME	FUNCTION
V_{CC}	+5V
V_{DD}	+12V
AGND	Analog Ground.
DGND	Digital Ground.
R/$\overline{W}$	TTL compatible Read/Write Control pin.
IN+, IN–	Analog Signal Input pins
OUT+, OUT–	AGC Amplifier Output pins
BYP	The AGC timing capacitor C_{AGC} is tied between this pin and AGND.
$\overline{HOLD}$	TTL compatible pin that holds the AGC gain when pulled low.
AGC	Reference input voltage level for the AGC circuit.
D_{IN+}, D_{IN-}	Analog input to the hysteresis comparator.

NAME	FUNCTION
HYS	Input for setting hysteresis level of the hysteresis comparator.
LEVEL	Provides rectified signal level for input to the hysteresis comparator.
D_{OUT}	Buffered test point for monitoring D input of the flip-flop.
C_{IN+}, C_{IN-}	Analog input to the differentiator.
D_{IF+}, D_{IF-}	External differentiating network connection pins.
C_{OUT}	Buffered test point for monitoring the clock input to the flip-flop.
OS	Connection for read output pulse width setting capacitor C_{OS}.
$\overline{RD}$	TTL compatible read output.
$\overline{V_{FLT}}$	Undervoltage detector output, active low; ML4042 only.

TABLE 1 MODE SELECT

R/$\overline{W}$	$\overline{HOLD}$	MODE	DESCRIPTION
1	1	READ	AGC amp section active, Digital section active.
1	0	HOLD	AGC gain constant, Digital section active.
0	X	WRITE	AGC gain maximum, Digital section inactive, Input common mode resistance reduced.

0 = Logic level low
1 = Logic level high
X = Don't care

ABSOLUTE MAXIMUM RATINGS

(Note 1)

Power Supply Voltage Range
- V_{CC} ..... −0.3 to 6 V_{DC}
- V_{DD} ..... −0.3 to 14 V_{DC}

Terminal Voltage Range
- R/W, IN+, IN−, HOLD ..... −0.3 V to V_{CC} +0.3 V
- RD ..... −0.3 V to V_{CC} +0.3 V or +12 mA
- All others ..... −0.3 V to V_{DD} +0.3 V

Storage Temperature Range ..... −65°C to +150°C
Junction Temperature (T_J) ..... +135°C
Lead Temperature (Soldering, 10 sec) ..... 260°C

OPERATING CONDITIONS

Supply Voltage
- V_{CC} ..... 5 V ± 10%
- V_{DD} ..... 12 V ± 10%

$V_{(CIN+}-C_{IN-)}$, $V_{(DIN+}-D_{IN-)}$ ..... $1V_{P-P}$
V_{HYS} ..... 1.0 V
C_{OS} ..... 50 to 200 pF

Typical Component Values (Refer to Typical Applications)
- C_{IN} ..... 0.001 µF
- C_S ..... 0.01 µF
- C_{OUT} ..... 0.0047 µF
- R_{OUT} ..... 400 Ω
- C_{AGC1} ..... 220 pF
- C_{AGC2} ..... 2000 pF
- R_{AGC} ..... 2.21 kΩ
- C_{LEVEL} ..... 150 pF
- R_{LEVEL1} ..... 1.54 kΩ
- R_{LEVEL2} ..... 6.49 kΩ
- C_{OS} ..... 50 pF

ELECTRICAL CHARACTERISTICS

The following specifications apply over the recommended operating conditions of V_{CC} = 5 V ± 10%, V_{DD} = 12 V ± 10%, 0°C < T_A < 70°C and external components as specified under operating conditions unless otherwise specified. (See Note 2.)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP NOTE 4	MAX	UNITS
DC Characteristics						
I_{CC}	V_{CC} Supply Current	Outputs unloaded			14	mA
I_{DD}	V_{DD} Supply Current	Outputs unloaded			70	mA
P_D	Power Dissipation	Outputs unloaded, T_A = 70°C			930	mW
Digital Inputs Characteristics ($\overline{HOLD}$, R/$\overline{W}$)						
V_{IH}	High Voltage		2			V
V_{IL}	Low Voltage		−0.3		0.8	V
I_{IH}	High Current	V_{IH} = 2.4 V			100	µA
I_{IL}	Low Current	V_{IL} = 0.4 V	−0.4			mA
Digital Outputs Characteristics (C_{OUT}, $\overline{RD}$)						
V_{OL}	Output Low Voltage	I_{OL} = 4 mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} = 400 µA	2.4			V
WRITE AND HOLD MODE CHARACTERISTICS						
Mode Control						
t_{RW}	Read to Write Transition Time				1	µs
t_{WR}	Write to Read Transition Time	AGC settling not included, time to high input resistance	1.2		3	µs
t_{RH}	Read to Hold Transition Time				1	µs
Write Mode						
Z_{IC}	Common Mode Input Impedance (both sides)	R/$\overline{W}$ pin = low		250		Ω

ELECTRICAL CHARACTERISTICS (Continued)

The following specifications apply over the recommended operating conditions of $V_{CC}=5V\pm10\%$, $V_{DD}=12V\pm10\%$, $0°C\leq T_A\leq 70°C$, IN+ and IN− AC coupled, OUT+ and OUT− differentially loaded with >600Ω and each side loaded with <10pF to GND, $C_{BYP}=2000pF$, OUT+ and OUT− AC coupled to D_{IN+} and D_{IN-} respectively, $V_{AGC}=2.2V$ unless otherwise specified. (See Note 2.)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP NOTE 4	MAX	UNITS
READ MODE CHARACTERISICS						
AGC Amplifier						
R_{ID}	Differential Input Resistance	$V_{(IN+-IN-)}=100mV_{P-P}$ @ 2.5MHz		5		kΩ
C_{ID}	Differential Input Capacitance	$V_{(IN+-IN-)}=100mV_{P-P}$ @ 2.5MHz			10	pF
Z_{IC}	Common Mode Input Impedance (both sides)	R/$\overline{W}$ pin high		1.8		kΩ
		R/$\overline{W}$ pin low		0.25		kΩ
$A_{V_{MAX}}$	Maximum Gain	$V_{BYP}=2.6V$	83			V/V
$A_{V_{MIN}}$	Minimum Gain	V_{BYP} = 6V	2		4	V/V
e_N	Input Noise Voltage	Gain set to maximum			30	nV/$\sqrt{Hz}$
BW	Bandwidth	Gain set to maximum, −3dB point	30			MHz
ΔV_{OS}	Maximum Gain and Minimum Gain AGC Amp Output Offset Voltage Difference	$V_{BYP}=2.6V$ for maximum gain $V_{BYP}=5.0V$ for minimum gain			700	mV
$V_{BYP_{MAX}}$	Max Voltage at BYP Pin at Minimum Gain	$V_{(D_{IN+}-D_{IN-})}=1.6V$, $V_{AGC}=3.0V$		6.0	6.7	V
V_{OP}	Maximum Output Voltage Swing	Set by V_{AGC}	3			V_{P-P}
I_{OD}	OUT+ to OUT− Pin Current	No DC path to GND, See Note 3	±3.2			mA
R_O	Output Resistance			18	32	Ω
C_O	Output Capacitance			12		pF
V_{IP} V_{AGC}	$(D_{IN+}-D_{IN-})$ Input Voltage Swing VS AGC Input Level	$30mV_{P-P}\leq V_{(IN+-IN-)}\leq 550mV_{P-P}$, $0.5V_{P-P}\leq V_{(D_{IN+}-D_{IN-})}\leq 1.5V_{P-P}$	0.37	0.48	0.56	V_{P-P}/V
V_{IP}	$(D_{IN+}-D_{IN-})$ Input Voltage Swing Variation	$30mV_{P-P}<V_{(IN+-IN-)}<550mV_{P-P}$, AGC Fixed, over supply and temp.			+8	%
t_D	Gain Decay Time	See Figure 1a; $V_{IN}=300mV_{P-P}$ then $>150mV_{P-P}$ at 2.5MHz, V_{OUT} to 90% of final value.		50		μs
t_A	Gain Attack Time	See Figure 1b; from Write to Read transition to V_{OUT} at 110% of final value, $V_{IN}=400mV_{P-P}$ @ 2.5MHz		4		μs
I_{AGCfc}	Fast AGC Capacitor Charge Current	$V_{(D_{IN+}-D_{IN-})}=1.6V$, $V_{AGC}=3.0V$	1.3	1.5	2.0	mA
I_{AGCsc}	Slow AGC Capacitor Charge Current	$V_{(D_{IN+}-D_{IN-})}=1.6V$, Vary V_{AGC} until slow discharge begins	0.14	0.17	0.22	mA
	Fast to Slow Attack Switchover Point	$\frac{V_{(D_{IN+}-D_{IN-})}}{V_{(D_{IN+}-D_{IN-})}\text{ Final}}$		1.25		-
I_{AGCD}	AGC Capacitor Discharge Current	$V_{(D_{IN+}-D_{IN-})}=0.0V$ Read Mode		4.5		μA
		Hold Mode	−0.2		+0.2	μA
CMRR	CMRR (Input Referred)	$V_{IN+}=V_{IN-}=100mV_{P-P}$ @ 5MHz, gain at maximum	40			dB
PSRR	PSRR (Input Referred)	V_{CC} or $V_{DD}=100mV_{P-P}$ @ 5MHz, gain at maximum	30			dB
TREC	Write to Read Recovery Time. Includes AGC Settling	$V_{(IN+-IN-)}=100mV_{P-P}$ @ 2.5MHz	1.2	2	10	μs

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ELECTRICAL CHARACTERISTICS (Continued)

The following specifications apply over the recommended operating conditions of $V_{CC} = 5V \pm 10\%$, $V_{DD} = 12V \pm 10\%$, $0°C \leq T_A \leq 70°C$, IN+ and IN− AC coupled, OUT+ and OUT− differentially loaded with >600Ω and each side loaded with <10pF to GND, $C_{BYP} = 2000pF$, OUT+ and OUT− AC coupled to D_{IN+} and D_{IN-} respectively, $V_{AGC} = 2.2V$ unless otherwise specified. (See Note 2.)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP NOTE 4	MAX	UNITS
READ MODE CHARACTERISICS (Continued)						
Hysteresis Comparator						
V_{IP}	Input Signal Range				1.5	V_{P-P}
R_{ID}	Differential Input Resistance	$V_{(D_{IN+}-D_{IN-})} = 100mV_{P-P}$ @ 2.5MHz	5		15	kΩ
C_{ID}	Differential Input Capacitance	$V_{(D_{IN+}-D_{IN-})} = 100mV_{P-P}$ @ 2.5MHz			6.0	pF
Z_{IC}	Common Mode Input Impedance	(both sides)		2.0		kΩ
V_{IO}	Comparator Offset Voltage	HYS pin at −0.5V, ≤1.5kΩ across D_{IN+}, D_{IN-}		5		mV
V_{HYSP} V_{HYS}	Peak Hysteresis Voltage vs HYS pin voltage (input referred)	$1V < V_{HYS} < 3V$	0.16	0.21	0.25	V/V
I_I	HYS Pin Input Current	$1V < V_{HYS} < 3V$	0		−20	μA
I_O	LEVEL Pin Max Output Current		3			mA
R_O	LEVEL Pin Output Resistance	$I_{LEVEL} = 0.5mA$		180		Ω
V_{OL}	D_{OUT} Pin Output Low Voltage	$T_A = 70°C$	$V_{DD}-4.0$		$V_{DD}-2.5$	V
V_{OH}	D_{OUT} Pin Output High Voltage	$T_A = 70°C$	$V_{DD}-2.2$		$V_{DD}-1.5$	V
V_{LEVEL} $V_{D_{IN}}$	Level Pin Output Voltage vs $V_{(D_{IN+}-D_{IN-})}$	$0.6 < \lvert V_{(D_{IN+}-D_{IN-})} \rvert < 1.3V_{P-P}$ 10kΩ from level pin to GND	1.5		2.5	V/V_{P-P}
Active Differentiator						
V_{IP}	Input Signal Range				1.5	V_{P-P}
R_{ID}	Differential Input Resistance	$V_{(C_{IN+}-C_{IN-})} = 100mV_{P-P}$ @ 2.5MHz	5		11	kΩ
C_{ID}	Differential Input Capacitance	$V_{(C_{IN+}-C_{IN-})} = 100mV_{P-P}$ @ 2.5MHz			6	pF
Z_{IC}	Common Mode Input Impedance	(both sides)		2.0		kΩ
I_{OD}	D_{IF+} to D_{IF-} Pin Current	Differentiator Imped must be set so as not to clip signal at this current level	±1.3			mA
V_{IO}	Comparator Offset Voltage	D_{IF+}, D_{IF-} AC Coupled		5		mV
V_{OL}	C_{OUT} Pin Output Low Voltage	$0 \leq I_{OH} \leq 0.5mA$		$V_{DD}-3$		V
V_{PO}	C_{OUT} Pin Output Pulse Voltage	$0 \leq I_{OH} \leq 0.5mA$		0.4		V
PW_0	C_{OUT} Pin Output Pulse Width	$0 \leq I_{OH} \leq 0.5mA$		30		ns
A_V	Voltage Gain From $C_{IN\pm}$ to $D_{IF\pm}$	$R_{(D_{IF+} \text{ to } D_{IF-})} = 2k\Omega$	1.7		2.2	V/V
Undervoltage Detector (ML4042 Only)						
$V_{CC\,TH+}$	V_{CC} Fault Threshold+	$\overline{V_{FLT}}$ transition from low to high	3.8	4.2	4.5	V
$V_{CC\,TH-}$	V_{CC} Fault Threshold−	$\overline{V_{FLT}}$ transition from high to low	3.8	4.1	4.5	V
$V_{DD\,TH+}$	V_{DD} Fault Threshold+	$\overline{V_{FLT}}$ transition from low to high	9.6	10.2	10.8	V
$V_{DD\,TH-}$	V_{DD} Fault Threshold−	$\overline{V_{FLT}}$ transition from high to low	9.6	10.0	10.8	V
V_{OL}	Output Low Voltage ($\overline{V_{FLT}}$)	$I_{OL} = 1.6mA$			0.4	V
V_{OH}	Output High Voltage ($\overline{V_{FLT}}$)	$I_{OH} = -400\mu A$	2.7			V

ELECTRICAL CHARACTERISTICS (Continued)

The following specifications apply over the recommended operating conditions of $V_{CC} = 5V \pm 10\%$, $V_{DD} = 12V \pm 10\%$, $0°C \leq T_A \leq 70°C$, $V_{(C_{IN+}-C_{IN-})} = V_{(D_{IN+}-D_{IN-})} = 1.0V_{P-P}$ AC coupled sine wave at 2.5MHz, $R_{D_{IF}} = 100\Omega$, $C_{D_{IF}} = 65pF$, $V_{HYS} = 1.8V$, $C_{OS} = 60pF$, 4kΩ to V_{CC} and 10pF to GND on pin $\overline{RD}$ unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP NOTE 4	MAX	UNITS
Output Data Characteristics (Refer to Figure 2)						
t_{D1}	D-Flip-Flop Set Up Time	Min delay from $V_{(D_{IN+}-D_{IN-})}$ exceeding threshold to $V_{(D_{IF+}-D_{IF-})}$ reaching a peak	0			ns
t_{D3}	Propagation Delay				110	ns
t_{D5}	Output Data Pulse Width Variation	(See Note 5) C_{OS} = 60pF, T_A = 25°C	40	50	65	ns
t_{D3}-t_{D4}	Logic Skew (Pulse Pairing)				1	ns
t_R	Output Rise Time	$V_{OH} = 2.4V$			18	ns
t_F	Output Fall Time	$V_{OL} = 0.4V$			14	ns

Note 1: Absolute maximum ratings are limits beyond which the life of the integrated circuit may be impaired. All voltages unless otherwise specified are measured with respect to ground.

Note 2: Limits are guaranteed by 100% testing, sampling, or correlation with worst-case test conditions.

Note 3: AGC amplifier output current may be increased as in Figure 4.

Note 4: Typicals are parametric norm at 25°C.

Note 5: $t_{D5} = 830\ (C_{OS})$, $50pF < C_{OS} < 150pF$

FUNCTIONAL DESCRIPTION

Operating Modes

The ML4041, ML4042 has three definitive operation modes which are: Read mode, Write mode and Hold mode. These modes are defined by input pins $\overline{HOLD}$ and R/$\overline{W}$ as shown in Table 1. Read mode, the mode used normally for pulse detection, is assumed in the following sections unless otherwise noted.

AGC Amplifier Section

The purpose of the AGC amplifier is to provide a constant read signal level for both the level and slope detectors. Full differential processing of the read signal is used to minimize noise and distortion in the analog signal. A wide gain range is required due to large signal variation when moving the recording head from an inside to outside data track or variations in media.

The differential output voltage level V_{OUT} from the AGC amp is determined by voltage V_{AGC} present at pin AGC. V_{OUT} is full wave rectified and compared against V_{AGC} to create charge/discharge current for capacitor C_{BYP} connected at pin BYP. Voltage V_{BYP} across C_{BYP} controls the gain in the AGC amplifier.

Two distinct values of I_{BYP} are possible which determine a fast and slow AGC gain response attack rate. When V_{OUT} is more than 125% of the set level a high value of I_{BYP} is sourced which provides a fast AGC attack rate. When V_{OUT} is within 100% to 125% of the set level a reduced value of I_{BYP} is sourced which provides a slower attack rate. The fast-slow gain response attack rates provides for an initial quick system response and then minimum zero crossing distortion of the analog signal once the gain is within working range. V_{AGC} should be set so that the differential input voltage $V_{D_{IN}}$ into the level comparator is $1V_{P-P}$ at nominal Read signal conditions. The AGC amp section gain is given by:

$$\frac{A_{V2}}{A_{V1}} = \exp \frac{V_{BYP2} - V_{BYP1}}{5.8 \times V_T}$$

Where: A_{V1}, A_{V2} are initial and final amplifier gain values corresponding to initial and final V_{BYP} values.

$V_T = (KT)/Q = 26mV$ at room temperature.

The AGC amp's differential inputs must be AC coupled to the read amplifier (ML117, ML501, etc.) differential outputs. Similarly, AC coupling must be used at the AGC amp outputs.

AGC Amp During Write Mode—When the ML4041, ML4042 is put into write mode, the AGC amp's input impedance is lowered to allow a faster dampening of the Write to Read transient from the head pre-amp. The AGC gain is also set to maximum gain so that fast AGC attack will occur when changing back to the Read mode. Internal device timing is controlled so that settling occurs prior to Read mode activation. Minimal value input coupling capacitors should be chosen to reduce settling time, however, bandwidth requirements also need to be considered.

AGC Amp During Hold Mode — During the Hold mode, the charge/discharge current driving pin BYP is internally disconnected. AGC compensation capacitor C_{AGC} will then hold the present gain setting. The amplitude of V_{OUT} will therefore not affect the AGC gain and gain will remain constant.

Hold mode is used so that AGC gain will not be adjusted when embedded servo information is read. This prevents loosing the pulse peak amplitude information needed during position decoding, or creating additional gain settling time when again reading data. Embedded servo pulses are normally taken at outputs D_{IF-} and D_{IF+}, as shown in the typical application.

External Filter Network

Filtering for the level and slope detectors can be performed with a single filter or two separate filters. If separate filters are used, care must be used to insure that time delays are matched. A multi-pole Bessell filter is recommended due to the group delay and linear phase characteristics.

Level Detector

The full wave rectified V_{OUT} is buffered and available at pin LEVEL. The level detector uses a hysteresis comparator to compare the processed read signal amplitude against a reference voltage derived from voltage V_{LEVEL} output from pin LEVEL. Using V_{LEVEL} provides a feed-forward function that allows valid level detection to be performed prior to AGC amp gain settling. The level detector hysteresis value is set in a way that will only allow relatively large read pulse peaks (negative or positive) to be detected.

Slope Detector

The slope detector uses an external reactive component network to produce a voltage signal proportional to the differential of the read signal. By using a hysteresis comparator to detect zero slope of the read signal, the time occurrence of positive or negative read pulse peak values can be determined.

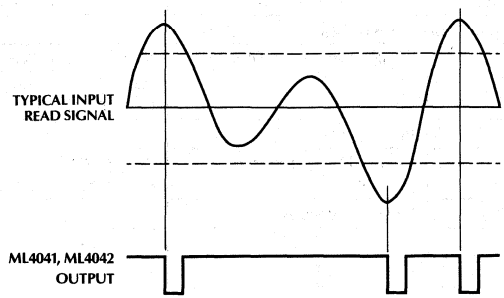
An external reactive network, shown in the Typical Application, is used between the D_{IF+} and D_{IF-} pins to provide the differential function given by:

$$A_V = \frac{-2000Cs}{LCs^2 + (R + 92)\,Cs + 1}$$

Where: C = External capacitor (20 pF to 150 pF)
L = External inductor
R = External resistor
$s = j\omega = j2\pi f$

Output Logic

The output logic provides a negative TTL pulse at pin $\overline{RD}$ which begins at the peak of a valid read pulse, as shown below.

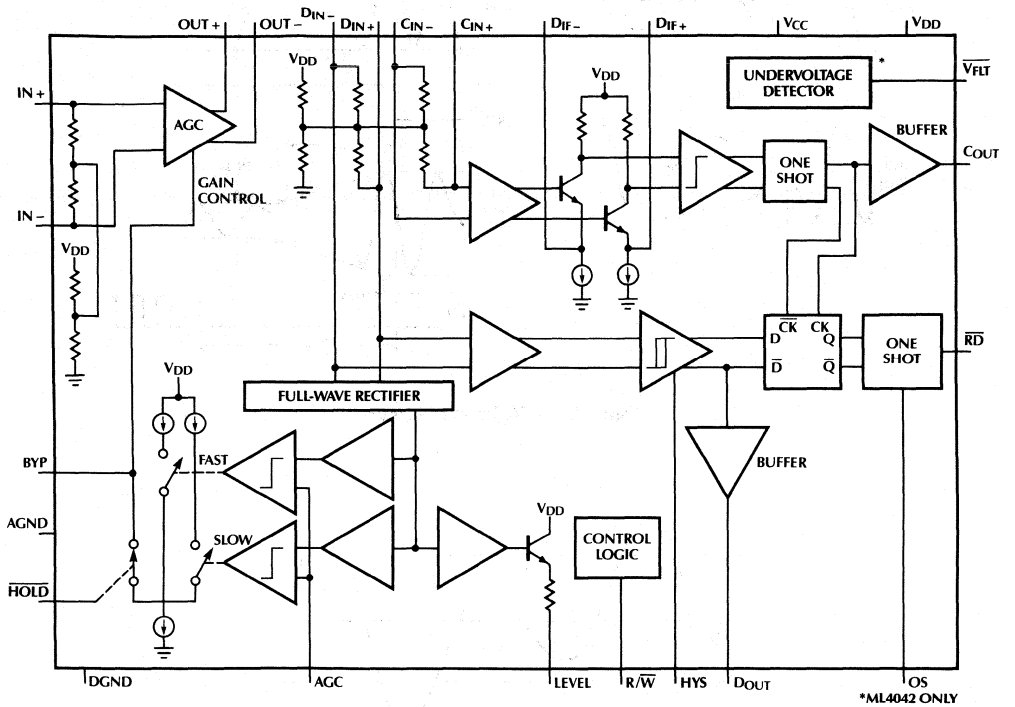


Pin R/$\overline{W}$ must be high for the output logic to be active. The key element in the output logic is the D flip-flop. The flip-flop is clocked by the slope detector at the time of a zero crossing, which loads data from level detector. The flip-flop inputs only change state when the level detector detects a peak amplitude of a polarity opposite to the previous valid peak. Thus, through the output logic the slope detector determines output timing and the level detector determines pulse validity.

Layout Considerations

As with any high gain, wide bandwidth analog circuitry, care needs to be exercised in PC layout. Power supply and ground lines should be bypassed and well isolated from other circuitry. A ground plane is recommended, as is keeping analog lines short and well balanced to prevent interaction with nearby circuitry in the disk drive.

BLOCK DIAGRAM



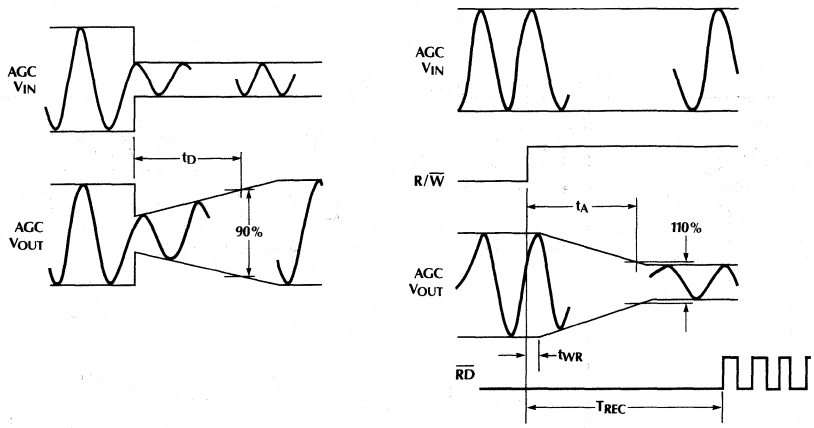


Figure 1. AGC Timing Diagram

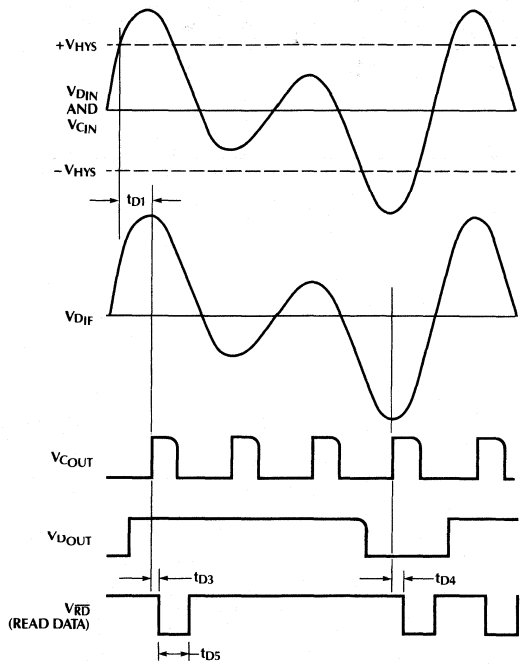


Figure 2. Output Logic Timing Diagram

TYPICAL APPLICATIONS

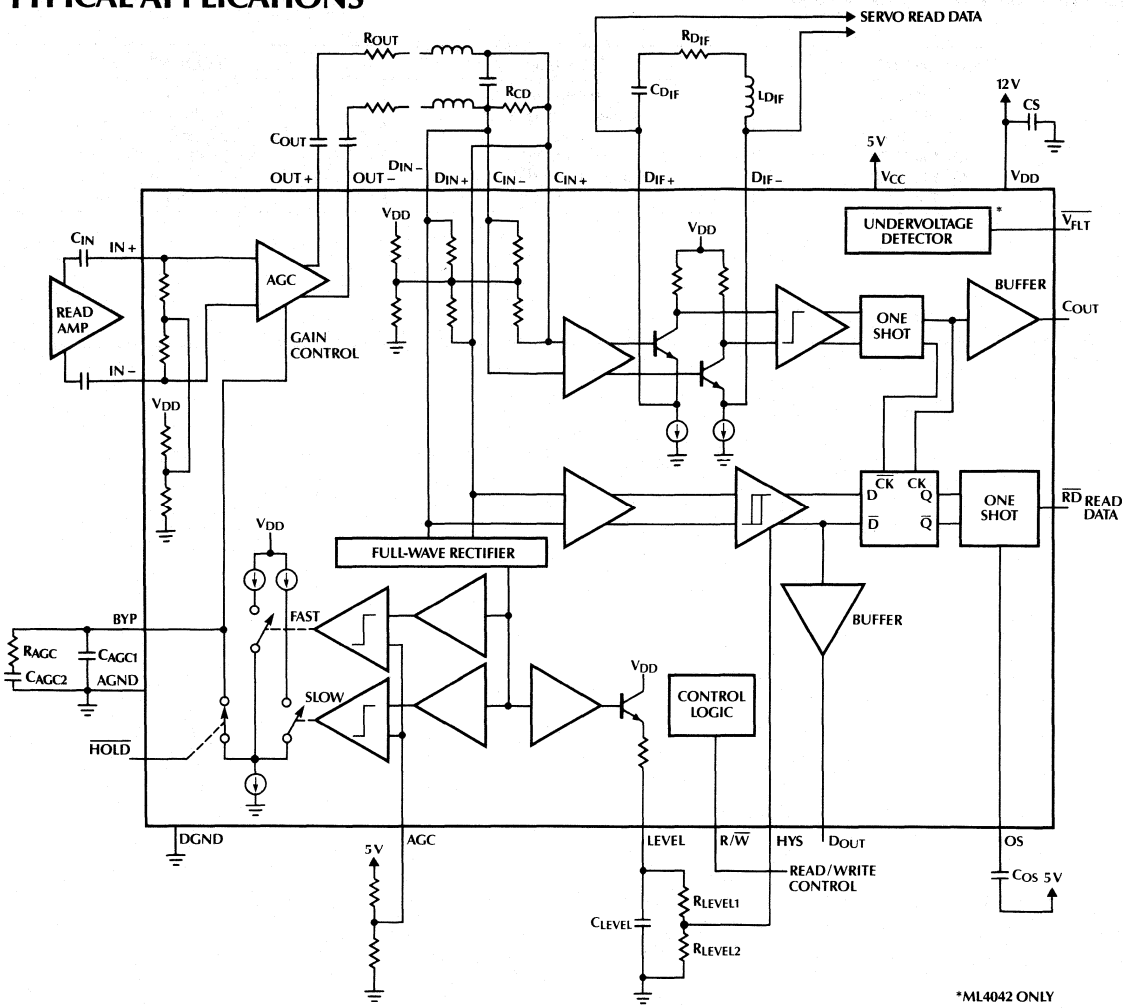


Figure 3. Typical Application Diagram

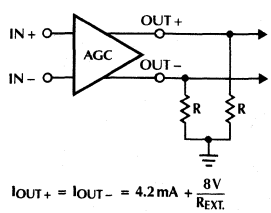


Figure 4. Modification of AGC Amplifier Output to Drive Low Impedance Filters

ORDERING INFORMATION

PART NUMBER	PACKAGE	PIN COUNT
ML4041CP	Molded DIP	24 PINS
ML4041CQ	Molded Leaded PCC	28 PINS
ML4041CS	SOIC	24 PINS
ML4042CP	Molded DIP	28 PINS
ML4042CQ	Molded Leaded PCC	28 PINS
ML4042CS	SOIC	28 PINS

Servo Demodulator

GENERAL DESCRIPTION

The ML4401 provides all of the analog circuitry necessary for the demodulation of di-bit servo signal information in Winchester disk drives. It interfaces to the servo head preamp and provides quadrature position signal outputs for the servo controller circuitry.

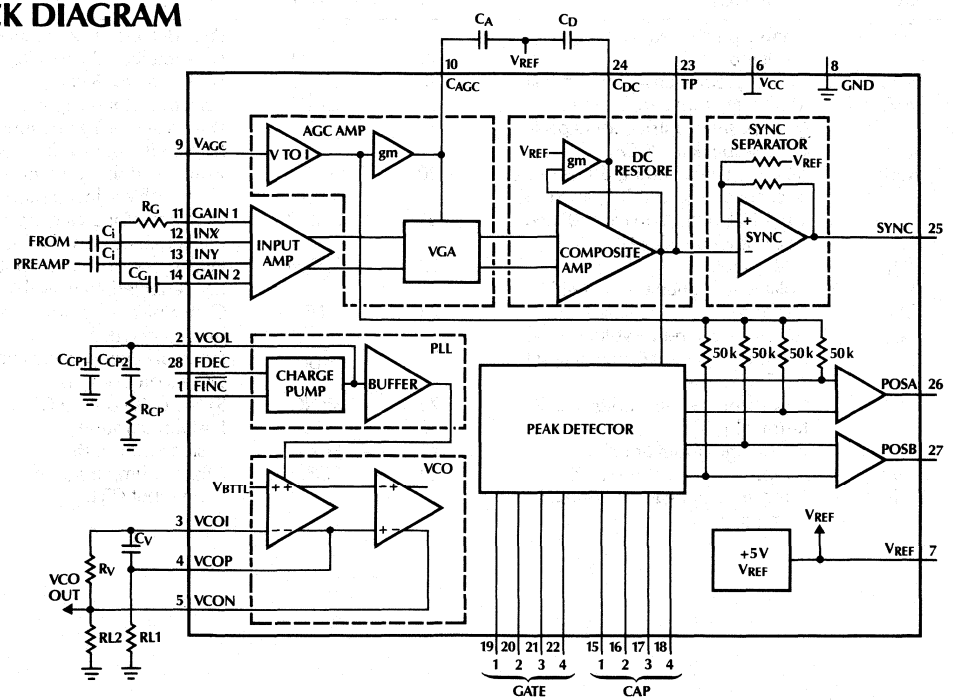
The ML4401 includes a high-performance 592-type input amplifier and differential AGC circuit. External logic is designed to meet the needs of the particular servo system utilizing the VCO and Charge Pump to create a PLL time base for Peak Detector gating. The SYNC output provides servo channel timing information for the logic.

The ML4401 when combined with the ML4402, ML4406/07/08 Servo Driver, the ML4403, ML4413 Servo Controller and the ML4404 Trajectory Generator, provides a flexible closed-loop servo control system.

FEATURES

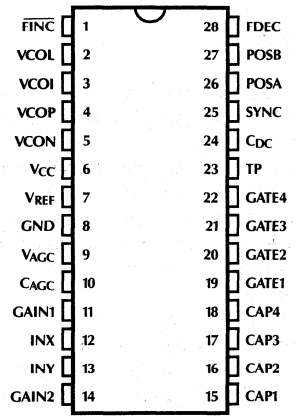
- Combines all analog di-bit demodulation circuitry
- Logic track-type switching can be used to minimize demodulator offset
- Exponential AGC characteristics makes AGC settling independent of input step size
- External loop compensation of analog blocks
- External digital circuitry allows flexible pattern format
- On-chip band gap voltage reference eliminates external referencing
- Operates from 12V power supply
- Compatible with Micro Linear's ML4403, ML4413 Servo Controller, ML4402, ML4406/07/08 Servo Driver and ML4404 Trajectory Generator

BLOCK DIAGRAM



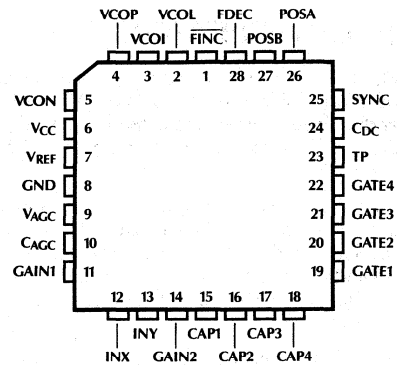
PIN CONNECTIONS

ML4401 28-Pin DIP
(Prototypes Only)



TOP VIEW

ML4401 28-Pin PCC



TOP VIEW

PIN DESCRIPTION

PIN #	NAME	FUNCTION
1	$\overline{\text{FINC}}$	Charge pump frequency increment input (TTL).
2	VCOL	PLL loop compensation terminal.
3	VCOI	VCO high impedance input.
4	VCOP	VCO positive output, for capacitive feedback to VCOI.
5	VCON	VCO negative output, drives resistance feedback to VCOI, also provides ECL output on ML4401 and TTL output on ML4411.
6	V_{CC}	+12V supply.
7	V_{REF}	Voltage reference output (+5V).
8	GND	Ground.
9	V_{AGC}	AGC gain reference voltage input.
10	C_{AGC}	External capacitor terminal to set AGC response.
11	GAIN1	Input amplifier gain adjusting RC terminal 1.
12	INX	X input into input amplifier.
13	INY	Y input into input amplifier.
14	GAIN2	Input amplifier gain adjusting RC terminal 2.
15	CAP1	Peak detector 1 capacitor terminal.
16	CAP2	Peak detector 2 capacitor terminal.
17	CAP3	Peak detector 3 capacitor terminal.
18	CAP4	Peak detector 4 capacitor terminal.
19	GATE1	Peak detector 1 gate input (TTL) high enabled, low disabled.
20	GATE2	Peak detector 2 gate input (TTL) high enabled, low disabled.
21	GATE3	Peak detector 3 gate input (TTL) high enabled, low disabled.
22	GATE4	Peak detector 4 gate input (TTL) high enabled, low disabled.
23	TP	Composite test point, normally left unconnected.
24	C_{DC}	External capacitor terminal to set DC restore response.
25	SYNC	SYNC pulse output (TTL).
26	POSA	Position output A.
27	POSB	Position output B.
28	FDEC	Charge pump frequency decrement input (TTL).

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

Power Supply Voltage, V_{CC} 14V
Input Voltages:
GAIN1, GAIN2 ..... −0.3 to 8V
C_{AGC} ..... −0.3 to 7.0V
V_{AGC} ..... −0.3 to 5.3V
CAP1, CAP2, CAP3, CAP4 ..... −0.3 to 10V
GATE1, GATE2, GATE3, GATE4, VCOP ..... −0.3 to 7.5V
INX, INY, VCON, VCOI, $\overline{FINC}$, FDEC, C_{DC} ..... −0.3 to V_{CC} +0.3V
Θ_{JA} for 28-Pin Plastic DIP ..... ≈60°C/Watt
Θ_{JA} for 28-Pin PLCC ..... 60°C/Watt
Storage Temperature Range ..... −65°C to +150°C
Junction Temperature (T_{JMAX}) ..... 150°C
Lead Temperature (Soldering, 10 sec) ..... 260°C

OPERATING CONDITIONS

Temperature Range ..... 0°C to 70°C
Supply Voltage (V_{CC}) ..... 12V_{DC} ± 10%
Input Coupling Capacitance (Ci) 0.01μF
Input Amp Gain Capacitance (C_G) 0.047μF
Input Amp Gain Resistance (R_G) 1kΩ
AGC Response Compensation Capacitance (C_A) 0.082μF
Composite DC Restore Capacitance (C_D) 0.01μF
PLL Compensation Components:
C_{CP1} 0.1μF
C_{CP2} 1μF
R_{CP} 910Ω
PLL Gain Components:
R_V 1000Ω
RL1, RL2 ..... 1000Ω
Peak Detector Capacitance (CAP1 thru CAP4) 270pF
SYNC Output Pull-Up Resistor (to 5V) 1000Ω
On track Base-to-Peak Voltage at pin TP 1.75V
V_{GA} Gain Control Voltage (at pin C_{AGC}) 0.65V

ELECTRICAL CHARACTERISTICS

The following specifications apply over the recommended operating conditions of T_A = 0 to 70°C, V_{CC} = 10.8 to 13.2V, V_{VAGC} = 5.0V, and external components as recommended above, unless otherwise specified (See Note 1.)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP NOTE 2	MAX	UNITS
Power Supply						
I_{CC}	Supply Current	V_{CC} = 12V		81	110	mA
TTL Inputs $\overline{FINC}$, FDEC, GATE1, GATE2, GATE3, GATE4						
V_{IH}	High Level Input Voltage		2.0			V
V_{IL}	Low Level Input Voltage				0.8	V
I_{IH}	High Level Input Current	V_{IH} = 2.4V	−1		30	μA
I_{IL}	Low Level Input Current	V_{IL} = 0.4V	−20		1	μA
SYNC Output (TTL Open Collector) See Note 3						
V_{OL}	Low Level Output Voltage	I_{OL} = 1.6mA	0	0.3	0.5	V
V_{THR}	Positive going input threshold			V_{REF} +0.9		V
V_{THF}	Negative going input threshold			V_{REF}		V
t_{PD} ±	Propagation Delay Rising, Falling	RL = 2k, C_L = 15pF		50		ns
VCOP Output ML4401 (T_A = 25°C)						
V_{OH}	High Level Output Voltage	RL = 1kΩ	4.0	4.3	4.6	V
V_{OL}	Low Level Output Voltage	RL = 1kΩ	2.9	3.2	3.5	V
VCOP Output ML4411						
V_{OH}	High Level Output Voltage	I_{OH} = 50μA	2.4			V
V_{OL}	Low Level Output Voltage	I_{OL} = 1.6mA	0		0.5	V
VCO and Charge Pump Section						
I_{BIAS}	V_{COI} Input Bias Current		0	25	50	μA
I_{CH}, I_{DIS}	V_{COL} Charge and Discharge Current		495	660	825	μA
I_{CH}/I_{DIS}	V_{COL} Charge/Discharge Ratio		0.95	1.00	1.05	μA/μA
I_{OFF}	V_{COL} OFF State Current	$\overline{FINC}$ = 2.0 FDEC = 0.8	0	25	50	nA

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ELECTRICAL CHARACTERISTICS (Continued)

The following specifications apply over the recommended operating conditions of $T_A = 0$ to 70° C, $V_{CC} = 10.8$ to 13.2 V, $V_{AGC} = 5.0$ V, and external components as recommended above, unless specified (See Note 1.)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP NOTE 2	MAX	UNITS
VCO and Charge Pump Section (Continued)						
F_{MAX}	MAX VCO Frequency to Maintain + and − 5% Control Range Note 4		30			MHz
F_{VCO}	VCO Frequency Range Note 4	T_A = 25°C, V_{CC} = 12, V_{COL} = 6V C_V = 100pF, R_V = 640kΩ	9.7	10.0	10.3	MHz
K_{VCO}	VCO Voltage to Frequency Factor			2		%/V
Input AMP, AGC AMP, and DC Restore						
R_{IN}	INX, INY Differential Input Resistance		7	10	14	kΩ
$I_{GAIN1, 2}$	GAIN1, GAIN2 Bias Current		0.66	1.0	1.20	mA
I_{BIAS}	V_{AGC} Input Bias Current		0	5	20	μA
G_{MAGC}	AGC Transconductance at C_{AGC}			370		μMHOS
R_{AGC}	Control Range of AGC Loop to Regulate Composite Amplitude to within 2% of Nominal			7/1		V/V
BW	Bandwidth from INX, INY to Composite Note 4		10	15		MHz
GMDCR	DC Restore Transconductance			200		μMHOS
Peak Detectors						
I_{CH}	Charge Current		12.7			mA
I_{DIS}	Discharge Current	T_A = 25°C	25	45	60	μA
T_{CDIS}	Tempco of I_{DIS}			−0.17		μA/°C
Voltage Reference						
V_{REF}	Reference Voltage	T_A = 25°C	4.85	5.10	5.35	V
TC	Tempco			50		ppm/°C
R_{OUT}	Load Regulation			2		mV/mA
PSRR	Line Regulation			10		mV/V
I_{SINK}	Maximum SINK Current		0.8			mA
Output Amplifiers (POSA, POSB)						
V_{OS}	Input Offset	V_{CAP}1-4 = 6V	−10	0	10	mV
A_V	Gain		1.23	1.28	1.33	V/V
A_{VA}/A_{VB}	Gain Tracking		−3	0	+3	%
V_{OUT}	Output Voltage Range		1.0		9.5	V
I_{SRC}	Output Source Current		5			mA
I_{SNK}	Output Sink Current		2			mA
SR	Slew Rate			2.5		V/μs
BW	3 dB Gain Bandwidth			3		MHz

Note 1: 0° C to 70° C operating temperature range devices are 100% tested with temperature limits guaranteed by 100% testing, sampling, or correlation with worst-case test conditions.

Note 2: Typicals are parametric norm at 25° C.

Note 3: Pin 25 is an open collector output which should not exceed 7 volts in the high state.

Note 4: This parameter is guaranteed but not 100% tested and is not used in outgoing quality level calculations.

APPLICATION HINTS

Using a nominal on-track servo signal, amplitude adjustment should be made as follows:

1. Set composite signal amplitude, measured at pin TP, by adjusting voltage at pin V_{AGC} (approximately 4.7 volts). The composite signal should be set to 1.75 volts base to peak of an on-track position pulse (an off-track position pulse will be about 3.5 volts maximum).

2. Adjust Rg so that the VGA is in mid-range. This is determined by measuring the voltage at pin C_{AGC}; it should be approximately 0.9 volts. C_{AGC} voltage will vary approximately ±0.5 volts over the AGC range.

FUNCTIONAL DESCRIPTION

Input Amplifier

The input amplifier is equivalent to a wide-band 592 type video amplifier and provides amplification and buffering to the AGC circuitry. The Inputs INX and INY, which must be AC coupled, accept the composite analog signal from the servo head differential preamplifier. Internal input termination resistors eliminate the need for external bias resistors. Prefiltering of the signal is normaly desired to eliminate unwanted components. External components R_G and C_G determine the input amplifier's low frequency cutoff and gain as follows:

$$FC = \frac{1}{2\pi\ (R_G + 60\Omega)\ C_G} \qquad A_V = \frac{1700}{R_G + 60\Omega}$$

Where: C_G = External series capacitance between pins GAIN1 and GAIN2

R_G = External series resistance between pins GAIN1 and GAIN2

Automatic Gain Control (AGC)

The purpose of the AGC loop is to maintain a constant peak output voltage level at outputs POSA and POSB. This peak level is established by the reference voltage applied to pin V_{AGC}.

$$V_{P\text{-}P\ (Composite)} = K1 \times V_{AGC} + K2$$

Where: K1 = 0.65

K2 = 0.41V

In this closed-loop system, the peak detector output voltages are fed back and combined with the V_{AGC} voltage to provide a gain control current. The current controls the variable gain amplifier (VGA) and is compensated at pin C_{AGC} to provide control of AGC bandwidth. The bandwidth of the entire AGC loop is determined by:

$$BW = \frac{K\ V_{VAGC}}{2\pi\ C_A}$$

Where: K = 4.3×10^{-4}

V_{VAGC} = External reference voltage at pin V_{AGC}

C_A = External capacitance at pin C_{AGC}

Optimum system stability is achieved by deriving V_{VAGC} from the V_{REF} output using a resistive divider.

Composite Amplifier

The input amplifier and AGC circuit of the ML4401 operate in a differential signal mode to provide good common mode and power supply rejection. The composite amplifier converts the differential signal into a buffered single-ended signal for the peak detector circuitry. The DC base line of the composite signal is equal to V_{REF} . The bandwidth of the DC restore function is controlled by capacitor C_D at pin C_{DC} with the following relationship:

$$BW = \frac{gm}{2\pi\ C_D}$$

Where: gm = 1/5 kΩ

C_D = External capacitance at pin C_{DC}

The composite signal is available at pin TP and is normally left unconnected. For short circuit protection a 425Ω resistor is connected in series with pin TP internally.

Synchronization Pulse Separator

The SYNC pulse separator is a threshold comparator with hysteresis which passes pulses from the composite amplifier above a set threshold. It provides a buffered open collector TTL output. The SYNC output, when gated through an external one-shot, is used to control the external gate timing and PLL logic.

Peak Detector

The peak detector circuit captures the peak signal amplitude of the di-bit pulses. The gates are controlled by inputs GATE1 through GATE4. Timing is established by the external logic circuitry. The external peak detector capacitors are connected from pins CAP1 through CAP4 to ground. The peak detector discharge rate (set by CAP1-CAP4) determines the maximum track crossing rate during an access operation. The performance of this block can be enhanced by using the velocity output of the ML4403, ML4413 to create a velocity proportional discharge. The peak detector outputs are fed into internal differential amplifiers that calculate the track error signals and provide buffered outputs POSA and POSB as follows:

POSA = 1.25 (CAP1 − CAP2) + V_{REF}

POSB = 1.25 (CAP3 − CAP4) + V_{REF}

Voltage Controlled Oscillator and Charge Pump

The VCO and external phase compare logic provide a time base for peak detector gate sychronization. Inputs $\overline{FINC}$ and FDEC provide increment and decrement signals to the charge pump for changing the oscillator frequency. The $\overline{FINC}$ and FDEC inputs gate the charge pump for the duration of the pulse width. The RC timing network formed by C_V and R_V at pins VCOI, VCON, and VCOP control the oscillators center frequency. (See Typical Performance Characteristics)

R_V should be greater than 330Ω. Too low of a value will result in excessive power dissipation. RL1, RL2 and R_V should be approximately equal, although the values of RL1 and RL2 do not require accuracy.

The VCO output should only be taken from pin VCON. Charge pump capacitor C_{CP1} is connected from pin VCOL to ground. Components R_{CP} and C_{CP2} are also connected in series from pin VCOL to ground to provide VCO loop compensation.

Internal Voltage Reference

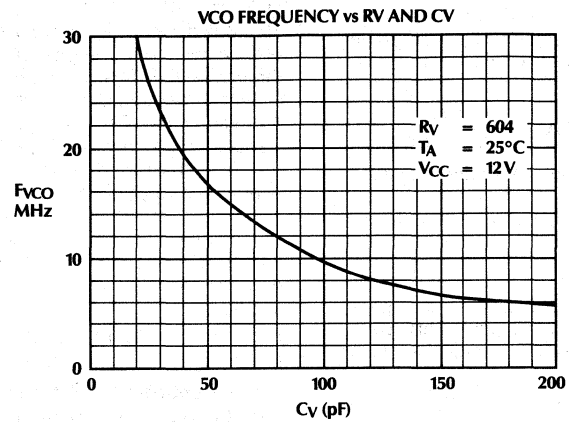
V_{REF} is an internal band-gap voltage reference. It is buffered and available at pin V_{REF} and is used by the ML4402, ML4403, ML4404 and other chips requiring a 5 volt reference.

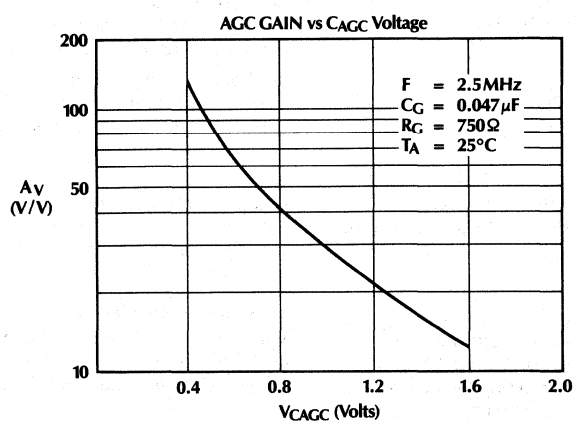
External Logic

The external logic provided by the user typically has a complexity of about 150 to 300 equivalent gates. Complexity and architecture depends on the users di-bit pattern and control function.

Note: Stray capacitance should be considered in applying the above relationships when low capacitor values are used. Stray capacitance of the integrated circuit terminal is typically about 2 to 3 pF.

TYPICAL PERFORMANCE CHARACTERISTICS





ORDERING INFORMATION

ORDERING NUMBER	PACKAGE	PIN COUNT	TEMPERATURE RANGE
ML4401CP	Plastic DIP	28 PINS	0°C to +70°C
ML4401YCQ	PLCC	28 PINS	0°C to +70°C

ML4402

Servo Driver

GENERAL DESCRIPTION

The ML4402 Servo Driver contains all of the control circuitry necessary to drive the head positioning actuator of a hard or rigid disk drive system. It receives the error signal generated from a servo controller circuit, such as the ML4403, ML4413, and drives an external transistor bridge which controls the head positioning voice coil actuator. The ML4402 output control circuitry includes current sense inputs to provide closed-loop control of actual actuator current. By using an external power transistor bridge, flexible thermal and space management is allowed as well as transistor selection which enables a wide application range.

Included in the device is a unique disable function which permits interruption of actuator current. During a disable, the output control amplifiers are shut down which cuts off all current to the external transistor bridge. Disable can be activated by a logic high into pin DIS or by the on-board low-voltage detector. Use of the low-voltage disable function prevents actuator response to a false error signal during a power failure. The low voltage detector can monitor up to two power supplies and has user definable low voltage trigger levels.

The ML4402, when combined with the ML4401/4431 Servo Demodulator, the ML4403, ML4413 Analog Servo Controller and the ML4404 Trajectory Generator, provides a flexible high-performance head positioning servo system.

FEATURES

- Low differential input offset voltage
- Contains all control circuitry necessary to drive an external transistor bridge
- Differential amplifiers internally compensated
- Unique disable function interrupts actuator current
- Programmable dual supply low voltage detector
- Single +12V power supply
- Compatible with Micro Linear's ML4401/4431 Servo Demodulator, ML4403, ML4413 Servo Controller and ML4404 Trajectory Generator chips

The ML4402-1 and ML4402-2 differ in offset voltage at the differential error signal inputs which is a result of the manufacturing trim process.

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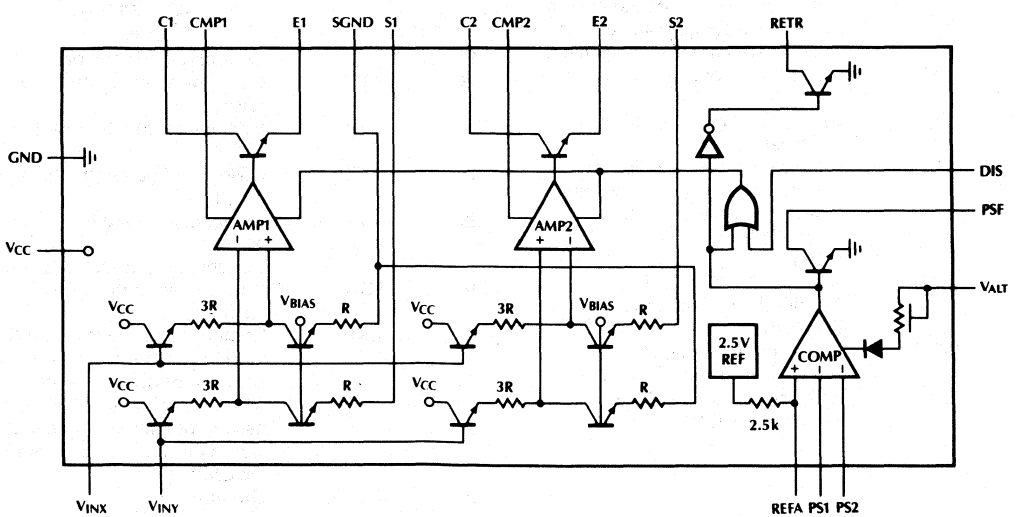
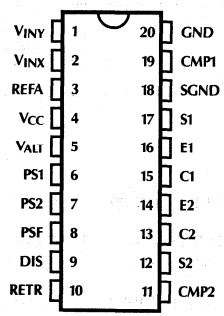
BLOCK DIAGRAM

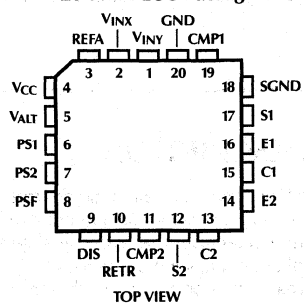


PIN CONNECTIONS



20-PIN DIP (Prototypes Only)

20-PIN PLCC Package



PIN DESCRIPTION

PIN #	NAME	FUNCTION
1	V_{INY}	Inverting input for error voltage signal. Used as a reference voltage (analog ground) input when using a single ended output from the ML4403 Servo Controller. Obtained from the V_{REF} output of the ML4401 Servo Demodulator.
2	V_{INX}	Non-inverting input for error voltage signal. Used as the signal input pin when using a single ended output from the ML4403.
3	REFA	Reference pin for low voltage comparator.
4	V_{CC}	+12 V power supply pin.
5	V_{ALT}	Optional +5 V power supply pin to keep the PSF pin operating if V_{CC} fails. With V_{ALT} at +5 V, the PSF pin will go low if V_{CC} goes to zero, or too low to operate the comparator.
6	PS1	Voltage input for low voltage comparator.
7	PS2	Voltage input for low voltage comparator.
8	PSF	Power supply failure indication, is an open collector output of comparator. Logic low indicates PS1 and/or PS2 voltage has gone below REFA.
9	DIS	Amplifier Disable pin. TTL input that disables both amplifiers with a logic high.
10	RETR	Return spring output, clamped open collector output, opposite logic polarity as pin PSF. Used to drive optional safety circuitry.
11	CMP2	Compensation node of AMP2 used to add additional compensation; the device is manufactured with approximately 27 pF of internal compensation. Bandwidth Effects: $f = \frac{gm}{2\pi (C + 27\,pF)}$ Slew Rate Effects: $SR = \frac{20\mu A}{C + 27\,pF}$ Where: gm = 150 μmhos C = External Compensation Capacitor C_{CMP1} or C_{CMP2}
12	S2	Current sense input for AMP2.
13	C2	Collector of output transistor of AMP2.
14	E2	Emitter of output transistor of AMP2.
15	C1	Collector of output transistor of AMP1.
16	E1	Emitter of output transistor of AMP1.
17	S1	Current sense input for AMP1.
18	SGND	Reference ground for S1, S2 feedback.
19	CMP1	Compensation node of AMP1, used to add additional compensation. The device is manufactured with approximately 27 pF of internal compensation. Bandwidth and Slew Rate effects are the same as the CMP2 pin.
20	GND	Ground.

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

Power Supply Voltage (V_{CC}) 14V
Terminal Voltage Range
(V_{INX}, V_{INY}, V_{ALT}, PS1, PS2, REFA, DIS) ..... −0.3 to V_{CC} +0.3V
S1, S2 ..... 7V
Terminal Input Current (CMP1, CMP2) 0.1mA
Storage Temperature Range ..... −65°C to +150°C
Junction Temperature (T_J) ..... 125°C
Lead Temperature (Soldering, 10 sec) ..... 260°C

OPERATING CONDITIONS

Supply Voltage
V_{CC} ..... 12V ±10%
V_{ALT} ..... 5V ±10%
Typical Component Values (Refer to Typical Application)
R_{OA} 470Ω
R_{OB} 240Ω
R_{OC} 150Ω
R_{OD} 0.5Ω

ELECTRICAL CHARACTERISTICS

The following specifications apply over the recommended operating conditions of V_{CC} = 10.8V to 13.2V, V_{INY} = 5V, T_A = 0 to 70° C, and external components as shown above unless otherwise specified (See Note 1).

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP NOTE 2	MAX	UNITS
Power Supply							
I_{CC}	V_{CC} Supply Current	Outputs unloaded, Pin REFA open			10	20	mA
I_{DD}	V_{ALT} Supply Current	V_{CC} = GND			150	500	µA
Amplifier Characteristics							
A_{V1}	Voltage Gain at Pin S1, $V_{S1}/(V_{INX}-V_{INY})$; Applies when $V_{INX} > V_{INY}$	V_{INX} = 5.1 and 6V V_{INY} = 5.0V		0.342	0.352	0.362	V/V
A_{V2}	Voltage Gain at Pin S2, $V_{S2}/(V_{INY}-V_{INX})$; Applies when $V_{INY} > V_{INX}$	V_{INX} = 4.9 and 4V V_{INY} = 5.0V		0.342	0.352	0.362	V/V
e_{AV}	Gain Linearity Error	$(A_{V1}-A_{V2})/0.5(A_{V1}+A_{V2})$		−2	0	2	%
V_{OS}	V_{INX}, V_{INY} Input Offset Voltage with Respect to Either Pin S1 or Pin S2	V_{OS} defined where A_{V1} or $A_{V2} > 0.16$ T_A = 25°C		−10		+10	mV
$V_{OS\ DIFF}$	Differential Input Offset	$V_{OS1}-V_{OS2}$ T_A = 25°C	ML4402-1 ML4402-2	−5 −10		+5 +10	mV
T_{CVOS}	Offset Voltage Tempco				15		µV/°C
V_S	Voltage Swing Range of Pin S1, S2 Above Ground	V_{S1}; V_{INX} = 6.7V V_{S2}; V_{INX} = 3.3V			0.5	0.65	V
I_{VR}	Input Voltage Range into V_{INX} and V_{INY}			3.3		10	V
I_{IB1}	Input Bias Current, V_{INX} and V_{INY}			0	10	75	µA
I_{IB2}	Input Bias Current, Pin S1 or S2 (sourcing)	V_{S1}, V_{S2} = GND		−1.6	−1.2	−0.8	mA
PSRR	Power Supply Rejection				60		dB
CMRR	Common Mode Rejection Ratio				80		dB
GBP	Gain Bandwidth Product	$C_{CMP1,2}$ = 0			0.83		MHz
SR	Slew Rate	$C_{CMP1,2}$ = 0			0.74		V/µS
Output Transistor Characteristics							
I_{OUT}	Output Current; I_{C1}, I_{E1}, I_{C2}, I_{E2}	$V_{INX}-V_{INY}$ = +1V V_{C1}, V_{C2} = 3V; V_{E1}, V_{E2} = 0.7V		50	100		mA

ELECTRICAL CHARACTERISTICS (Continued)

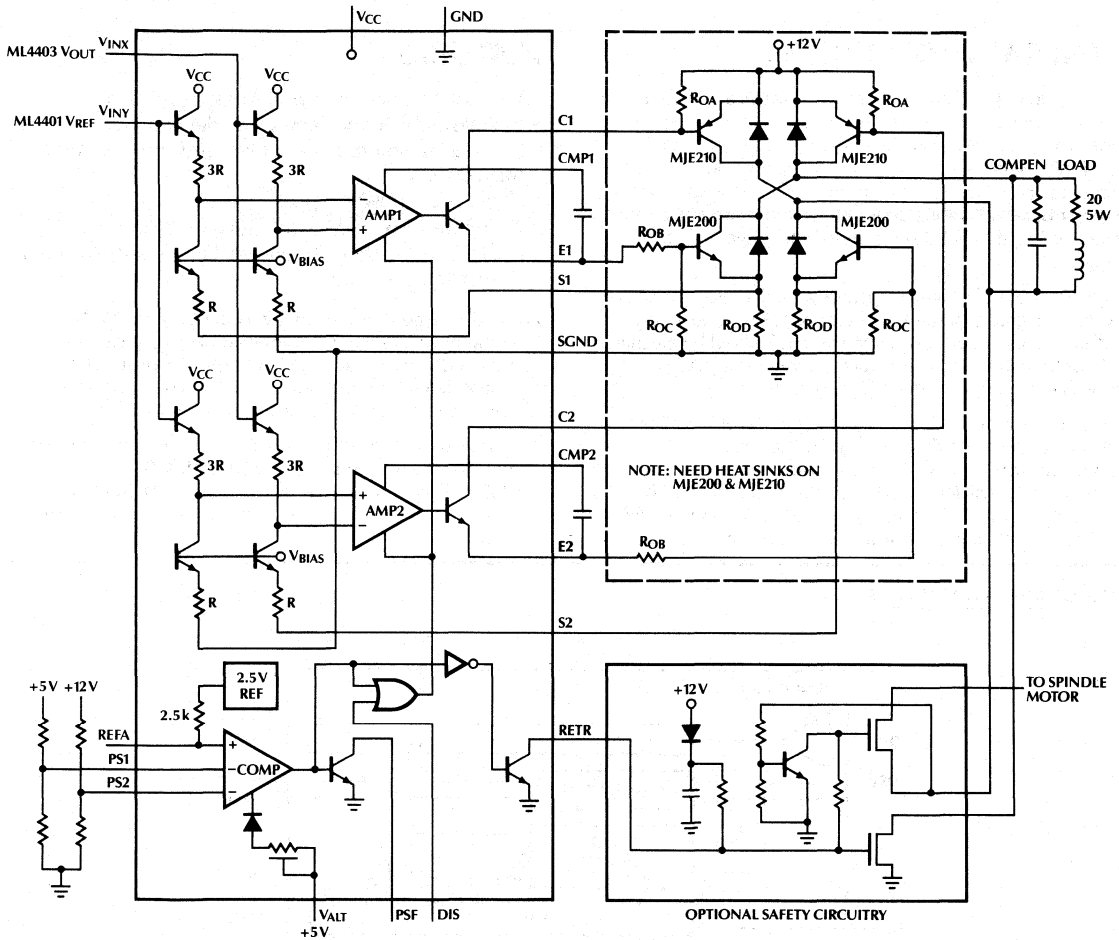
The following specifications apply over the recommended operating conditions of V_{CC} = 10.8 V to 13.2 V, V_{INY} = 5 V, T_A = 0 to 70° C, and external components as shown unless otherwise specified (See Note 1).

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP NOTE 2	MAX	UNITS
Internal Voltage Reference (V_{REF})						
PS_{MIN}	Minimum Allowable V_{CC} Voltage	Where V_{REF} > 2.48 V	4.75			V
V_{REF}	V_{REF} Voltage	T_J = 25° C	2.44	2.55	2.66	V
T_{REG}	V_{REF} Thermal Stability	Over Specified Range		50		ppm/° C
R_{REF}	R_{REF} Resistance	(Internal Resistor from V_{REF} to Pin REFA)		2.55		kΩ
Comparator						
V_{OS}	Input Offset Voltage, any Two Inputs		−30	5	30	mV
I_{IN}	Input Bias Current		−0.5	−0.1	0	μA
V_{OL}	PSF Logic 0 Voltage	I_{OL} = 1.6 mA	0	0.2	0.4	V
V_{OL}	RETR Logic 0 Voltage	I_{SINK} = 3 mA	0	0.5	1	V
I_{OH}	PSF Logic 1 Leakage Current	V_{PSF} = 5 V	−10	0.2	10	μA
I_{OH}	RETR Logic 1 Leakage Current	V_{RETR} = 2 V	−20	0.05	20	μA
Amplifier Disable Section						
V_{IH}	DIS Logic High Voltage		2.0			V
I_{IH}	DIS Logic High Current	V_{IH} = 2.4 V	−20		20	μA
V_{IL}	DIS Logic Low Voltage				0.8	V
I_{IL}	DIS Logic Low Current	V_{IL} = 0.4 V	−20		20	μA

Note 1: 0° C to 70° C operating temperature range devices are 100% tested with temperature limits guaranteed by 100% testing, sampling, or by correlation with worst-case test conditions.

Note 2: Typicals are parametric norm at 25° C.

TYPICAL APPLICATION DIAGRAM



ORDERING INFORMATION

PART NUMBER	PACKAGE	PIN COUNT	TEMPERATURE RANGE	COMMENTS
ML4402-1CP	PDIP	20 PINS	0°C to +70°C	Input Offset = ±5mV
ML4402-1CQ	PCC	20 PINS	0°C to +70°C	Input Offset = ±5mV
ML4402-2CP	PDIP	20 PINS	0°C to +70°C	Input Offset = ±10mV
ML4402-2CQ	PCC	20 PINS	0°C to +70°C	Input Offset = ±10mV

ML4403, ML4413

Servo Controller

GENERAL DESCRIPTION

The ML4403/4413 Servo Controller provides analog circuitry used in high performance trajectory and position control system for disk drive transducer heads. As a part of a head positioning servo system, this bipolar monolithic chip is designed to accept quadrature position signals and generate a servo error signal. While designed for minimum track access time, the ML4403/4413 supports a wide range of system designs.

Trajectory control functions include a track crossing detector, a velocity signal generator, and a velocity event detector. System stability and short settling time is insured by the interpolator function, which generates a ramp signal used to smooth the external position DAC output.

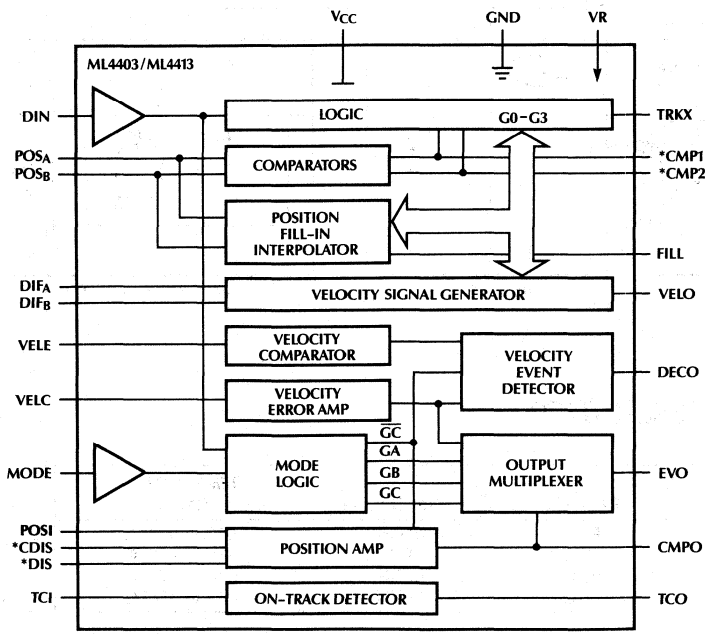
Position control is provided by a signal error amplifier within the device. When used with the ML4401/4431 Servo Position Demodulator, the track selection is performed by ML4401/4431 peak detector timing. This selection method eliminates track to track voltage offset problems and allows minimum track spacing. The ML4413 has a discharge function that enables zeroing of the external error amplifier compensation. This feature further reduces position settling time. An on-board on-track detector is provided which is used as a safety alarm by the controller for an off-track condition.

The ML4403/4413 Servo Controller, when combined with the ML4401 Servo Demodulator, the ML4402, ML4406/07/08 Servo Driver and the ML4404 Trajectory Generator provides a flexible closed-loop servo control system.

FEATURES

- Interpolate function smooths trajectory curve
- Flexible architecture allows user defined loop response
- Provides minimum track access time and maximum track density
- Single +12V power supply
- Compatible with ML4401 Servo Demodulator, ML4402, ML4406/07/08 Servo Driver and ML4404 Trajectory Generator

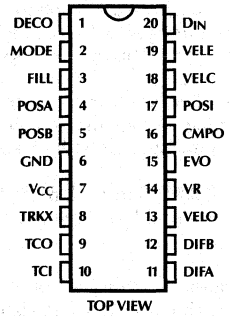
BLOCK DIAGRAM



* PINS WITH THE * IN FRONT ARE USED ON THE ML4413 ONLY.

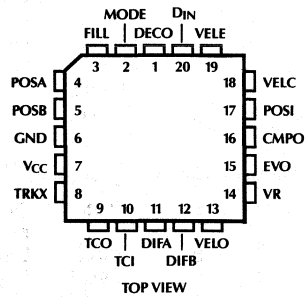
PIN CONNECTIONS

ML4403 20-PIN DIP (Prototypes only)



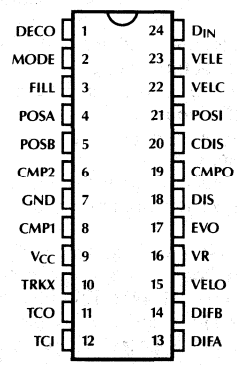
TOP VIEW

ML4403 20-PIN PLCC



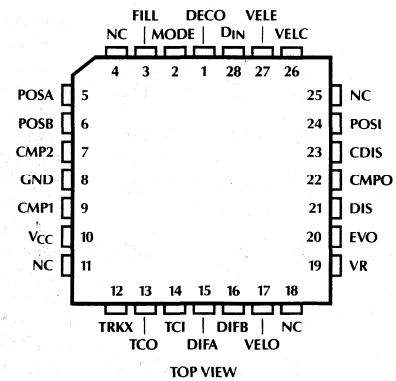
TOP VIEW

ML4413 24-PIN SKINNY DIP (Prototypes only)



TOP VIEW

ML4413 28-PIN PLCC



TOP VIEW

NC = NO CONNECTION

5

PIN DESCRIPTION

ML4403 DIP and PLCC	ML4413 DIP	ML4413 PLCC	NAME	FUNCTION
1	1	1	DECO	Digital output from the velocity event detector. In application, this output goes to a logic high when the actual actuator velocity reaches the trajectory curve. It remains high through the "braking" or negative acceleration. This pin goes low when velocity is zero and remains low during actuator acceleration. This pin is only allowed to go high during access mode. This output is open collector and requires an external pull-up resistor.
2	2	2	MODE	Digital input used to select Hold mode (low level) or Access mode (high level).
3	3	3	FILL	Analog output that provides a sawtooth waveform that, when summed with stair-step output of the external DAC, provides a smooth trajectory curve. Refer to Figure 3.
4	4	5	POSA	Analog input for quadrature position signals from demodulator (ML4401/
5	5	6	POSB	4431). Low pass prefiltering is recommended to eliminate peak detector ripple and external noise.
6	7	8	GND	Device ground connection.
	8	9	CMP1	Digital outputs that can be used for various control and count schemes. These
	6	7	CMP2	pins are only available on the ML4413. Timing is shown in Figure 3. These outputs are open collector outputs with an internal pull-up resistor tied to +5V.
7	9	10	V_{CC}	+12V power supply connection.
8	10	12	TRKX	Digital output that provides a logic transition at each track crossing which is defined as the point midway between two tracks. Refer to Figure 3. This output is open collector with an internal pull-up resistor tied to +5V.
9	11	13	TCO	Digital output from the on-track detector. Used in Hold mode, this pin goes to logic high when the position signal exceeds an established window. This output is open collector with an internal pull-up resistor tied to +5V.
10	12	14	TCI	Analog input into the on-track detector. The input is normally derived from the position signal.
11	13	15	DIFA	Analog inputs for differentiated quadrature position signals. These inputs are
12	14	16	DIFB	used to generate the velocity signal at output VELO.
13	15	17	VELO	Analog output that provides a continuous velocity (tachometer) signal by time multiplexing/inverting the DIFA, DIFB input signals.
14	16	19	VR	Reference voltage input. This value should typically be +5V, which is obtainable from the V_{REF} output of ML4401/4431.
15	17	20	E_{VO}	Multiplexed analog output of both velocity error and position error signals. This output is used as the input for the servo actuator driving circuity such as the ML4402.
	18	21	DIS	Digital input that, upon a logic high, electrically shorts pins CDIS and CMPO in order to keep the compensator capacitor discharged after entering hold mode. This pin and function is only available on ML4413. This function is used to reduce settling time when entering the Hold mode. Unlike pins MODE and DIN which float to logic high, this pin floats to logic low when left unconnected.
16	19	22	CMPO	Analog connection point for position compensation circuitry that is connected between this pin and POSI.
	20	23	C_{DIS}	Used to discharge external position compensation as shown in Figure 5. This pin is only available on ML4413. On the ML4403 this pin is internally connected to pin POSI.
17	21	24	POSI	Analog input for position control amplifier.
18	22	26	VELC	Analog input into velocity comparator. The velocity comparator trigger level is VR and is used for velocity event detection as described below.
19	23	27	VELE	Analog input for velocity error signal generated off-chip, referenced to VR.
20	24	28	D_{IN}	Digital input that controls actuator direction during Seek mode. This input affects the waveforms of outputs F_{ILL}, V_{ELO}, and E_{VO}. Refer to Figure 3.

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied. (All voltages referenced to GND.)

Power Supply Voltage, V_{CC} 14V
Terminal Voltage Range
VR ..... −0.3 to 7.0V
POSI ..... −0.3 to V_R +0.3V
DIN, POSA, POSB, DIFA, DIFB, VELE, VELC, MODE, DIS, TCI ..... −0.3 to V_{CC} +0.3V
Storage Temperature Range ..... −65°C to +150°C
Junction Temperature ..... +125°C
Lead Temperature (Soldering, 10 sec) ..... 260°C

OPERATING CONDITIONS

Temperature Range ..... 0°C to 70°C
Supply Voltage (V_{CC}) ..... 12V ± 10%

ELECTRICAL CHARACTERISTICS

The following specifications apply over the recommended operating conditions of V_{CC} = 10.8 to 13.2V, and V_R = 5.0V, unless otherwise specified. (See Note 1.)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP NOTE 2	MAX	UNITS
Power Supply						
I_{CC}	V_{CC} Supply Current	Outputs unloaded		38	60	mA
DIGITAL INPUT/OUTPUT CHARACTERISTICS						
Inputs D_{IN} and Mode						
V_{IH}	Logic High Voltage		2.0			V
I_{IH}	Logic High Current	V_{IH} = 2.4V	−40	1	40	µA
V_{IL}	Logic Low Voltage				0.8	V
I_{IL}	Logic Low Current	V_{IL} = 0.4V	−100	−50	0	µA
Input DIS (ML4413 Only)						
V_{IH}	Logic High Voltage		2.0			V
I_{IH}	Logic High Current	V_{IH} = 2.4V	0	180	250	µA
V_{IL}	Logic Low Voltage				0.65	V
Outputs TCO and TRKX						
V_{OL}	Output Low Voltage	I_{OL} = 1.6mA	0		0.4	V
V_{OH}	Output High Voltage	I_{OH} −50µA	2.4			V
t_{PD}	Propagation Delay	C_L = 15pF		200		ns
V_{TH}	Track Comparator Window	+ and − relative to VR	235	257	270	mV
Outputs CMP1 and CMP2 (ML4413 Only)						
V_{OL}	Output Low Voltage	I_{OL} = 0.4mA	0		0.4	V
V_{OH}	Output High Voltage	I_{OH} = −50µA	2.4			V
Output DECO						
V_{OL}	Output Low Voltage	I_{OL} = 1.6mA	0		0.5	V

5

ELECTRICAL CHARACTERISTICS (Continued)

The following specifications apply over the recommended operating conditions of V_{CC} = 10.8 to 13.2 V, and V_R = 5.0 V, unless otherwise specified. (See Note 1.)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP NOTE 2	MAX	UNITS
ANALOG INPUT/OUTPUT CHARACTERISTICS						
Outputs Fill, VELO, COMPO, and EVO						
V_{OS1}	Input Offset Voltage EVO, FILL			2		mV
V_{OS2}	Input Offset Voltage COMPO		−5		5	mV
V_{OS3}	VELO Input Offset Voltage Tracking Between 4 Multiplex States	Variation in output level in 4 multiplex states with DIFA = DIFB = 5 V	−10		10	mV
SR_1	Slew Rate FILL			4		V/μs
SR_2	Slew Rate COMPO, VELO, EVO			1		V/μs
V_{OUT}	Output Range All		1.0		9.0	V
I_{SRC1}	Source Current COMP, VELO, FILL		3			mA
I_{SRC2}	Source Current EVO		1.5			mA
I_{SNK1}	Sink Current FILL		0.25			mA
I_{SNK2}	Sink Current EVO, VELE		2			mA
I_{SNK3}	Sink Current COMPO		4			mA
Operational Amplifiers						
V_{OS}	Input Offset Voltage			2		mV
t_C	Average Temperature Coeff of Input Offset Voltage			20		μV/°C
I_{OS}	Input Offset Current			10		nA
I_B	Input Bias Current			100		nA
AV_{OL}	Open Loop Gain			200		V/mV
GBW	Gain Bandwidth Product			1		MHz
POSA, POSB Comparators						
V_{OS}	Input Offset Voltage			2		mV
V_{HYS}	Hysteresis			±500		mV
t_C	Average Temp Coeff of Input Offset Voltage			20		μV/°C
I_{OS}	Input Offset Current			50		nA
I_B	Input Bias Current			500		nA
A_V	Voltage Gain			200		V/mV
Pd	Response Time			500		ns

Note 1: 0°C to +70°C operating temperature range devices are 100% tested with temperature limits guaranteed by 100% testing, sampling, or by correlation with worst-case test conditions.

Note 2: Typicals are parametric norm at 25°C.

FUNCTIONAL DESCRIPTION

Power Supply and Reference Requirements

The ML4403/4413 operates from a single 12V ± 10% power supply, a 5.0V reference is required at pin VR which is available from pin V_{REF} on the ML4401/4431. VR serves as a system reference or "analog ground".

Modes of Operation

The device has two modes of operation, Access and Hold mode, which are controlled by pin MODE. To accomplish this, pin MODE controls the output multiplexer that selects either the velocity or position error signal.

Access Mode

The head actuator servo system uses Access mode to move the recording head(s) from one data track to another. Access mode circuitry within the ML4403/4413 includes analog functions necessary to measure and control head actuator velocity. The head velocity is controlled in a fashion that provides for a fast track-to-track movement and minimum settling time, which results in minimum track access time.

Actuator Trajectory

Similar to racing to the next stop sign, the fastest way to move from one data track to the next is through maximum acceleration and maximum braking (negative acceleration). In a disk drive the acceleration, either positive or negative, is governed by maximum available actuator current. To do this in a controllable manner and land on the target track, an achievable "braking curve" or trajectory function is first defined. At the beginning of Access mode, maximum acceleration is applied until the head velocity reaches this defined braking curve. Following the velocity profile of the trajectory curve, controlled braking stops the head on the target track.

Unlike acceleration, velocity and distance are accurately measurable and therefore controllable parameters. The trajectory function, as shown in Figure 2, is therefore expressed as velocity (track crossing rate) vs. distance (tracks to go). The desirable constant positive and negative acceleration will result in the expression of velocity as a function of the square root of distance. Therefore generation of the trajectory curve, velocity vs. distance, requires a non-linear function.

Actuator Trajectory Generation

At the start of a track access cycle, initial tracks-to-go count is supplied by the microprocessor. As the head moves, the count is decremented by the ML4403/4413 track crossing detector. To generate the analog "desired velocity" signal required for braking control, the tracks-to-go count (distance variable) is converted through a DAC (Digital to Analog Converter) with a non-linear square function included either before or after the conversion. One common approach used to obtain this non-linear function is to pre-process the tracks-to-go count (or multiple thereof) in the microprocessor. This can be performed algorithmically by the use of a look up table.

An alternate method, as shown in the typical application of Figure 5 places the non-linear function after the DAC conversion. The tracks-to-go count is maintained by a simple discrete down-counter that is initialized by the microprocessor. To eliminate the DAC steps and provide a smooth distance signal, the DAC output is summed with the ML4403/4413's FILL output in the external summing amplifier shown. The FILL output generates a sawtooth wave, as shown in Figure 3. This distance signal is then passed through the non-linear trajectory generator which generates the "desired velocity" signal used during braking. Generating a smooth trajectory curve reduces electrical/mechanical system oscillation and target track settling time.

Inductance-caused actuator lag can also create a target track overshoot problem. The trajectory curve generator, as indicated, can be designed to allow the microprocessor to modify the non-linear function in a way to account for this lag. Refer to Figure 2. The amount of lag will depend on duration of braking. Braking duration can be correlated against acceleration duration which is indicated by the timing of pin DECO.

The track crossing detector, which drives the trajectory position counter (see Figure 5), is generated with external logic. The input comparators have a fixed amount of internal hysteresis to provide noise immunity and media dropouts. The CMP1 and CMP2 outputs on the ML4413 can be used to perform more sophisticated sequential track crossing detection schemes. This can further reduce the detector's susceptability to media dropouts.

Hold Mode

At the end of an Access cycle, the head is stopped, or nearly so, on the target track. Hold mode is then selected to maintain accurate head positioning on that track. In this mode, the compensator output (CMPO) is multiplexed into the error amplifier output (EVO).

Track Selection

Track position is held by maintaining a zero value of the position input signal, with respect to VR. However, to allow selection of one of four track types and maintain error signal polarity, selection of POSA, POSB, or their inverse needs to be possible. Commonly this selection process is accomplished with an analog multiplexer-inverter matrix. The problem inherent with this approach is the track-to-track offset differences, caused by the amplifier input offset differences within the matrix.

The track selection scheme adopted by the ML4401/4431 and ML4403/4413 combination performs the multiplexing within the ML4401/4431. The selection/inversion operation is performed with the external support logic of the ML4401/4431 by changing the peak detector sample timing. This method eliminates the offset problems and allows a higher track density.

Position Amplifier and Compensator Zeroing

During track following mode (mode low), the compensator amplifier acts as an integrator which nulls out the position error. The timing of the transition between access mode and track follow is critical to minimize settling time. The velocity at which this transition occurs can be externally set by resistor RCMP (see Figure 5). During seek mode, the large compensator capacitor (CCMP) is discharged through an internal switch, so that the integrating loop sees no initial charge at the beginning of track follow mode. This can reduce settling time by several milliseconds.

The ML4413 provides a further enhancement of this feature. The switch can remain closed after the beginning of the seek-to-track follow transition by holding pin DIS high. In this way, the time at which the logic switches modes, and the time that integration begins can be controlled independently, and further settling time reduction can be acheived.

On-Track Detector

The on board on-track detector is a window comparator that provides a digital alarm of an off-track condition. This feature is useful as a safety to prevent data transfer during an off-track condition that may occur during track settling or mechanical jarring.

Velocity Control

As a necessary element of velocity control, a velocity signal is generated and is output at pin VELO. To accomplish this, the quadrature position signals are first differentiated through external RC networks and then input into pins DIFA and DIFB. The ML4403/4413 then time multiplexes these differentiated signals to obtain a continous velocity signal that is output at pin VELO. It is important to note that the trajectory generator shown in Figure 5 generates a "desired velocity" signal positive with respect to VR, and that VELO creates a negative signal with respect VR. This allows the use of a simple external resistor bridge to create the velocity error signal.

The summing function can be modified, as illustrated, by the action of pin DECO when the actual velocity reaches the trajectory curve. Modification can also be made just prior to that time with the "optional trajectory overshoot compensation" circuit, shown in Figure 5, that prevents overshoot due to actuator motor inductance.

Inductance-caused actuator lag can also create a track overshoot problem. The trajectory curve generator, as indicated, can be designed to allow the microprocessor to modify the non-linear function in a way to account for this lag as shown in Figure 2. The amount of lag will depend on duration of braking. Braking duration can be correlated against acceleration duration which is indicated by the timing of pin DECO.

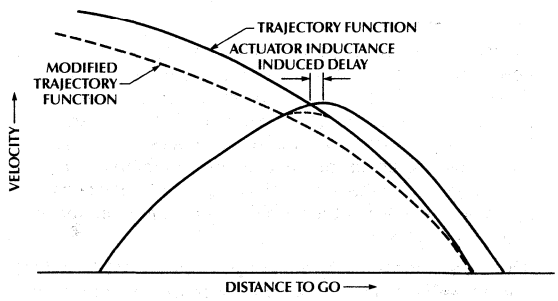


Figure 2.

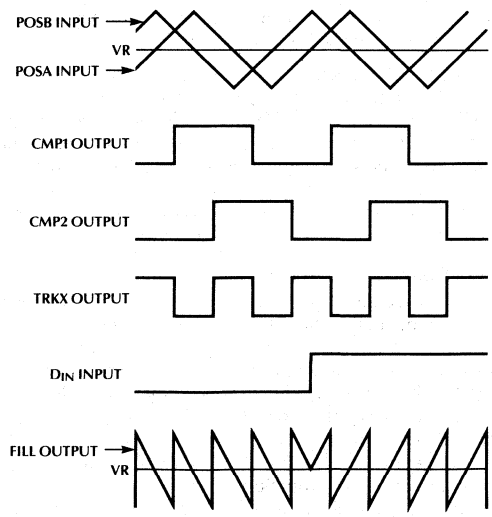
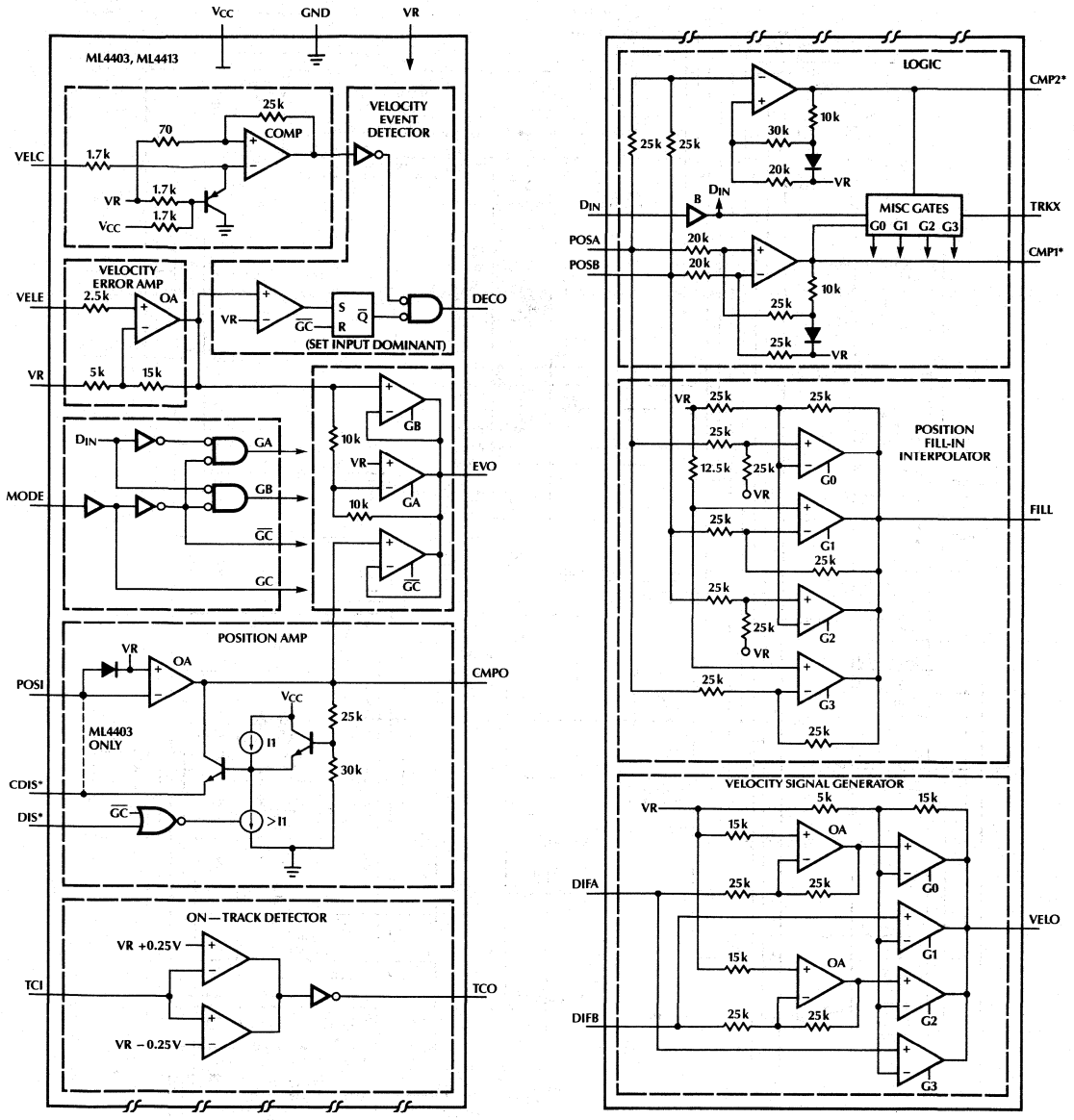


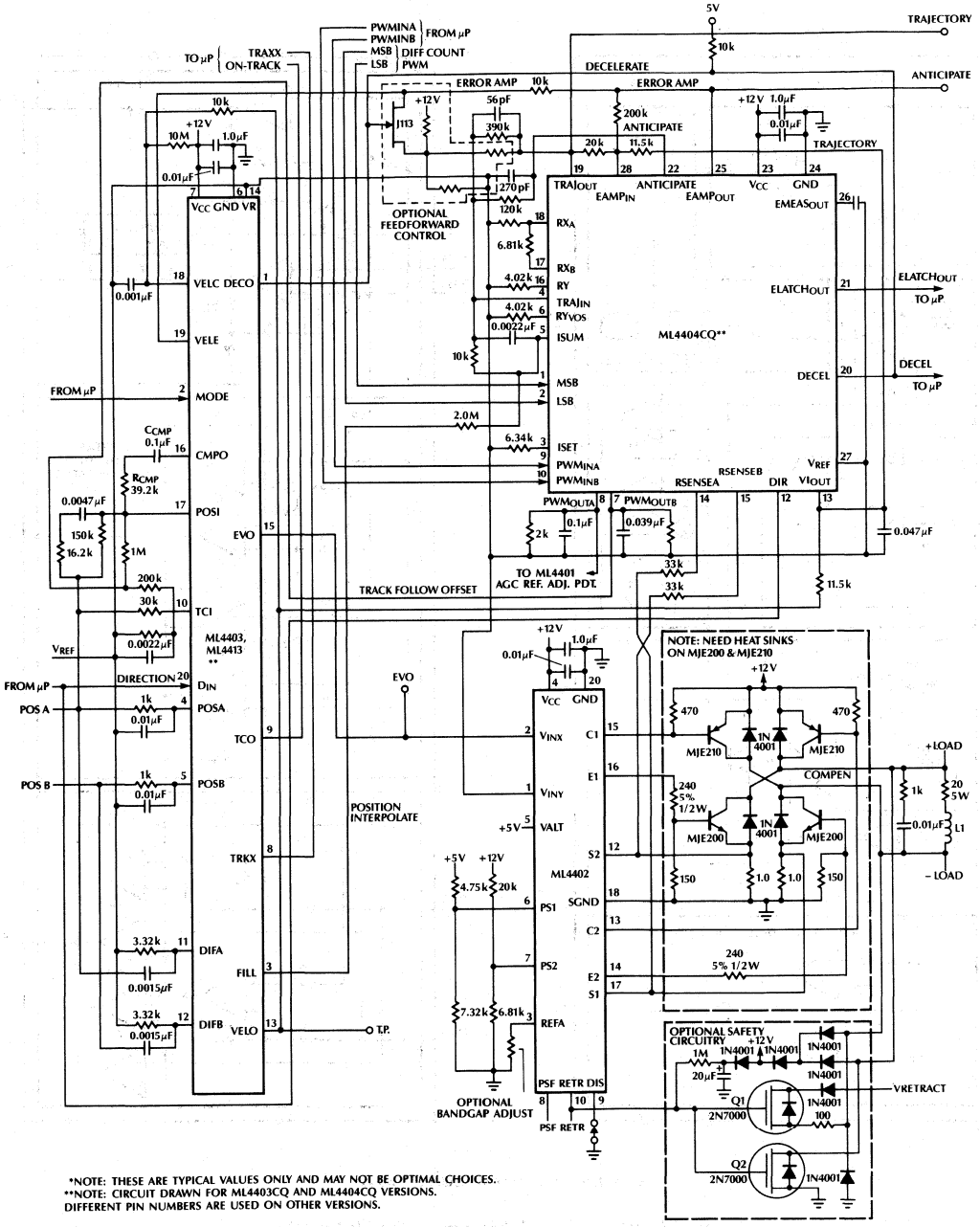
Figure 3.



*NOTE: THESE PINS ONLY AVAILABLE ON ML4413

Detailed Function of Block Diagram of the ML4403/13

Figure 4.



*NOTE: THESE ARE TYPICAL VALUES ONLY AND MAY NOT BE OPTIMAL CHOICES.
**NOTE: CIRCUIT DRAWN FOR ML4403CQ AND ML4404CQ VERSIONS.
DIFFERENT PIN NUMBERS ARE USED ON OTHER VERSIONS.

Figure 5. Connecting the ML4403 to the ML4404 Trajectory Generator and the ML4402 Servo Driver

ORDERING INFORMATION

PART NUMBER	PACKAGE	PIN COUNT	TEMPERATURE RANGE
ML4403CP	Plastic DIP	20 PINS	0°C to +70°C
ML4403CQ	Plastic PCC	20 PINS	0°C to +70°C
ML4413CP	Plastic DIP (0.3" Wide)	24 PINS	0°C to +70°C
ML4413CQ	Plastic PCC	28 PINS	0°C to +70°C

2092 Concourse Drive
San Jose, CA 95131
Tel: 408/433-5200
Telex: 275906

Micro Linear

ML4404

Trajectory Generator

GENERAL DESCRIPTION

The ML4404 Trajectory Generator provides the trajectory function for time optimal head positioning systems. The ML4404 receives position and velocity information from a servo controller, such as the ML4403, and generates the desired time optimal velocity trajectory. Desired Velocity is then compared with the actual velocity to create the error signal used by the servo controller.

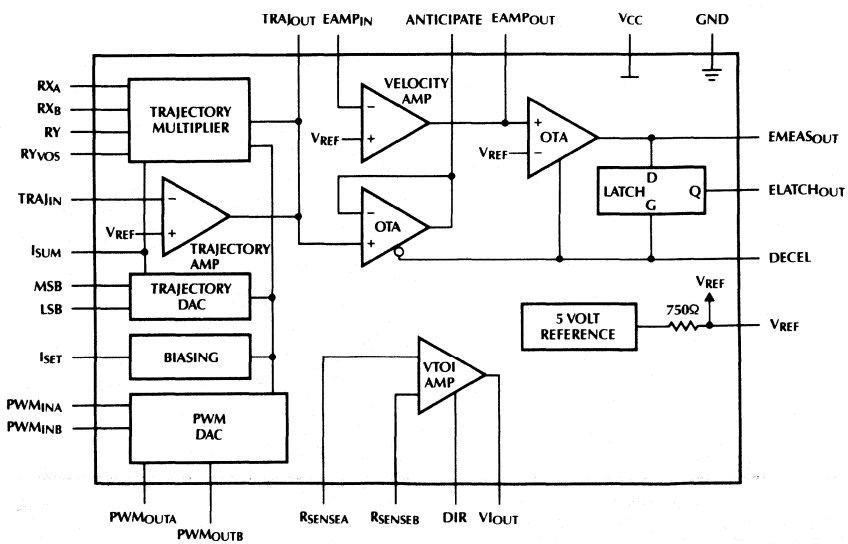
An anticipate function is included to compensate for phase shift error caused by actuator inductance. Another feature on the ML4404 is an error measure output which averages the velocity error during deceleration, so that the control system can monitor and adjust the necessary transducer gain for minimum access time.

The servo system usually requires accurate analog voltages to be set through software control. This is easily accomplished with a duty cycle to current translator function on the ML4404. By controlling the duty cycle of a TTL line, a processor can set an analog voltage on the translator output. These translators are fully independent blocks which can be used anywhere in the control system.

FEATURES

- Flexible architecture allows a user defined trajectory function
- Anticipate function compensates for phase delay caused by actuator inductance
- Feed forward function improves system stability
- Uncommitted PWM to current translators allow an analog voltage to be set with microprocessor control
- Single +12V power supply
- Compatible with Micro Linear's ML4401, ML4431 Demodulator, ML4402, ML4406/07/08 Driver, and ML4403, ML4413 Controller

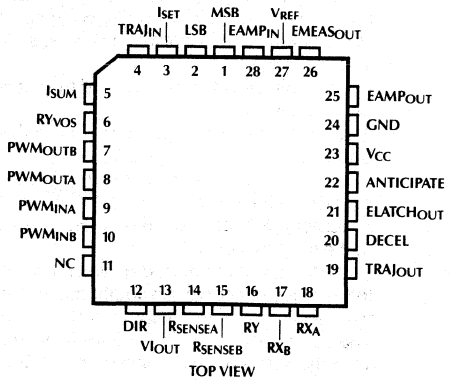
BLOCK DIAGRAM



Micro Linear

PIN CONNECTIONS

ML4404 28-Pin PLCC



PIN DESCRIPTION

PIN # ML4404	NAME	FUNCTION
1	MSB	Pulse width modulated (PWM) DAC TTL input (active low). The DAC output current is the position input to the trajectory generator. The MSB/LSB ratio is 8/1. The duty cycle of these two TTL inputs are controlled by a processor to form an 8-bit PWM DAC. The 3 higher order bits are modulated into the MSB.
2	LSB	Pulse width modulated (PWM) DAC TTL input (active low). The 5 lower order bits are modulated into the LSB input.
3	I_{SET}	A resistor (R_{SET}) from this pin to V_{REF} sets the internal bias levels. $I_{BIAS} = 3V/R_{SET}$. The nominal value should be between 0.25 and 0.5 mA.
4	$TRAJ_{IN}$	The trajectory generator input. This node is connected through an external filter to the sum of the PWM DAC output and the multiplier output.
5	I_{SUM}	The trajectory DAC output which is summed with the multiplier output feedback. An external RC filter network from this pin to $TRAJ_{IN}$ smooths out PWM DAC ripple.
6	RY_{VOS}	Nulls out the offset of the trajectory curve at the origin. A resistor equal to RY is connected from this pin to V_{REF}. This pin is available only on the ML4404.
7	PWM_{OUTB}	PWM to current translator output.
8	PWM_{OUTA}	PWM to current translator output.
9	PWM_{INA}	TTL input for the PWM to current translator. This converter translates a signal's duty cycle to an analog voltage.
10	PWM_{INB}	TTL input for the PWM to current translator. This converter translates a signal's duty cycle to an analog voltage.
11	NC	No Connection.
12	DIR	TTL direction input from the processor. Controls the polarity of the V/I converter output.

PIN DESCRIPTION (Continued)

PIN # ML4404	NAME	FUNCTION
13	VI_{OUT}	The V/I converter output. This circuit block monitors the differential voltage across the sense resistors of an actuator driver (such as the ML4402) and converts it to a bidirectional current whose scale factor is set by two external resistors. This current can be used to compensate for a noise reducing low pass filter in the output of the velocity transducer so that there is no net phase shift in the velocity signal.
14	R_{SENSEA}	A gain setting resistor is connected from this input to the sense resistor on the bridge driver.
15	R_{SENSEB}	A gain setting resistor is connected from this input to the sense resistor on the bridge driver.
16	RY	A resistor (RY) is connected from this pin to V_{REF}. RY and RX set the second order term of the trajectory curve.
17	RX_B	A resistor (RX) is connected between RX_A AND RX_B to set the second order term in the trajectory curve.
18	RX_A	A resistor (RX) is connected between RX_A and RX_B to set the second order term in the trajectory curve. An additional resistor (RK3) can be connected from RX_A to either the trajectory output ($TRAJ_{OUT}$) or to V_{REF} to set the third order term.
19	$TRAJ_{OUT}$	The trajectory output. This voltage relative to V_{REF} is proportional to the desired velocity. A resistor and capacitor from this pin to $TRAJ_{IN}$ sets the first order term and the loop compensation.
20	DECEL	Decelerate mode TTL input from the servo controller (such as the ML4403). When low (during accelerate) the anticipate output becomes a voltage follower, the error measure output is a high impedance, and the error sign is latched. When high (during deceleration) anticipate goes to high impedance, error measure integrates the velocity error, and the error sign latch is transparent.
21	$ELATCH_{OUT}$	The latched sign of the access loop error during deceleration. This TTL output can be used by the processor to adjust the velocity transducer gain to match that required by the mechanical system.
22	ANTICIPATE	Modifies the trajectory curve during acceleration and the accelerate to decelerate transition. This accounts for the time delay error caused by the actuator inductance.
23	V_{CC}	+12V power supply.
24	GND	Ground.
25	$EAMP_{OUT}$	Error amplifier output. The positive trajectory output (desired velocity) is summed with the negative velocity input (actual velocity) to form a difference output. The velocity input comes from the servo controller (such as the ML4403).
26	$EMEAS_{OUT}$	Error measure output. This output averages the value of the access loop error during deceleration.
27	V_{REF}	The analog zero reference point. This pin is intended to be driven with the ML4401 V_{REF} output. The ML4404 has an internal 5V reference connected through a current limiting resistor to this pin so that standalone operation/evaluation is available.
28	$EAMP_{IN}$	Error amplifier input. The INPUT summing node for the trajectory and velocity signals.

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied. (All voltages referenced to GND.)

Power Supply Voltage, V_{CC} 14V
V_{REF}, R_{SENSEA}, R_{SENSEB} ..... −0.3 to +7V
TTL Inputs, I_{BIAS}, $ELATCH_{OUT}$ ..... −0.3 to +7V
PWM_{OUTA}, PWM_{OUTB}, PWM_{OUTC} ..... −0.3 to V_{CC} +0.3V
Anticipate, V_{IOUT}, $EAMP_{OUT}$ ..... −0.3 to V_{CC} +0.3V
$EAMP_{IN}$, $TRAJ_{IN}$ ..... −0.3 to V_{CC} +0.3V
I_{SUM} ..... V_{REF} −1 to V_{REF} +1V
$TRAJ_{OUT}$, RX_A, RX_B, RY, RY_{VOS} ..... V_{REF} −1 to V_{CC} +0.3V
Storage Temperature Range ..... −65°C to +150°C
Junction Temperature (T_J) ..... +125°C
Lead Temperature (Soldering, 10 sec) ..... 260°C

OPERATING CONDITIONS

(See Figure 7)

Temperature Range ..... 0°C to 70°C
Supply Voltage (V_{CC}) ..... 12V ± 10%
R_{SET} 6.2K
RK1 ..... 110K
RY 3K
RY_{VOS} 3K
RX 6.8K
RK3 ..... 12K to V_{REF}
CCOMP 56pF
CF1 ..... 0.0022μF
CF2 ..... Open
RF 10K
R_{LOAD} ..... 20K to V_{REF}

ELECTRICAL CHARACTERISTICS

The following specifications apply over the recommended operating conditions of V_{CC} = 10.8 to 13.2V, V_{REF} = 5V, TA = 0 to 70°C, R_{FILT} = 10K, RY = RY_{VOS} = 3K, RK1 = 100K, RX = 6.8K, R_{SET} = 6.2K and RK3 = 12K to V_{REF} unless otherwise specified. (See Note 1.)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP NOTE 2	MAX	UNITS
DC CHARACTERISTICS						
I_{CC}	Power Supply Current			23	35	mA
DIGITAL INPUT/OUTPUT CHARACTERISTICS						
(Inputs PWM_{INA}, B, C, MSB, LSB, DIR)						
V_{IH}	Logic High Voltage		2.0			V
I_{IH}	Logic High Current	V_{IH} = 2.4V	−40	10	40	μA
V_{IL}	Logic Low Voltage				0.8	V
I_{IL}	Logic Low Current	V_{IL} = 0.4V	−40	1	40	μA
Inputs (DECEL)						
V_{IH}	Logic High Voltage		2.0			V
I_{IH}	Logic High Current	V_{IH} = 2.4V	−250	5	40	μA
V_{IL}	Logic Low Voltage				0.8	V
I_{IL}	Logic Low Current	V_{IL} = 0.4V	−1600	−850	0	μA
Outputs ($ELATCH_{OUT}$)						
V_{OL}	Output Low Voltage	I_{OL} = 1.6mA	0	0.3	0.4	V
V_{OH}	Output High Voltage	R_L = 5K to V_{REF}	2.4	5.0	5.5	V
Trajectory Amplifier (See Note 3)						
I_B	Input Bias Current		0	7	20	nA
A_V	Open Loop Gain			75k		V/V
BW	Unity Gain Bandwidth			1		MHz
PHIM	Phase Margin			75		DEG
Velocity Error Amplifier						
V_{OS}	Input Offset Voltage		−10		10	mV
I_B	Input Bias Current		0	50	300	nA
A_V	Open Loop Gain			120k		V/V
I_{SOURCE}	Source Current		4	8		mA
I_{SINK}	Sink Current		1	2		mA
BW	Unity Gain Bandwidth			1		MHz
PHIM	Phase Margin			75		DEG
V_{OUT}	Output Voltage Range		0.5		V_{CC} − 3	V

ELECTRICAL CHARACTERISTICS (Continued)

The following specifications apply over the recommended operating conditions of V_{CC} = 10.8 to 13.2V, V_{REF} = 5V, T_A = 0 to 70°C, R_{FILT} = 10K, RY = RY_{VOS} = 3K, RK1 = 100K, RX = 6.8K, R_{SET} = 6.2K and RK3 = 12K to V_{REF} unless otherwise specified. (See Note 1)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP NOTE 2	MAX	UNITS
Biasing						
V_{IS}	I_{SET} Voltage		2.00	2.02	2.06	V
PWM to Current Translators						
	I_{CHARGE}/I_{SET}, I_{DIS}/I_{SET}	PWM_{OUT} = 5.0V		0.98		mA/mA
	I_{CHARGE}/I_{DIS}	PWM_{OUT} = 5.0V	0.910	0.99	1.10	mA/mA
V_{OUT}	Output Voltage Range		1.5		9	V
Transconductance Amps						
V_{OS}	Input Offset Voltage		-10		10	mV
gm	Transconductance			1700		μMhos
I_{OUTMAX}	Max Output Current			90		μA
I_B	Input Bias Current			4.5		μA
Latch/Comparator						
I_B	Input Bias Current		0	2	10	μA
V_{OS}	Input Offset Voltage		-10		10	mV
A_V	Open Loop Gain			15k		V/V
t_{pd}	Propagation Delay	C_L = 10pF, R_L = 2K to V_{REF}		60		ns
V/I Amp						
I_{OS}/I_{SENSE} *100	Sense Current Offset	$I_{SENSEA} = I_{SENSEB}$ 0.1mA < I_{SENSE} < 1mA V_{IOUT} = 5V	-2	0	2	%
V_{SMAX}	Max R_{SENSE} Voltage		0.5	0.64		V
V_{OUT}	Output Range		1.5		9	V
Trajectory DAC						
I_{MSB}/I_{SET}	MSB Current			0.98		mA/mA
I_{MSB}/I_{LSB}	MSB to LSB Ratio		7.8	8.00	8.5	mA/mA
Trajectory Multiplier (Note 4)						
V_{OS}	V_{OUT} – V_{REF} at Origin	V_{OUT} at I_{SUM} = 0	-5		5	mV
	V_{TRACK1} : $V_{TRACK32}$	(V_{OUT} at I_{LSB}/32)/(V_{OUT} at I_{LSB})	0.090		0.140	mV/mV
	V_{TRACK2} : $V_{TRACK32}$	(V_{OUT} at I_{LSB}/16)/(V_{OUT} at I_{LSB})	0.165		0.205	mV/mV
	V_{TRACK4} : $V_{TRACK32}$	(V_{OUT} at I_{LSB}/8)/(V_{OUT} at I_{LSB})	0.270		0.320	mV/mV
	V_{TRACK8} : $V_{TRACK32}$	(V_{OUT} at I_{LSB}/4)/(V_{OUT} at I_{LSB})	0.430		0.470	mV/mV
	$V_{TRACK16}$: $V_{TRACK32}$	(V_{OUT} at I_{LSB}/2)/(V_{OUT} at I_{LSB})	0.660		0.695	mV/mV
V_{LSB}	$V_{TRACK32}$	V_{OUT} at $I_{SUM} = I_{LSB}$	0.935		1.035	V
V_{CROSS}	Crossover Error	(V_{OUT} at $I_{SUM} = I_{LSB}$) – (V_{OUT} at $I_{SUM} = I_{MSB}/8$)	-25		+10	mV
	$V_{TRACK32}$: $V_{TRACK256}$	(V_{OUT} at I_{MSB}/8)/(V_{OUT} at I_{MSB})	0.305		0.325	mV/mV
	$V_{TRACK64}$: $V_{TRACK256}$	(V_{OUT} at I_{MSB}/4)/(V_{OUT} at I_{MSB})	0.450		0.470	mV/mV
	$V_{TRACK128}$: $V_{TRACK256}$	(V_{OUT} at I_{MSB}/2)/(V_{OUT} at I_{MSB})	0.670		0.685	mV/mV
	$V_{TRACK192}$: $V_{TRACK256}$	(V_{OUT} at I_{MSB}*3/4)/(V_{OUT} at I_{MSB})	0.840		0.860	mV/mV
V_{MSB}	$V_{TRACK256}$	V_{OUT} at $I_{SUM} = I_{MSB}$ (Full Scale + 1)	3.070		3.225	V
PSRR	Supply Rejection	at Origin at Full Scale		0.2 2		mV/V mV/V

Note 1: 0°C to +70°C operating temperature range devices are 100% tested with temperature limits guaranteed by 100% testing, sampling, or by correlation with worst-case test conditions.
Note 2: Typicals are parametric norm at 25°C.
Note 3: Minimum recommended load resistor is 10kΩ from the trajectory output to V_{REF}.

FUNCTIONAL DESCRIPTION

Power Supply and Reference Requirements

The ML4404 operates from a single 12V power supply. In addition, a 5.0V reference is required at pin V_{REF} which is available from the ML4401, ML4431. V_{REF} serves as a system reference or "analog ground".

Biasing

All of the critical internal biasing on the ML4404 is set as a function of an external resistor, R_{SET}. An internal feed-back loop forces the voltage on I_{SET} (pin 3) to be 2.0V. R_{SET} is connected from this pin to V_{REF} (5.0V) and the resulting current is used in the multiplier and duty cycle-to-current translators.

$$I_{BIAS} = (V_{REF} - 2) / R_{SET} = 3V / R_{SET}$$

The nominal value of I_{BIAS} should be between 0.25 and 0.50mA.

Trajectory Multiplier/Amplifier

The Trajectory Multiplier/Amplifier generates the optimal velocity output from the position-to-go input. The optimal velocity is the $TRAJ_{OUT}$ voltage relative to V_{REF}. The input position is set by the duty cycle of the MSB and LSB inputs.

During an access operation, the actuator is first driven to maximum acceleration, and then into braking or deceleration. To minimize access times the trajectory curve (velocity vs position) during deceleration must be accurately controlled so that the head stops exactly on the desired track (without overshooting or undershooting). The head is driven to maximum acceleration until this braking curve is reached. Then the velocity is controlled to follow this optimal trajectory during deceleration.

According to the theory for a second order system, time optimal access is achieved if the position is proportional to the square of velocity ($P = KV^2$, or $V = KP^{1/2}$). However, in the real system environment, this theory needs modification in two important areas. First, as shown in Figure 1, the slope of the trajectory at the origin (final position) is infinite for a pure square root function. This infinite slope would result in an infinite bandwidth servo loop. As a result, a first order linear term needs to be included which will reduce the slope of this curve near the origin. Second, at large velocity, the square root function is not quite optimal, due to non-zero actuator inductance. A higher order term to modify the curve in this region needs to be included.

This trajectory curve, with its first, second, and third order terms is implemented with a multiplier in the feedback loop of an opamp (see Figure 2). The position input is a current which is a fraction of I_{BIAS}, as discussed in the trajectory DAC section below. The first order term is implemented with a feedback resistor (RK1) directly in the feedback path of the op amp. This transfer function of this I/V converter is expressed by $V_{OUT} = RK1 * I_{IN}$. The second order term comes from the multiplier.

$$I_{IN} = (V_{OUT}^2 / (2.25\, I_{BIAS} * RX * RY))$$

With both terms together,

$$I_{IN} = \frac{V_{OUT}}{RK1} + \frac{V_{OUT}^2}{2.25\, I_{BIAS} * RX * RY}$$

The first order term dominates near the origin, and the second order term dominates, at higher velocities.

The multiplier is modified by the addition of a resistor (RK3) which results in the third order term. This resistor is connected from RXA (pin 18) to either $TRAJ_{OUT}$ or V_{REF}. As shown in Figure 3, the shape of the trajectory curve for large velocities can be adjusted in either direction from nominal, depending on which pins RK3 is connected between. It should be noted that the above equations are only approximate. The actual multiplier transfer function is not a pure second order function, even with RK3 unconnected. The multiplier is designed to approximate the required trajectory for most typical servo systems. For most applications, very little correction with RK3 will be required. On the ML4404, an additional resistor (RY_{VOS}) equal to RY can be included which nulls the offset of the curve near the origin.

Since the resistors R_{SET}, RK1, RX, RY, RK3, and RY_{VOS} are all external, any desired trajectory can be set. The constraints on these values are as of follows:

$V_{OUTMAX} < 1.5 * RX * I_{BIAS}$
$V_{OUTMAX} > 1.5 * RY * I_{BIAS}$
$V_{OUTMAX} < 3.5V$
$6k < R_{SET} < 12k$ for $V_{REF} = 5V$
$R_{FILT} < RK1/10$
$R_{FILT} * C_{FILT2} < RK1 * C_{COMP}$
$R_{LOAD} > 10k$ to V_{REF}

V_{OUTMAX} is the maximum trajectory output voltage (relative to V_{REF}).

Trajectory DAC

The trajectory DAC creates, a position input for the trajectory multiplier. The position input is controlled by the duty cycle of the TTL inputs MSB and LSB. For most applications the position information will be digitally encoded to 8-bit resolution — each code representing one track. Therefore, the full scale input of the trajectory curve is 255 tracks. The input current corresponding to this full scale is I_{BIAS}.

Since the duty cycle of a single line is difficult to control to 0.4% (1/256), the duty cycle to input current translator section is divided into 2 signals (MSB and LSB). As shown in Figure 4, the ratio between these two currents is 8/1. The 5 lower order bits of code are modulated into the LSB input, and the 3 higher order bits into the MSB input. For example, a position input of 32 tracks would correspond to the MSB line always inactive, and the LSB line always active. 256 tracks would be MSB always active, and the LSB always inactive. 1 track would be MSB always inactive, and LSB 1/32 of the period active.

In general for an 8-bit binary code D7 D6 D5 D4 D3 D2 D1 D0 where D7 is the high order bit, the active duty cycle for the MSB input is D7 D6 D5/8 and the active duty cycle for the LSB input is D4 D3 D2 D1 D0 /32. For example 10100011 (163 tracks) would be active 5/8 of a period on the MSB, and 3/32 of a period on the LSB.

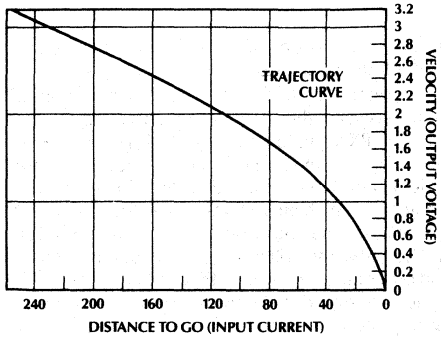


Figure 1.

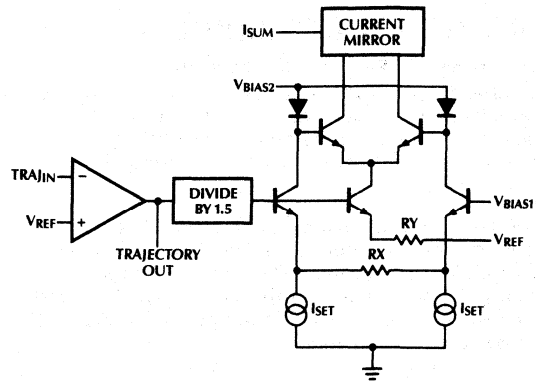


Figure 2.

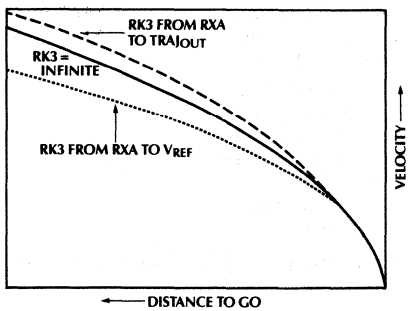


Figure 3.

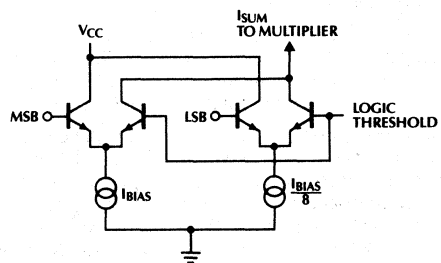


Figure 4.

AC Considerations — Trajectory Amp/Multiplier

The AC response of the trajectory output is primarily controlled by the external components C_{FILT1}, C_{FILT2}, R_{FILT}, RK1, and C_{COMP}. Four parameters must be considered to determine the values of these components.

First, the value of RK1 is set based on the bandwidth of the servo loop. RK1 sets the gain of the trajectory function at the origin. As the system bandwidth increases, more gain is required near the origin, and the value of RK1 increases.

Second, the exponential decay rate of the trajectory output during deceleration must be fast enough for the mechanical system to dominate the loop response. As the head approaches the target track, the multiplier (2nd and 3rd order terms) becomes less significant, and the first order term dominates. In this region, the exponential decay is dominated by the RK1 * C_{COMP} product. This product should be set at a frequency which is a few times higher than that of the position loop bandwidth, so that the overall phase margin is not significantly degraded.

Third, the filter components should be set such that the ripple from the trajectory DAC is minimized. Once the values for C_{COMP} and RK1 have been set, then the values of the remaining components, C_{FILT1}, C_{FILT2}, and R_{FILT}, can be determined. As the capacitance and resistance of these components increase the PWM ripple from the trajectory DAC is reduced. Due to the nonlinear nature of this circuit block, a mathematical analysis of the ripple is quite cumbersome, so the values of these components are best chosen empirically. The PWM ripple is dependent on R_{FILT}, C_{FILT1}, C_{FILT2}, as well as the duty cycle (50% duty cycle on the MSB will result in the largest ripple), and the frequency of modulation (the ripple is proportional to the square of the period).

Fourth, the R_{FILT}-C_{FILT} combination must be set such that the dynamic response of the trajectory output does not overshoot during deceleration. Ideally, the RC combination should be set such that the system is critically damped to a maximum deceleration input.

Note that a tradeoff exists between the ripple amplitude and the transient response. Too large a value of R_{FILT}-C_{FILT} will cause an overshoot in the transient response, and a low ripple level. Too small a value will provide acceptable transient response, but a large ripple amplitude. A range of values exists for most applications which results in acceptable performance for both ripple and transient response.

Anticipate

The function of the anticipate block is to modify the trajectory curve during acceleration. This compensates for the actuator inductance delay during the accelerate-to-decelerate transition.

At the start of a access operation, the actuator is driven into acceleration. The actuator velocity increases until either the maximum velocity is reached, or the trajectory deceleration curve is reached. As shown in Figure 5, if the trajectory curve is reached first, then the actuator needs to be driven into deceleration so that the trajectory curve can be followed. This accelerate-to-decelerate transition requires that the

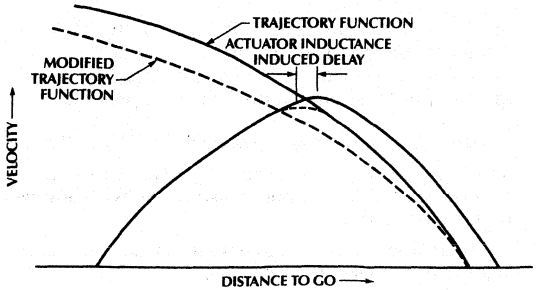


Figure 5.

current in the actuator be reversed. Since this cannot happen instantaneously (due to actuator inductance), a phase shift results. The actuator will then overshoot the desired trajectory, and miss the target track. However, if the curve can be modified (see Figure 5) such that the accelerate-to-decelerate transition begins before the nominal trajectory is reached, this overshoot problem can be eliminated. This function is implemented with a switched transconductance amp. During acceleration (DECEL input low), the anticipate output becomes a voltage follower-the anticipate signal is identical to the $TRAJ_{OUT}$ signal. An external resistor from anticipate to $TRAJ_{IN}$ will modify the trajectory curve as required. During deceleration, the anticipate output becomes a high impedance and the normal trajectory curve is followed.

In addition to the external resistor, an external capacitor to V_{REF} sets the anticipate decay time constant equal to the current reversal time for the actuator.

Velocity Error Amplifier

The function of this block is to subtract the desired velocity (from the trajectory output) with the actual velocity (from the servo controller) to create a velocity error output. This error output is multiplexed through the servo controller into the servo driver during access mode (see ML4403, ML4413 data sheet).

Since the polarity of the velocity input from the ML4403, ML4413 is the opposite of the trajectory output polarity, the difference function is accomplished with a summing amplifier, as shown in the application diagram. The summing resistors and the feedback resistor are external.

V/I Amp — Velocity Filter

The function of this block is to create a low noise velocity input. The velocity error amp requires that a clean, noise-free velocity input be compared with the desired velocity (from the trajectory output) to create a velocity error signal.

One way to create this velocity signal is to differentiate position. However, the differentiated signal will be noisy, and this noise can excite the mechanical resonances in the system. Another way to create velocity is to integrate acceleration. This eliminates the noise problem, however, the integrator DC accuracy will be poor due to the drift.

The ML4404 uses both of these techniques to achieve a low noise tachometer function which will operate at low frequencies noise from the mechanical resonances is attenuated by the RC filter. The filter output is then summed with a current proportional to acceleration.

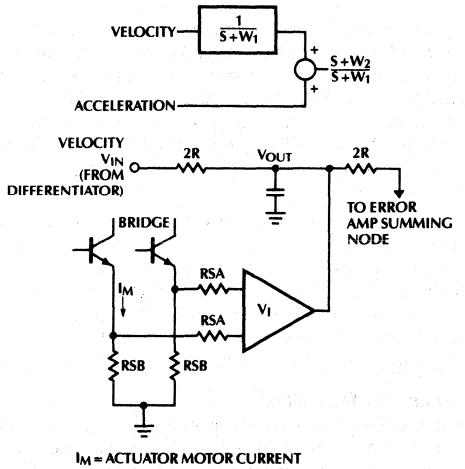


Figure 6.

The V/I amp creates this current by monitoring the sense resistors in the bridge driver. The resulting transfer function has both a pole and a zero, and can be expressed by:

$$\frac{V_{OUT}}{V_{IN}} = \frac{R*(M*RSB/(KF*KT*RSA))*S + 1}{R*C*S + 1}$$

Where KT = The velocity transducer gain (from differentiator)

KF = Motor force constant

M = Total moving mass

The above equation is a first order approximation which assumes that the, frictional components of the system (such as windage) are negligible. If the pole and zero are set to identical frequencies, then an all pass function is achieved. To do this, first, set the pole (W = 1/RC) at a frequency much lower than the mechanical resonances. Then set the scaling resistors, RSA, such that:

$$RSA = M*RSB/(KF*KT*C)$$

Note that setting a lower corner frequency results in increased dependence on the actuator current being an accurate representation of true acceleration. Some frictional terms and bias forces (such as flex cable force), as well as variations in KF, will distort this relationship. The lower limit on this corner frequency will be determined by these non ideal effects.

Error Averaging

The velocity error output should ideally be within a few millivolts of V_{REF} (near zero error) through the deceleration region. However, due to manufacturing tolerances, this error will not be identical for each drive. The $EMAS_{OUT}$ and $ELATCH_{OUT}$ pins, allow this error to be nulled out for each individual system.

During deceleration (DECEL input high) a transconductance amplifier is switched on (see Block Diagram) and the velocity error output is integrated through an external capacitor. This average velocity error is then compared with V_{REF} and sent to $ELATCH_{OUT}$ (TTL output).

5

During acceleration (DECEL input low) the amplifier is switched off (high impedance output) and the external capacitor is discharged to V_{REF} through an external resistor. In this condition, the TTL output, $ELATCH_{OUT}$, is held in its previous state. Since the velocity error during acceleration is not of interest, the $ELATCH_{OUT}$ during acceleration is the sign of the average velocity error output at the end of the previous deceleration cycle.

The processor can modify the velocity transducer gain based on the state of the $ELATCH_{OUT}$ signal. During a power-up sequence, this transducer gain can be iteratively adjusted through several seek operations until the velocity error is minimized. As described below, one of the PWM to current translators on the ML4404 could be used to adjust this transducer gain.

PWM To Current Translators

The function of this block is to convert the duty cycle of a TTL input line to an analog output voltage. To optimize a complex servo control system, the manufacturing tolerances of some components must be accounted for. Traditionally, the manufacturing process included an expensive sequence of measurement and adjustment to bring each individual unit within specification. A more cost effective solution is to perform these tasks through software control.

The ML4404 implements this function with TTL to current translators. The external components R_{PWM} and C_{PWM} set the desired characteristics. The operation of these translators can be expressed by:

$$VO = V_{REF} + I_{BIAS} * R_{PWM} * (2 * DUTY\ CYCLE/100 - 1)$$

Thus for a 50% duty cycle, the output voltage equals the reference voltage. The output voltage increases linearly with the input duty cycle.

The external capacitor (C_{PWM}) should be made sufficiently large to smooth out the PWM ripple.

The ML4404 has two translators. These stand-alone converters can be used for any purpose, but their intended functions are:

1. To set the AGC reference voltage on the ML4401, ML4431 servo demodulator.
2. To offset the position loop null location for data recovery (compensator inputs on the ML4403, ML4413 servo controller).
3. To offset the access arrival point for the trajectory (I_{SUM} node on the ML4404).

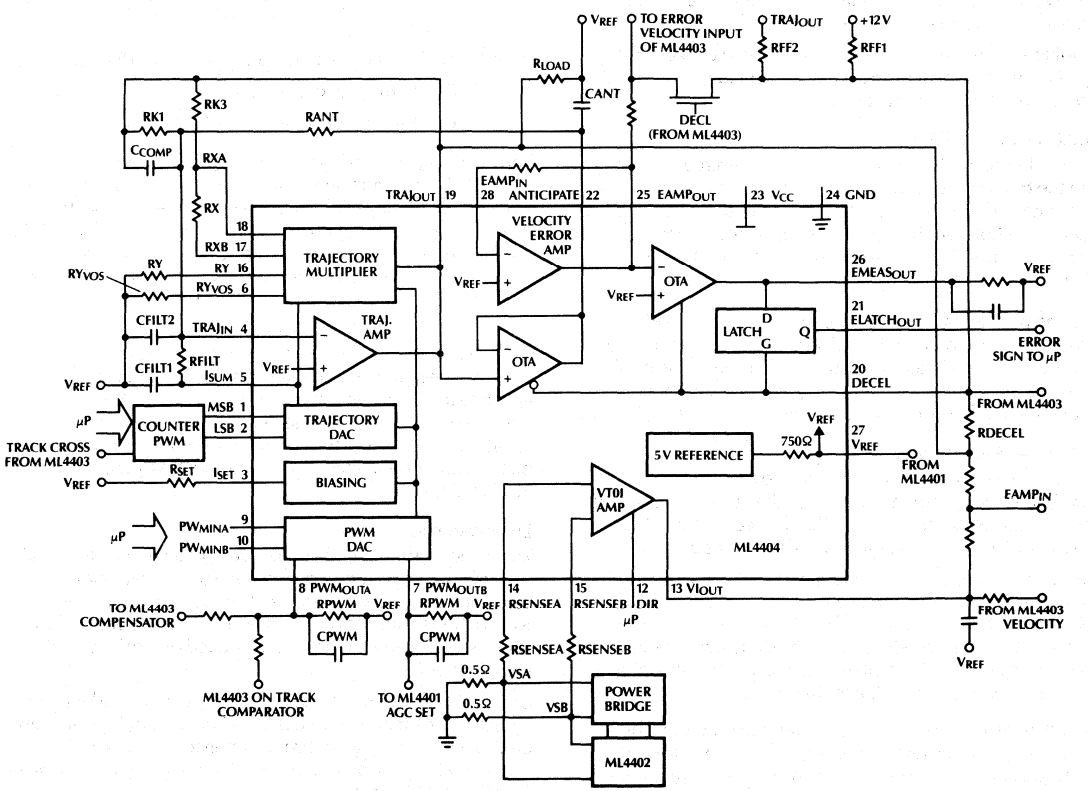
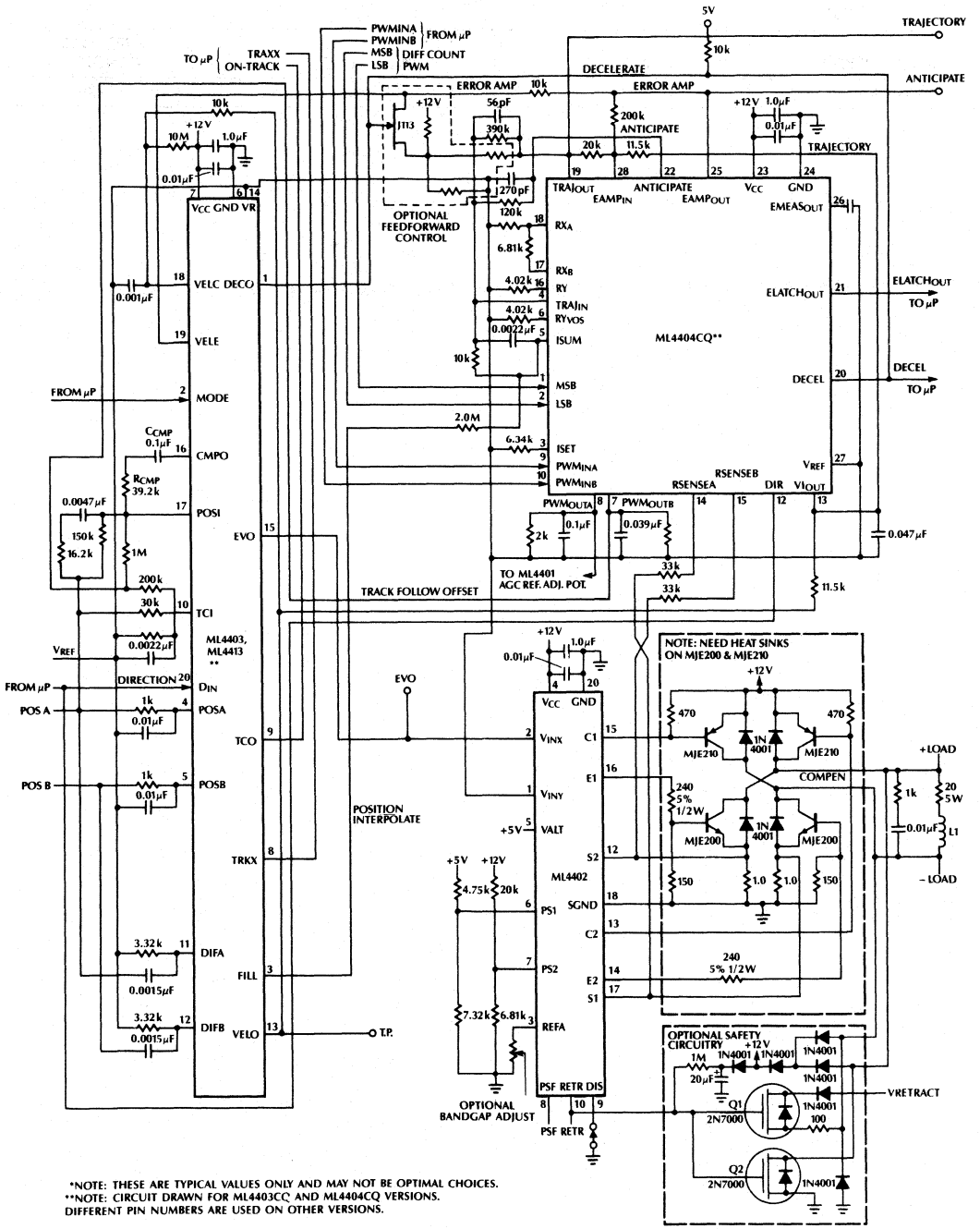


Figure 7. Typical External Component Connections



*NOTE: THESE ARE TYPICAL VALUES ONLY AND MAY NOT BE OPTIMAL CHOICES.
**NOTE: CIRCUIT DRAWN FOR ML4403CQ AND ML4404CQ VERSIONS. DIFFERENT PIN NUMBERS ARE USED ON OTHER VERSIONS.

Figure 8. Connecting the ML4403 to the ML4404 Trajectory Generator and the ML4402 Servo Driver

ORDERING INFORMATION

PART NUMBER	PACKAGE	PIN COUNT	TEMPERATURE RANGE
ML4404YCQ	PLCC	28 PINS	0°C to +70°C

ML4406, ML4407

Disk Voice Coil Servo Driver

GENERAL DESCRIPTION

The ML4406 is a voice coil power driver intended for use in Hard Disk servo systems. The ML4406 contains all power and control circuitry necessary to drive the voice coils of most 3.5" drives. In addition, power fail detection and head retraction functions are provided for orderly shut-down of the drive.

The transconductance is programmed by a logic input at 1/4 A/V and 1/24 A/V respectively, using a 1Ω sense resistor. This allows for greater DAC resolution in digitally controlled servos during track follow without compromising dynamic range during seek.

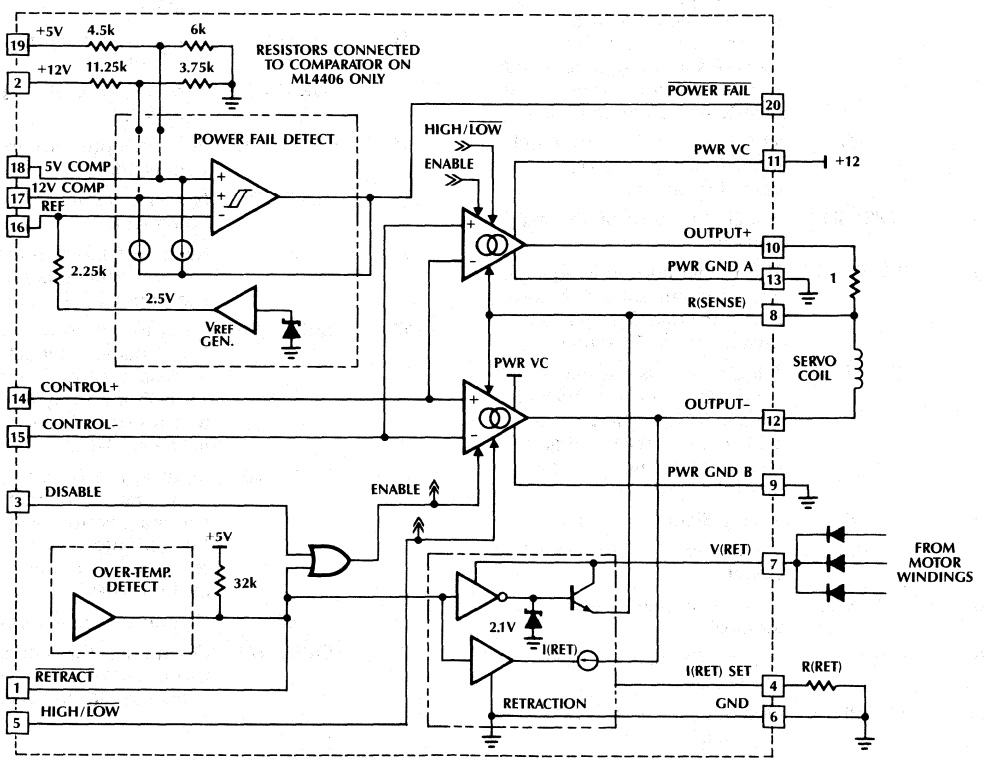
The retraction circuit, main drive cicruit, and control circuits are each powered from their own supplies. This allows maximum flexibility and provides for the lowest forward drop.

The power fail detection circuit includes a precision 2.5V bandgap reference with the option of either internally generated power-fail thresholds (ML4406) or open comparator inputs for adjustable thresholds (ML4407).

The ML4406 is implemented using Micro Linear's bipolar array technology. This allows for easy customization of the IC for a user's specific application.

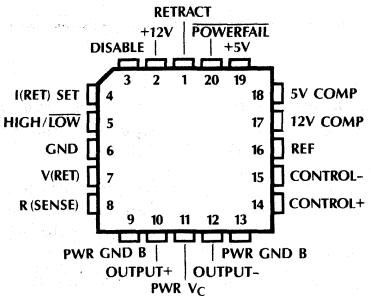
FEATURES

- 500mA power output with 1.5V total forward drop
- Low offsets, cross-over distortion and quiescent current
- Pin-programmable transconductance settings
- Retraction circuitry with programmable retract current, voltage limiting, and separate supply pin
- On-chip precision power fail detect circuitry
- Over-temperature protection with flag output
- Logic input available for disabling outputs



PIN CONFIGURATION

ML4406/ML4407
20-Pin PCC



PIN DESCRIPTION

PIN NO.	NAME	FUNCTION
1	$\overline{\text{RETRACT}}$	A logic "0" input causes the main outputs to tri-state and the retraction circuit to activate. This input also functions as a flag output and will go low in the event of an over-temperature condition.
2	+12V	12V power to the circuit and input to the power fail detection circuit.
3	DISABLE	A logic "1" turns off the main outputs.
4	I(RET) SET	The retract current is equal to 200 × the current which flows out of this pin. This pin is driven with a .7V source.
5	HIGH/$\overline{\text{LOW}}$	A logic "1" sets the trans-conductance gain to 1/4 while a logic "0" sets the gain to 1/24. Transconductance gain is voltage across R_{SENSE} ÷ the input voltage.
6	GND	Analog Signal Ground.
7	V(RET)	Power supply for the retract circuit.
8	R(SENSE)	Current sensing resistor terminal.
9	PWR GND B	Ground Terminal for power amplifier.
10	OUTPUT+	Output terminal for bridge amplifier.
11	PWR VC	Power supply for bridge amplifier.
12	OUTPUT–	Output terminal for bridge amplifier.
13	PWR GND A	Ground Terminal for power amplifier.
14	CONTROL+	Positive input for current command.
15	CONTROL–	Negative input for current command.
16	REF	Reference input to the Power Fail comparator. Leave open to use internal 2.5V reference.
17	12V COMP	Input to the Power Fail Comparator. Connect to an external resistor divider for the ML4407. Internally connected to a resistor divider from 12V in the ML4406.
18	5V COMP	Input to the Power Fail Comparator. Connect to an external resistor divider for the ML4407. Internally connected to a resistor divider from 5V in the ML4406.
19	+5V	5V power supply terminal.
20	$\overline{\text{POWER FAIL}}$	Open collector output drives low if pin 17 or pin 18 are below pin 16. Normally tied to pin 1.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (Pins 11, 13, 7, 2) 14V
Voltage Pins 19, 18, 17, 16, 1, 3, 5 ..... –.3V to +7V
Pins 14, 15 ..... –.3 to +V_{CC}
Output Current ..... ±750mA
Retraction Current 80mA
Retract Set Current (Pin 4) 3mA
Junction Temperature ..... 150°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (soldering 10 sec.) ..... 260°C
Thermal Resistance (θ_{JA}) ..... 60°C/W

OPERATING CONDITIONS

Temperature Range ..... 0°C to 70°C
Supply Voltage (PWR VC, +12V) ..... 12V ± 10%
+5V (Pin 19) ..... 5V ± 10%
V(RET) (Pin 7) ..... 2.5V to 16V
Control + Voltage Range (Pin 15 = 5V) ..... 0V to V_{CC}
Control – Voltage Range ..... 4V to 8V

Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, T_A = Operating Temperature Range, V_{CC} = 12V, R_{SENSE} = 1Ω, R_{COIL} = 15Ω, CONTROL– (Pin 15) = 5V, R_{SET} (Pin 4) = 1.2KΩ.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Amplifier						
Offset					±10	mA
Gain	Pin 5 = 2V		238	250	263	mA/V
	Pin 5 = 0.8V		39.6	41.7	43.8	mA/V
Bandwidth				100		KHz
Sinking Saturation	I_{OUT} = 100mA				.6	V
	I_{OUT} = 300mA				.8	
	I_{OUT} = 500mA				1.0	
Sourcing Saturation	I_{OUT} = 100mA				1.2	V
	I_{OUT} = 300mA				1.3	
	I_{OUT} = 500mA				1.5	
Retraction Circuit						
I(RET)SET				.75		V
Turn On Time				300		ns
Turn Off Time				2		ms
I(RET) Current	Pin 1 = 0.8V		34	50	65	mA
Power Fail Detection Circuit						
Reference Voltage			2.3	2.48	2.6	V
Reference Source Impedance				2.25		kΩ
Comparator Bias Current	ML4407 only, Pin 20 high			50	250	nA
Hysteresis Current	Pin 20 low, ML4407 only			10		μA
Offset Voltage	ML4407 only				10	mV
12V Threshold	ML4406 only		9.5	10	10.5	V
Hysteresis	ML4406 only			120		mV
5V Threshold	ML4406 only		4.40	4.575	4.75	V
Hysteresis	ML4406 only			30		mV
Logic Inputs						
Voltage High (V_{IH})			2	1.4		V
Voltage Low (V_{IL})				1.4	.8	V
Current High (I_{IH})	V_{IN} = 5V				±10	μA
Current Low (I_{IL})	V_{IN} = 0V	Except Pin 1	–40	–10		μA
		Pin 1 Only	–250	–160		μA

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ELECTRICAL CHARACTERISTICS (Continued)

Unless otherwise specified, T_A = Operating Temperature Range, V_{CC} = 12V, R_{SENSE} = 1Ω, R_{COIL} = 15Ω, CONTROL– (Pin 15) = 5V, R_{SET} (Pin 4) = 1.2kΩ.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Current Consumption					
Pin 19	I_{LOAD} = 0		1	2	mA
Pin 7	I_{RET} = 0		1	2	mA
Pin 2 + Pin 11	I_{LOAD} = 0		10	15	mA

FUNCTIONAL DESCRIPTION

POWER AMPLIFIER

The ML4406 power amplifier circuit is set up as a Howland current source with a fixed gain of 1/4 or 1/24 (set by driving pin 5 high or low respectively). This architecture yields minimal cross-over distortion while maintaining low output cross conduction currents. The gain figure refers to the ratio of input voltage to the output voltage seen across R_{SENSE}. For example, at a 1/4 gain setting with V– input at 2.5 and the V+ input at 4.5V, +500mA would flow through the coil using a 1Ω sense resistor. Under the same conditions with pin 5 low, the current would be 83mA. The ability to change from low to high gain allows more complete utilization of DAC resolution when in the track follow mode.

The output stage (Figure 2) is designed to provide minimal saturation losses and employs a "composite PNP" for the sourcing drive and a saturable NPN to sink current. Sourcing saturation drop is typically .9V while sinking saturation drop is typically < 0.4V.

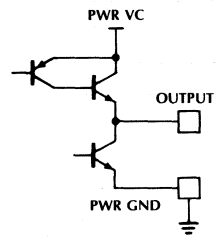

Figure 2. Main Power Output Stage

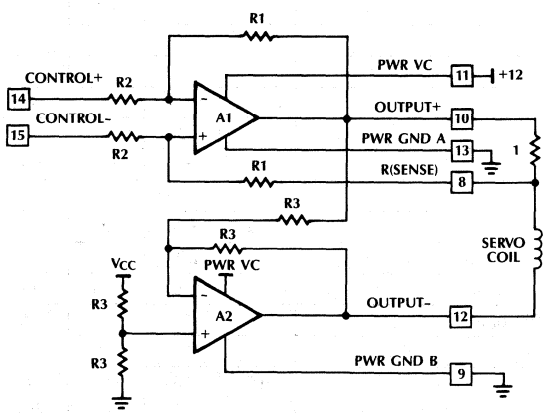

Figure 1. Power Amplifier Topology

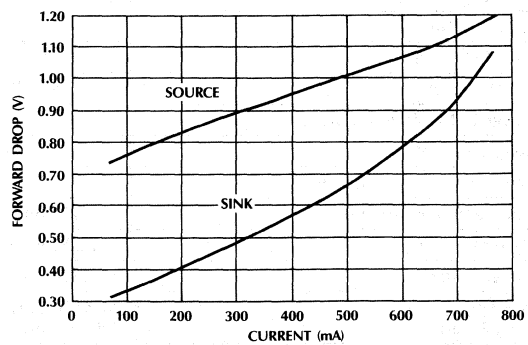

Figure 3. Output Saturation Voltage vs. Output Current (Power V_C = 12V)

FUNCTIONAL DESCRIPTION (Continued)

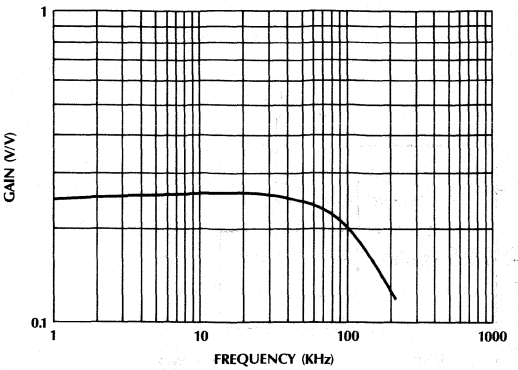

Figure 4. Gain vs. Bandwidth

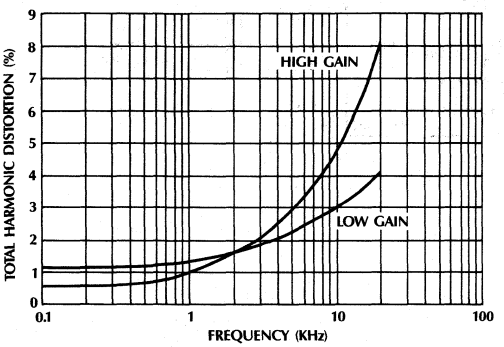

Figure 5. Total Harmonic distortion vs Frequency
Low Gain Setting ($V_{PIN\ 5}$ = 0), R_{SENSE} = 1Ω, V_{IN} = 2.4V_{P-P}
High Gain Setting ($V_{PIN\ 5}$ = 0), R_{SENSE} = 1Ω, V_{IN} = 0.4V_{P-P}

Power Fail Detect

The ML4406 power fail detection circuit consists of a precision trimmed reference, resistor dividers, and an "or-function" comparator with hysteresis. The 10μA current sink on the comparator input lowers the comparator's positive input by 15mV when the output of the comparator is high. This creates an effective hysteresis of 30mV at the 5V input (on the ML4406). The amount of hysteresis and threshold levels can be programmed by external resistor dividers on the ML4407. The impedance of the external divider sets the amount of hysteresis while the division ratio sets the power fail threshold. The output at pin 20 is open-collector and is normally tied to pin 1 which is internally pulled-up to 5V.

Retract

The retract circuit features a current sink which is programmed via external resistor from pin 4 to ground (R_{RET}). The output of the retract circuit is voltage limited to 1.4V. The current sink provides an acceleration limit during retract while the voltage limited source provides a velocity limit. Pin 1 (Retract Input) also serves as a flag to indicate an over-temperature condition on the die. Pin 1 goes low in the event of over-temperature, which occurs when the die temperature exceeds a safe operating limit (about 160°C).

The retraction current is set by programming R_{RET} where $I_{RETRACT}$ = 200 × 1.4/R_{RET}. The retract circuit works down to 3V on $V_{RETRACT}$ (Pin 7).

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APPLICATIONS

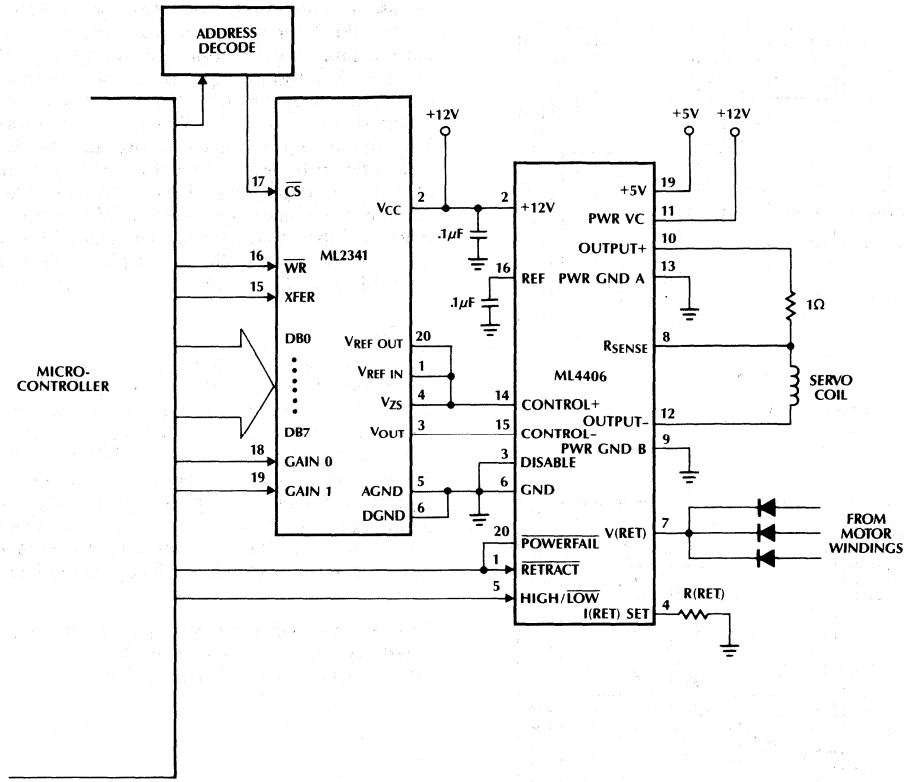

Figure 6. Typical Application: ML4406 used with ML2341 8-bit DAC provides up to 12-bit effective resolution

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ML4406CQ	0°C to +70°C	20-Pin MOLDED PCC
ML4407CQ	0°C to +70°C	20-Pin MOLDED PCC

Micro Linear

ML4408

Low Voltage Voice Coil Servo Driver

GENERAL DESCRIPTION

The ML4408 is a voice coil power driver intended for use in both High Performance 5V and 12V Hard Disk servo systems. The ML4408 contains all control circuitry necessary to drive the voice coils of most small drives. To maximize compliance voltage, the ML4408 includes two 1-Amp NPN drivers and provides drivers for external PNP transistors. In addition, power fail detection and a low voltage head retraction functions are provided for orderly shut-down of the drive.

The transconductance programmed by a logic input at 1/4 A/V and 1/24 A/V respectively, when using a 1Ω sense resistor. This allows for greater DAC resolution in digitally controlled servos during track follow without compromising dynamic range during seek.

The retraction circuit, main drive circuit, and control circuits are each powered from their own supplies. Retract is self-contained for 12V systems but allows the use of an external PNP for 5V systems to allow retraction with as little as 1V of back EMF from the spindle.

The power fail detection circuit includes a precision 1.5V bandgap reference and a power fail comparator.

The ML4408 is implemented using Micro Linear's bipolar array technology. This allows for customization of the IC for a user's specific application.

FEATURES

- Low saturation voltage (<1V at 1A)
- No cross-over distortion with low quiescent current
- Pin-programmable transconductance settings
- Retraction circuitry with programmable retract voltage and separate power pin operates to 1V
- On-chip precision power fail detect circuitry
- Over-temperature protection with flag output
- Operates from single +5V or +12, +5V supplies

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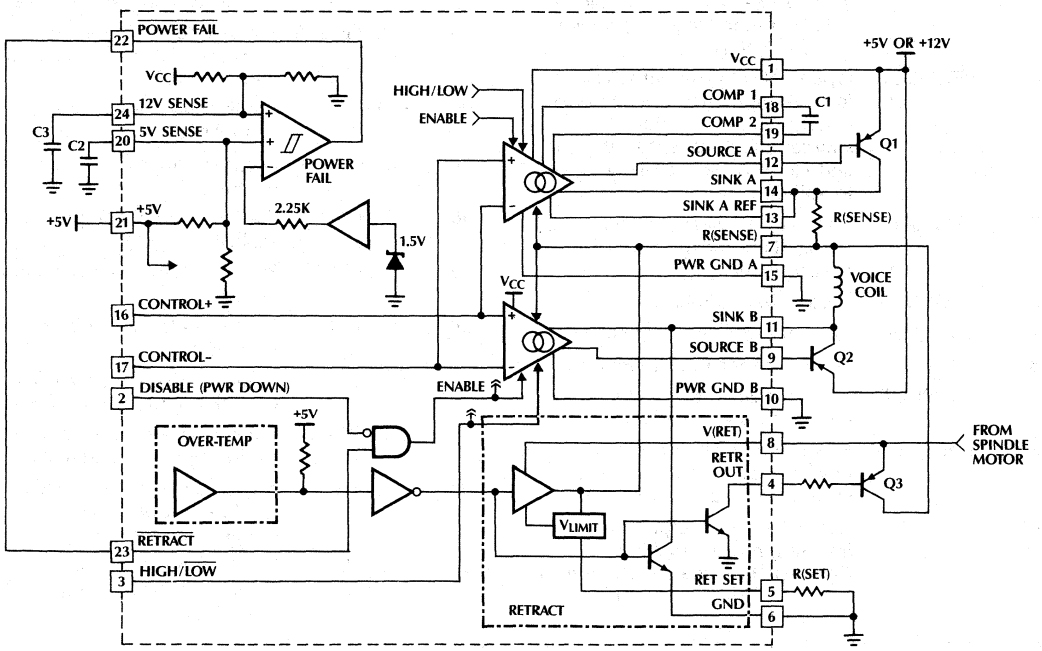
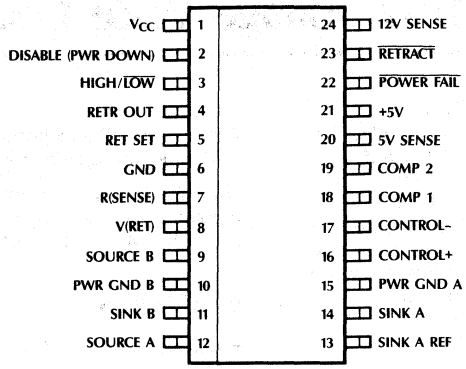
BLOCK DIAGRAM



PIN CONFIGURATION

ML4408
24-Pin SOIC



TOP VIEW

PIN DESCRIPTION

PIN #	NAME	FUNCTION
1	V_{CC}	Supply input to power amplifiers.
2	DISABLE (PWR DOWN)	A Logic "1" puts the IC into a low power state and disables the power amplifiers.
3	HIGH/LOW	A logic "1" sets the transconductance gain to 1/4 while a logic "0" sets the gain to 1/24. Transconductance gain is the $V_{RSENSE} \div V_{CONTROL}$.
4	RETR OUT	Open collector output which pulls low during retract. Used to drive external power transistor to source retract current to the coil and can provide a braking signal to spindle.
5	RET SET	External set resistor to establish a voltage limit for the internal retract driver.
6	GND	Analog signal ground.
7	R(SENSE)	Current sense resistor terminal.
8	V(RET)	Supply pin for retract circuits.
9	SOURCE B	PNP Base drive output for inverting power amplifier.
10	PWR GND B	Power return pin for inverting power amplifier. Normally used for current sensing.
11	SINK B	Current sinking output for inverting power amplifier. Connects to voice coil (–) terminal.
12	SOURCE A	PNP Base drive output for non-inverting power amplifier.
13	SINK A REF	Kelvin sensing point for power amplifier. Connect to SINK A.
14	SINK A	Current sinking output for non-inverting power amplifier. Connects to voice coil (+) terminal.
15	PWR GND A	Power return pin for non-inverting power amplifier. Normally used for current sensing.
16	CONTROL+	Positive input for current command.
17	CONTROL–	Negative input for current command.
18	COMP 1	Pin for external compensation capacitor.
19	COMP 2	Pin for external compensation capacitor.
20	5V SENSE	Center node of a resistor divider from +5V.
21	+5V	Input for +5V for power fail detection and logic power supply.
22	POWER FAIL	Open Collector output drives low for low voltage conditions.
23	RETRACT	A logic "0" initiates retract. Also used as an open-collector over-temperature output flag.
24	12V SENSE	Input to the power fail comparator from a resistor divider from V_{CC}.

Micro Linear

ML4410

Sensorless Spindle Motor Controller

GENERAL DESCRIPTION

The ML4410 provides complete commutation for delta or wye wound Brushless DC (BLDC) motors without the need for signals from Hall Effect sensors. This IC senses the back EMF of the 3 motor windings (no neutral required) to determine the proper commutation phase angle using phase lock loop techniques. This technique will commutate virtually any 3-phase BLDC motor and is insensitive to PWM noise and motor snubbing.

Included in the ML4410 is the circuitry necessary for a Hard Disk Drive microcontroller driven control loop. The ML4410 controls motor current with either a constant off-time PWM or linear current control driven by the microcontroller. Speed feedback for the micro is a stable digital frequency equal to the commutation frequency of the motor. All commutation is performed by the ML4410. Braking and Power Fail are also included in the ML4410.

Two different start-up sequencing (minimum start-up time or minimum reverse rotation at start up) algorithms are supported by the ML4410. Since the timing of the start-up sequencing is determined by the micro, the system can be optimized for a wide range of motors and inertial loads.

The ML4410 modulates the gates of external N-channel power MOSFETs to regulate the motor current. The IC drives external PNP transistors or P-channel MOSFETs directly. Special circuits are used to save base drive power at low load currents.

FEATURES

- Back-EMF Commutation Provides Maximum Torque for Minimum "Spin-Up" Time for Spindle Motors
- Accurate, Jitter-Free Phase Locked Motor Speed Feedback Output
- Linear or PWM Motor Current Control
- Easy Microcontroller Interface for Optimized Start-Up Sequencing and Speed Control
- Power Fail Detect Circuit with Delayed Braking
- Drives External N-Channel FETs and PNP's or P-Channel FETs

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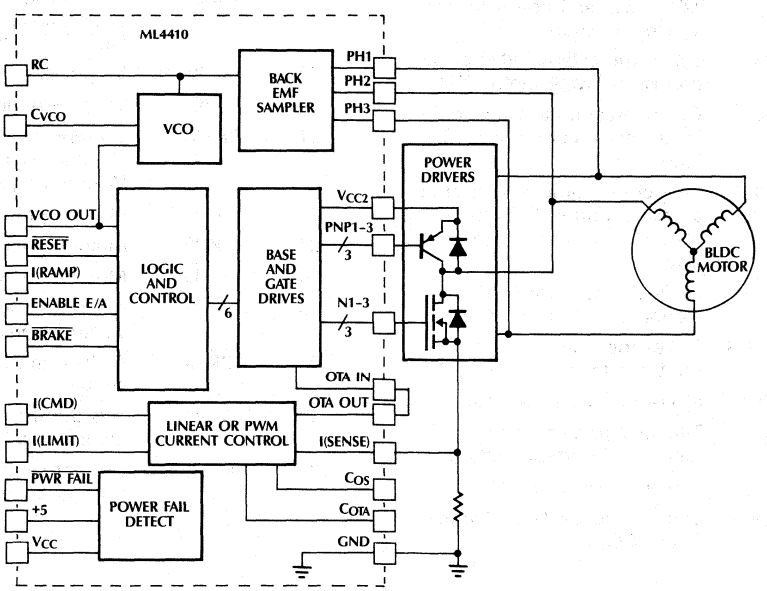
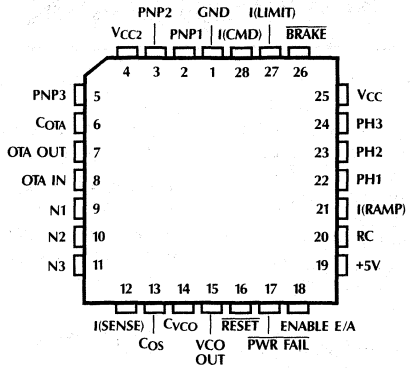
BLOCK DIAGRAM



PIN CONFIGURATION

ML4410
28-Pin PCC



TOP VIEW

PIN DESCRIPTION

PIN #	NAME	FUNCTION
1	GND	Signal and Power Ground.
2	PNP1	Drives the external PNP power transistor driving motor PH1.
3	PNP2	Drives the external PNP power transistor driving motor PH2.
4	V_{CC2}	12V power and power for the braking function.
5	PNP3	Drives the external PNP power transistor driving motor PH3.
6	C_{OTA}	Compensation capacitor for linear motor current amplifier loop.
7	OTA OUT	Output of motor current error amplifier, normally connected to OTA IN or to external MOSFET gate.
8	OTA IN	Driving voltage for N1–N3. Normally tied to OTA OUT.
9–11	N1, N2, N3	Drives the external N-channel MOSFETs for PH1, PH2, PH3.
12	I(SENSE)	Motor current sense input.
13	C_{OS}	Timing capacitor for fixed off-time PWM current control.
14	C_{VCO}	Timing capacitor for VCO.
15	VCO OUT	Open Collector Logic Output from VCO.
16	$\overline{\text{RESET}}$	Input which holds the VCO off and sets the ML4410 to the RESET condition.
17	$\overline{\text{PWR FAIL}}$	A "0" output indicates 5V or 12V is under-voltage.
18	ENABLE E/A	A "1" logic input enables the error amplifier and closes the back-EMF feedback loop.
19	+5V	5V power supply input.
20	RC	VCO loop filter components.
21	I(RAMP)	Current into this pin sets the initial acceleration rate of the VCO during start-up.
22	PH1	Motor Terminal 1.
23	PH2	Motor Terminal 2.
24	PH3	Motor Terminal 3.
25	V_{CC}	12V power supply. Terminal which is sensed for power fail.
26	$\overline{\text{BRAKE}}$	A "0" activates the braking circuit.
27	I(LIMIT)	Sets the threshold for the PWM comparator.
28	I(CMD)	Current Command for Linear Current amplifier.

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

Supply Voltage (pins 4, 25) 14V
Output Current (pins 2, 3, 5, 9, 10, 11) ..... ±150mA
Logic Inputs (pins 16, 17, 18, 26) ..... -0.3 to 7V
Junction Temperature ..... 150°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering 10 sec) ..... 150°C
Thermal Resistance (θ_{JA}) ..... 60°C/W

OPERATING CONDITIONS

Temperature Range ..... 0°C to +70°C
V_{CC} Voltage +12V (pin 25) ..... 12V ± 10%
+5V (pin 19) ..... 5V ± 10%
I(RAMP) Current (pin 21) ..... 0 to 100μA
I Control Voltage Range (pins 27, 28) ..... 0V to 7V

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, T_A = Operating Temperature Range, $V_{CC} = V_{CC2}$ = 12V, R_{SENSE} = 1Ω, $C_{OTA} = C_{VCO}$ = .01μF, C_{OS} = .02μF

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Oscillator (VCO) Section (Mode 1 or 2 unless otherwise specified)					
Frequency vs. $V_{PIN\ 20}$	$1V \leq V_{PIN\ 20} \leq 10V$		300		Hz/V
Frequency	V_{VCO} = 6V	1200	1800	2400	Hz
	V_{VCO} = .5V	70	140	210	Hz
Reset Voltage at C_{VCO}	Mode = 0		125	250	mV
Sampling Amplifier					
V_{RC}	Mode 0		125	250	mV
I_{RC}	Mode 1, R_{RAMP} = 39KΩ	70	100	130	μA
	Mode 2A, V_{PH2} = 4V	30	50	70	μA
	Mode 2A, V_{PH2} = 6V	-15	2	+15	μA
	Mode 2A, V_{PH2} = 8V	-30	-50	-70	μA
Motor Current Control Section					
I(SENSE) Gain	$V_{PIN\ 27}$ = 5V, $0V \leq V_{PIN\ 28} \leq 2.5V$	TBD	5	TBD	V/V
One Shot Off Time		12	25	33	μs
I(CMD) Transconductance Gain			.19		mmho
Power Fail Detection Circuit					
12V Threshold		9.1	9.8	10.5	V
Hysteresis			150		mV
5V Threshold		3.8	4.25	4.5	V
Hysteresis			70		mV
Logic Inputs					
Voltage High (V_{IH})		2			V
Voltage Low (V_{IL})				.8	V
Current High (I_{IH})	V_{IN} = 2.7V	-10	1	10	μA
Current Low (I_{IL})	V_{IN} = 0.4V	-500	-350	-200	μA

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ELECTRICAL CHARACTERISTICS (Continued)

Unless otherwise specified, T_A = Operating Temperature Range, V_{CC} = V_{CC2} = 12V, R_{SENSE} = 1Ω, C_{OTA} = C_{VCO} = .01μF, C_{OS} = .02μF

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Outputs	I(CMD) = I(LIMIT) = 2.5V				
I_{PNP} Low		50	75	100	mA
I_{PNP} High	Off State	-100		100	μA
V_N High	$V_{PIN\ 8}$ = 10V	9.7	10	10.3	V
V_N Low			.2	.7	V
A_V Pin 8 to V_N	$V_{PIN\ 8}$ = 6V	.95	1	1.05	V/V
LOGIC Low	I_{OUT} = 0.5mA			.4	V
LOGIC I_{OUT} High			5		μA
Supply Currents	(N and PNP Outputs Open)				
5V Current			2	4	mA
V_{CC} Current			38	50	mA
V_{CC2} Current			4	10	mA

FUNCTIONAL DESCRIPTION

The ML4410 provides closed-loop commutation for 3-phase brushless motors. To accomplish this task, a VCO, Integrating Back-EMF Sampling error amplifier and sequencer form a phase-locked loop, locking the VCO to the back-EMF of the motor. The IC also contains circuitry to control motor current with either linear or constant off-time PWM modes. Braking and power fail detection functions are also provided on chip. The ML4410 is designed to drive external power transistors (N-channel MOSFET sinking transistors and PNP sourcing transistors) directly, and contains a special circuit to reduce PNP base currents when output current demand is reduced.

Start-up sequencing and motor speed control are accomplished by a microcontroller. Speed sensing is accomplished by monitoring the output of the VCO, which will be a signal which is phased-locked to the commutation frequency of the motor.

START-UP SEQUENCING

When the motor is initially at rest, it is generating no back-EMF. Because a back-EMF signal is required for closed loop commutation, the motor must be started "open-loop" until a velocity sufficient to generate some back-EMF is attained (around 100 RPM).

Two modes are possible for starting the motor. For the lowest possible starting time, the chip is held in the reset (mode R) state by holding pin 16 low and providing full current to the motor (figure 1a).

Step	Pin 16	Pin 18	Pin 21	I(LIMIT) I(CMD)
1	0	0	Fixed	I_{MAX}
2	1	0	Fixed	I_{MAX}
3	1	1	0	I_{MAX}

Figure 1a. Minimum Time Start-Up Sequence

Step 1: The IC is held in reset (mode R) with full power applied to the windings (see figure 4). This aligns the rotor to a position which is 30° (electrical) before the center of the first commutation state.

Step 2: A fixed current is input to pin 21 and appears as a current on pin 20, and will accelerate the motor at a fixed rate.

Step 3: When the motor speed reaches about 100 RPM, the back-EMF loop can be closed by pulling pin 18 low.

Using this technique, some reverse rotation is possible. The maximum amount of reverse rotation is 360/N, where N is the number of poles. For an 8 pole motor, 45° reverse rotation is possible.

The second technique minimizes inital reverse rotation, at the expense of spin-up time. This technique (figure 1b) establishes a fixed low-frequency rotation on the motor and slowly ramps the current to the motor.

Step 1: Reset is held low briefly (10μs) to initialize the internal logic.

Step	Pin 16	Pin 18	Pin 21	I(LIMIT) I(CMD)
1	0	0	X	0
2	1	0	1	0
3	1	0	0	RAMP to I_{MAX}
4	1	0	1	I_{MAX}
5	1	1	0	I_{MAX}

Figure 1b. Minimum Reverse Rotation Start-Up Sequence

Step 2: A low frequency rotational field is established with 0 current commanded. To establish the low frequency, inject a current (via a resistor connected to the microcontroller output port) into pin 21 and monitor the VCO OUT (pin 15) frequency.

Step 3: When the desired frequency is reached, set the current into pin 21 to 0, and begin to ramp the motor current by slowly increasing the current command (pins 27 or 28).

Step 4: After full current is reached, inject some current into pin 21 to increase the frequency.

Step 5: The back-EMF feedback loop can then be closed when the motor speed is sufficient.

Some small amount of reverse rotation is still possible with this starting method.

SPEED CONTROL — CURRENT LOOP

To facilitate speed control, the ML4410 includes two current control loops — linear and PWM (figure 2). The linear control loop senses the motor current on the I(SENSE) terminal through R_{SENSE}. An internal current sense amplifier's output modulates the gates of the 3 N-channel MOSFET's when OTA OUT is tied to OTA IN, or can modulate a single MOSFET gate to control current.

The ML4410 also includes a current mode constant off-time PWM circuit. When motor current builds to the threshold set on I(LIMIT) input (pin 27), a one-shot is fired whose timing is set by C_{OS}. The current in the motor will be controlled by the lower of pin 27 and pin 28.

The motor's source transistor drivers are open-collector NPN's with internal 50KΩ pull-up resistors, whose current is controlled according to the current demanded through the motor. To conserve power, the ML4410 sets the current to PNP1, PNP2, and PNP3, proportional to the lower of pin 27 and pin 28.

Drivers N1 through N3 are totem-pole outputs capable of sourcing and sinking 10mA. Switching noise in the external MOSFETs can be reduced by adding resistance in series with the gates.

BRAKING

Applying a 0 on pin 26 activates the braking circuit. The brake circuit turns on PNP1 through PNP3 and turns off NPN1 through NPN3.

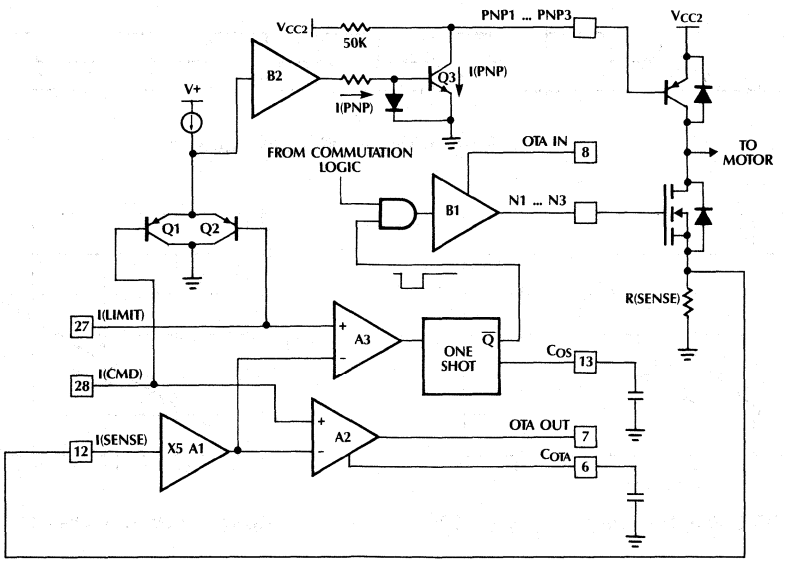


Figure 2. Current Control and Output Drive

BACK-EMF SENSING AND COMMUTATOR

The ML4410 contains a patented back-EMF sensing circuit which samples the phase which is not energized to determine whether to increase or decrease the commutator (VCO) frequency. A late commutation causes the error amplifier to charge the integrator (RC) on pin 20, increasing the VCO input while early commutation causes pin 20 to discharge. C1 and R1 provide the basic integration time constant for the motor/commutator phase lock loop while C2 is a noise filter. Larger inertial loads will require larger values of R1 and C1. These values are best determined empirically. Analog speed control loops can use pin 20 as a speed feedback voltage.

STATE	OUTPUTS						INPUT SAMPLING
	N1	N2	N3	PNP1	PNP2	PNP3	
R or 0	OFF	ON	OFF	ON	OFF	ON	N/A
A	OFF	OFF	ON	ON	OFF	OFF	PH2
B	OFF	OFF	ON	OFF	ON	OFF	PH1
C	ON	OFF	OFF	OFF	ON	OFF	PH3
D	ON	OFF	OFF	OFF	OFF	ON	PH2
E	OFF	ON	OFF	OFF	OFF	ON	PH1
F	OFF	ON	OFF	ON	OFF	OFF	PH3

Figure 3. Commutation State Table

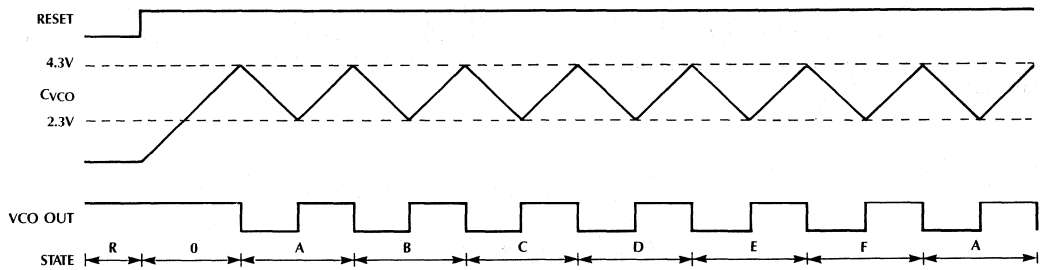


Figure 4. Start-Up Timing and Mode Sequencing

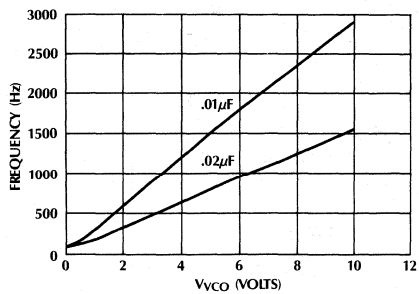


Figure 5. VCO Output Frequency vs V_{VCO} (pin 20)

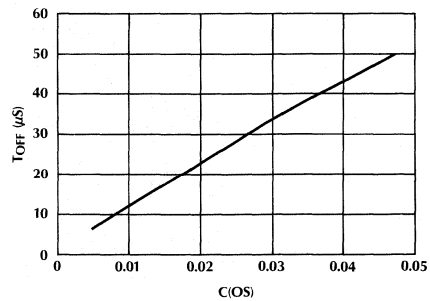


Figure 6. I(LIMIT) Output Off-Time vs C_{OS}

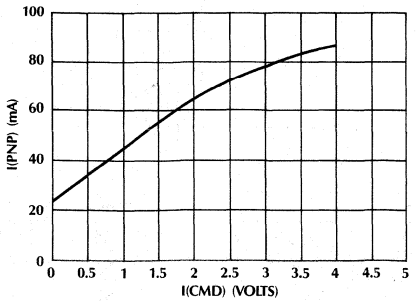


Figure 7. Available PNP Drive Current vs I(CMD) Input

APPLICATIONS

Figure 8 shows a typical application of the ML4410 in a hard disk drive spindle control. Although the timing necessary to start the motor in most applications would be generated by a microcontroller, Figure 9 shows a simple "one shot" start-up timing approach.

Speed control can be accomplished either by:

1. Sensing the VCO OUT frequency with a Microcontroller and adjusting I(CMD) via an analog output from the Micro (PWM DAC).
2. Using analog circuitry for speed control (Figure 10).

Q1, Q2, and Q3 are MJE210 or equivalent. Q4, Q5, and Q6 are IRFU010 or equivalent. Base resistors (100Ω) are included to reduce power dissipation in the IC during start-up. If requested currents are low, these can be eliminated. Switching transients due to commutation can be reduced by increasing the 470Ω gate resistors on Q4–Q6.

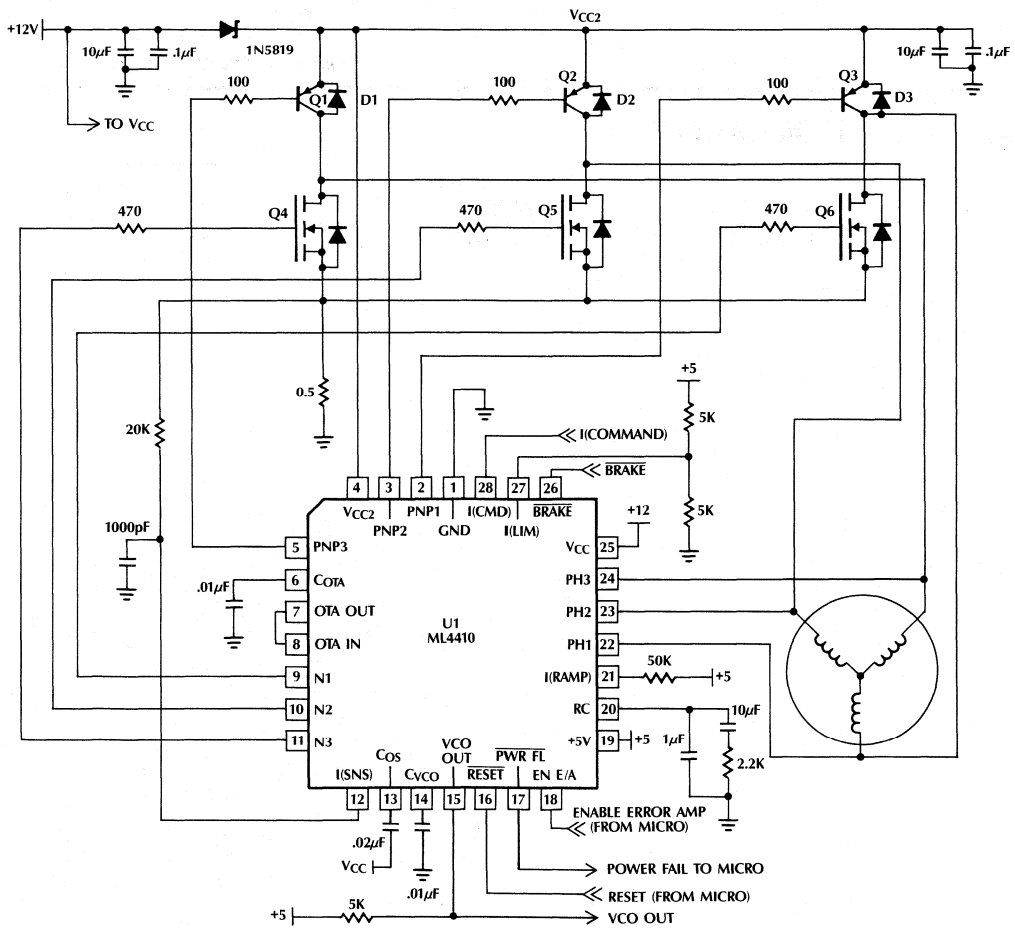


Figure 8. ML4410 Typical Application

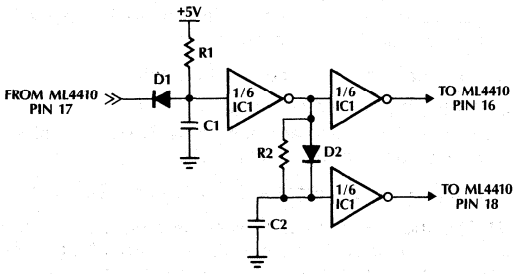
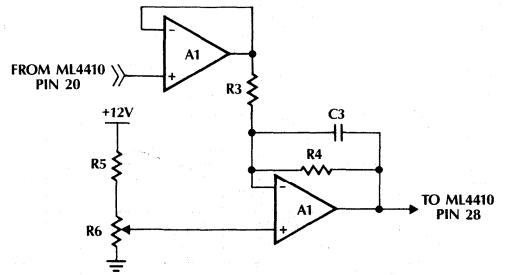


Figure 9. Analog Start-Up Circuit



Symbol	Value
A1	LM358
Q1	74HC14
D1, D2	1N4148
R1	1MΩ
R2	1MΩ
R3	100KΩ

Symbol	Value
R4	100KΩ
R5	50KΩ
R6	50KΩ
C1	3.3μF
C2	3.3μF
C3	.47μF

Figure 10. Analog Speed Control

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ML4410CQ	0°C to +70°C	28-Pin Molded PCC

Micro Linear

ML4415, ML4415R
ML4416, ML4416R

15 Channel Read/Write Circuit

GENERAL DESCRIPTION

The ML4415, ML4416 devices are bipolar monolithic read/write circuits designed for use with fixed disk ferrite center-tapped recording heads. They provide a low noise read path, write current control, and data protection circuitry for all channels.

These multiplexed read/write data channels exhibit features not found in similar read/write circuits such as improved write current stability and elimination of write current "glitches" during power up.

The ML4416 has fourteen read/write data channels and a chip select pin. The chip select pin allows additional read/write circuits in the system by enabling or disabling a particular chip. The ML4415 has fifteen read/write data channels and no chip select pin.

The ML4415R and ML4416R versions include on-chip damping resistors.

FEATURES

- Write current disable during power up
- Enhanced write current stability
- Designed for center-tapped ferrite heads
- ML4415 provides 15 read/write channels
- ML4416 — easily multiplexed for larger systems
- Includes write unsafe detection
- TTL compatible control signals
- Programmable write current source
- +5V, +12V power supplies

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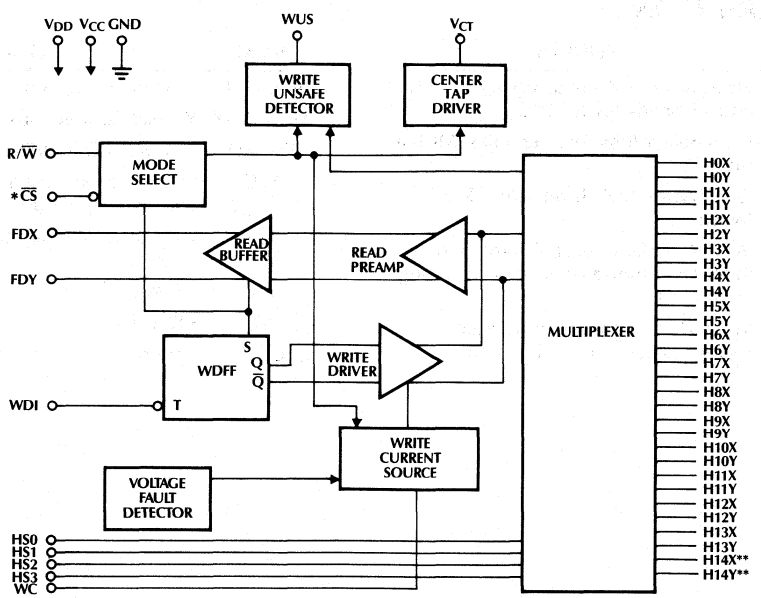
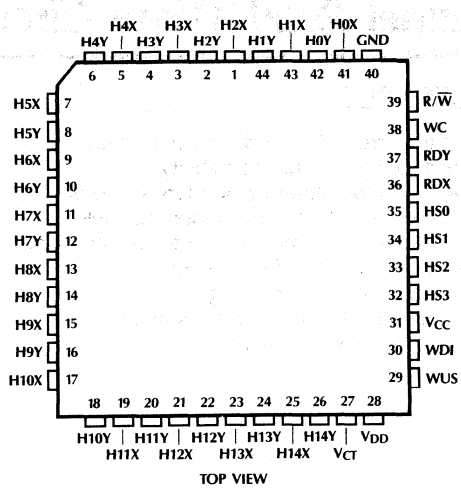
BLOCK DIAGRAM



* ML4416 ONLY
** ML4415 ONLY

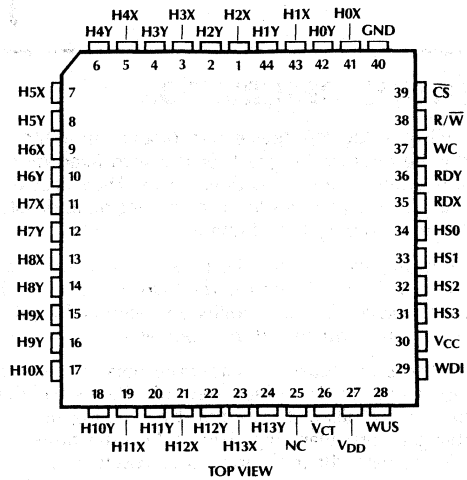
PIN CONNECTIONS

ML4415CQ, ML4415RCQ
44-Pin PCC



TOP VIEW

ML4416CQ, ML4416RCQ
44-Pin PCC



TOP VIEW

PIN DESCRIPTION

NAME	FUNCTION
HS0–HS3	Head Select (14 heads for the ML4416, and 15 heads for ML4415).
$\overline{CS}$	Chip Select (low level enables, ML4416 only)
R/W	Read/Write (high level select Read Mode)
WUS	Write Unsafe, open collector output (high level indicates an unsafe writing condition)
WDI	Write Data In (negative transition toggles head current direction)

NAME	FUNCTION
H0X–H14X	X head connections
H0Y–H14Y	Y head connections
RDX, RDY	X, Y Read Data (differential read signal out)
WC	Write Current (used to set the write current magnitude)
V_{CT}	Voltage Center Tap (center tap voltage source)
V_{CC}	+5 volts
V_{DD}	+12 volts
GND	Ground

ABSOLUTE MAXIMUM RATINGS

(Note 1)

Power Supply Voltage Range
- $V_{DD}1$ ..... −0.3 to 14 V_{DC}
- $V_{DD}2$ ..... −0.3 to 14 V_{DC}
- V_{CC} ..... −0.3 to 6 V_{DC}

Input Voltage Range
- Digital Inputs ($\overline{CS}$, R/$\overline{W}$, HS, WDI) ... −0.3 to V_{CC} +0.3 V_{DC}
- Head Ports ..... −0.3 to $V_{DD}1$ +0.3 V_{DC}
- Write Unsafe (WUS) ..... −0.3 to 14 V_{DC}

Write Current (I_W) ..... 60 mA

Output Current
- Read Data (RDX, RDY) ..... −10 mA
- Center Tap Current (I_{CT}) ..... −60 mA
- Write Unsafe (WUS) ..... 12 mA

Storage Temperature ..... −65°C to 150°C

Junction Temperature (T_J) ..... 135°C

Lead Temperature (Soldering 10 sec.) ..... 300°C

OPERATING CONDITIONS

Supply Voltage
- $V_{DD}1$ ..... 12 V ± 10%
- V_{CC} ..... 5 V ± 10%

Head Inductance
- L_H ..... 5 to 15 µH

Damping Resistor (R_D, ML4415R or ML4416R) .. 500 to 2000Ω

RCT Resistor (1/4 Watt) ..... 120Ω ± 5%

Write Current (I_W) ..... 10 to 40 mA

ELECTRICAL CHARACTERISTICS

Unless otherwise specified $V_{DD}1 = V_{DD}2 = 12\,V \pm 10\%$, $V_{CC} = 5\,V \pm 10\%$, $R_{CT} = 120\,\Omega \pm 5\%$, $I_W = 40\,mA$, $0°C \leq T_A \leq 70°C$ (Notes 2 and 3).

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
DC OPERATING CHARACTERISTICS						
POWER SUPPLY						
I_{CC}	V_{CC} Supply Current	Read or Idle Mode		31	35	mA
		Write Mode		26	30	mA
I_{DD}	V_{DD} Supply Current	Read Mode		29	35	mA
		Write Mode		17 + I_W	20 + I_W	mA
		Idle Mode		17	20	mA
P_D	Power Dissipation	Read Mode		550	655	mW
		Write Mode $I_W = 40\,mA$, $R_{CT} = 0\,\Omega$		890	960	mW
		Idle Mode		378	455	mW
DIGITAL INPUTS ($\overline{CS}$, R/$\overline{W}$, HS, WDI)						
V_{IH}	High Voltage		2			V_{DC}
V_{IL}	Low Voltage				0.8	V_{DC}
I_{IH}	High Current	$V_{IH} = 2.0\,V$			100	µA
I_{IL}	Low Current	$V_{IL} = 0.8\,V$	−0.4			mA
WUS OUTPUT						
V_{OL}	Output Low Voltage	$I_{OL} = 8\,mA$ (Safe)			0.5	V_{DC}
I_{OH}	Output High Current	$V_{OH} = 5\,V$ (Unsafe)			100	µA
CENTER TAP VOLTAGES						
V_{CT}	Read Mode	Read Mode		4		V_{DC}
V_{CT}	Write Mode	Write Mode		6		V_{DC}

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ELECTRICAL CHARACTERISTICS (Continued)

Unless otherwise specified $V_{DD}1$ = 12V ± 10%, V_{CC} = 5V ± 10%, R_{CT} = 120Ω ± 5%, I_W = 35mA, L_H = 10μH, R_D = 750Ω (ML4415, ML4416), f_{DATA} = 5MHz, C_L (RDX, RDY) ≤ 20pF, 0°C ≤ T_A ≤ 70°C (Notes 2 and 3) (V_{IN} is referenced to V_{CT} for Read Mode Characteristics).

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
WRITE MODE CHARACTERISTICS						
I_{HCW}	Head Current (per side)	Write Mode $0 \leq V_{CC} \leq 3.7V$ $0 \leq V_{DD}1 \leq 8.7V$	−200	0.15	200	μA
I_{WR}	Write Current Range	$I_W = K/R_{WC}$	10		40	mA
K	Write Current Constant		2.375	2.5	2.625	
V_{HD}	Differential Head Voltage Swing		7.0	10.2		V_{PK}
I_{HU}	Unselected Head Transient Current				2	mA_{PK}
C_{OD}	Differential Output Capacitance			8.8	15	pF
R_{OD}	Differential Output Resistance	ML4415, 4416	10k			Ω
		T_J = 25°C ML4415R, 4416R	600		960	Ω
f_{WDI}	WDI Transition Frequency	WUS = Low	250	490		kHz
A_I	I_{WC} to Head Current Gain			0.99		mA/mA
I_L	Unselected Head Leakage	Sum of X & Y Side Leakage Current			85	μA
READ MODE CHARACTERISTICS						
A_V	Differential Voltage Gain	$V_{IN} = 1mV_{P-P}$ @ 300kHz, R_L (RDX, RDY) = 1kΩ	85	106	115	V/V
DR	Dynamic Range	DC Input Voltage (V_I) Where Gain Falls 10%, $V_{IN} = V_I + 0.5mV_{P-P}$ @ 300kHz	−3	±7	+3	mV
BW	Bandwidth (−3dB)	$\|Z_S\| < 5Ω, V_{IN} = 1mV_{P-P}$	30	40		MHz
e_{IN}	Input Noise Voltage	BW = 15MHz, L_H = 0, R_H = 0		1.2	1.5	nV/ $\sqrt{Hz}$
C_{IN}	Differential Input Capacitance	f = 5MHz		14	20	pF
R_{IN}	Differential Input Resistance	f = 5MHz, T_J = 25°C ML4415, 4416	2k	15K		Ω
		V_{IN} = $6mV_{P-P}$ ML4415R, 4416R	460		860	Ω
I_{HCR}	Head Current (per side)	Read or Idle Mode $0 \leq V_{CC} \leq 5.5V$ $0 \leq V_{DD}1 \leq 13.2V$	−200		200	μA
I_{IN}	Input Bias Current (1 side)			8.5	45	μA
CMRR	Common-Mode Rejection Ratio	$V_{CM} = V_{CT} + 100mV_{P-P}$ @ f = 5MHz	50	77		dB
PSRR	Power Supply Rejection Ratio	$100mV_{P-P}$ @ 5MHz on $V_{DD}1$, $V_{DD}2$, or V_{CC}	45			dB
CS	Channel Separation	Unselected Channels: $V_{IN} = 100mV_{P-P}$ @ 5MHz and Selected Channel: $V_{IN} = 0mV_{P-P}$	45	57		dB
V_{OS}	Output Offset Voltage	Read Mode	−460	±29	+460	mV
		Write or Idle Mode	−20	±1	+20	mV
V_{OCM}	Common-Mode Output Voltage	Read Mode	4.5	5.5	6.5	V
		Write or Idle Mode		5.6		V
R_{OUT}	Single-Ended Output Resistance	f = 5MHz			30	Ω
I_L	Leakage Current, RDX, RDY	(RDX, RDY) = 6V Write or Idle Mode	−100	±15	100	μA
I_O	Output Current	AC Coupled Load, RDX to RDY	±2.1	±2.7		mA

ELECTRICAL CHARACTERISTICS (Continued)

Unless otherwise specified $V_{DD}1$ = 12V ± 10%, V_{CC} = 5V ± 10%, R_{CT} = 120Ω ± 5%, I_W = 35mA, L_H = 10μH, R_D = 750Ω (ML4415, ML4416), f_{DATA} = 5MHz, 0°C ≤ T_A ≤ 70°C (Notes 2 and 3)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
SWITCHING CHARACTERISTICS						
t_{RW}	R/$\overline{W}$ to Write Switching Delay	To 90% of Write Current Output		.105	1	μs
t_{WR}	R/$\overline{W}$ to Read Switching Delay	To 90% of 100mV, 10MHz Read Signal Envelope or to 90% Decay of Write Current		.036	1	μs
t_{IW} or t_{IR}	$\overline{CS}$ to Select Switching Delay	To 90% of Write Current or to 90% of 100mV, 10MHz Read Signal Envelope		.165	1	μs
t_{WI} or t_{RI}	$\overline{CS}$ to Unselect Switching Delay	To 90% Decay of 100mV, 10MHz Read Signal Envelope or to 90% Decay of Write Current		.084	1	μs
t_{HS}	Head Select Switching Delay	To 90% of 100mV, 10MHz Read Signal Envelope		.045	1	μs
tD1	Safe to Unsafe Write Unsafe Delay	I_W = 35mA	1.6	3.9	8	us
tD2	Unsafe to Safe Write Unsafe Delay	I_W = 35mA		.387	1	us
tD3	Prop. Delay Head Current	L_H = 0, R_H = 0 From 50% points		23	25	ns
	Asymmetry Head Current	WDI has 50% Duty Cycle and 1nS Rise/Fall Time		0.9	2	ns
	Rise/Fall Head Current	10% and 90% Points		5	20	ns

Note 1: Absolute maximum ratings are limits beyond which the life of the integrated circuit may be impaired. All voltages unless otherwise specified are measured with respect to ground.

Note 2: Limits are guaranteed by 100% testing, sampling, or correlation with worst-case test conditions.

Note 3: Maximum junction temperature (T_J) should not exceed 135°C.

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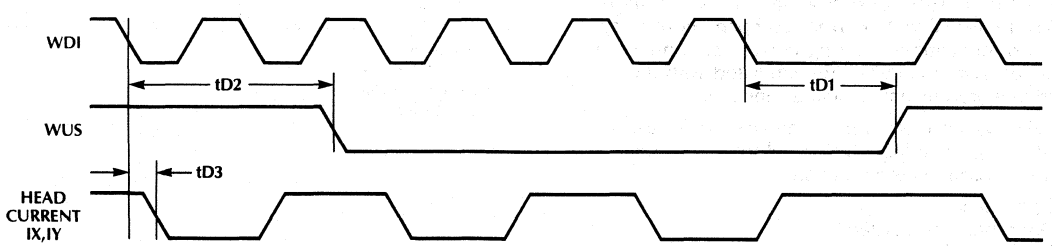
TIMING DIAGRAM



Write Mode Timing Diagram

FUNCTIONAL DESCRIPTION

CIRCUIT OPERATION

For any selected head, the ML4415/4416 functions as a read amplifier when in the Read mode, or as a write current switch when in the Write mode. Pins HS0, HS1 and HS2 determine head selection while pin R/W controls the Read/Write mode. A detected "write-unsafe" condition is indicated by pin WUS.

READ MODE

When the ML4415, 4416 is in the Read Mode, it operates as a low-noise differential amplifier on the selected channel. In Read mode the write data flip-flop is set and both the write unsafe detector and the write current source are deactivated. The center tap voltage is also lowered. Pins RDX and RDY provide differential emitter follower outputs which are in phase with the X and Y head input pins.

Note that during the Read or Chip Deselect mode the internal write current is deactivated, thus making external write current gating unnecessary.

WRITE MODE

The ML4415, 4416 operates as a write-current switch when in the Write mode. Write current magnitude is determined by the following relationship:

$I_W = K/R_{WC}$

Where: K = Write Current Constant

R_{WC} = Resistance connected between pin WC and GND.

The head current is toggled between the X and Y side of the selected head by a negative transition WDI (Write Data Input). When switching the ML4415, 4416 to write mode, the WDFF (Write Data Flip-Flop) is initialized to pass write current through the X-side of the head.

The ML4415, 4416 exhibit enhanced write current stability, compared to similar read/write circuits, which reduces the problem of oscillation. This is a result of increased internal write current compensation. Also, write current "glitches" during power-up, common in similar read/write circuits, are eliminated with an exclusive write current disabling function.

The WUS (Write Unsafe) pin is an open collector output that gives a logic high level for any of the following unsafe write conditions:

- Open head
- Open head center-tap
- Too low WDI frequency
- Read mode selected
- Device not selected
- No write current

Two negative transitions on WDI are required to clear WUS after the fault condition is removed.

The ML4415, 4416 also offers a voltage fault detection circuit that prevents write current during power-loss or power-up.

Table 1.

Head Select

HS3	HS2	HS1	HS0	HEAD
0	0	0	0	H0
0	0	0	1	H1
0	0	1	0	H2
0	0	1	1	H3
0	1	0	0	H4
0	1	0	1	H5
0	1	1	0	H6
0	1	1	1	H7
1	0	0	0	H8
1	0	0	1	H9
1	0	1	0	H10
1	0	1	1	H11
1	1	0	0	H12
1	1	0	1	H13
1	1	1	0	H14*

* ML4415 only
0 = Logic Level Low
1 = Logic Level High
X = Don't Care

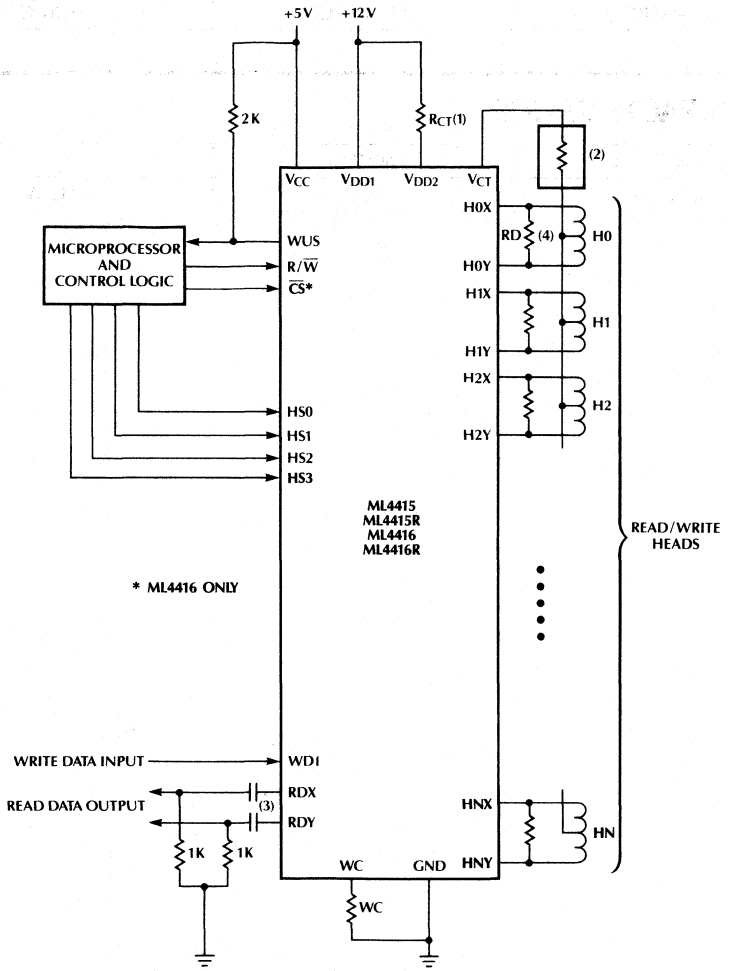
Table 2.

Mode Select

$\overline{CS}$**	R/$\overline{W}$	MODE
0	0	Write
0	1	Read
1	X	Idle

** ML4416 only
0 = Logic Level Low
1 = Logic Level High
X = Don't Care

TYPICAL APPLICATION



NOTES:

1. RCT is optional and is used to limit internal power dissipation (Otherwise connect $V_{DD}1$ to $V_{DD}2$).
   RCT (1/2 Watt) = 120 (40/I_W) ohms
   where I_W = Write Current, in mA
2. Ferrite head optional: used to suppress write current overshoot and ringing. Recommend Ferroxcube 3659065/4A6.
3. RDX and RDY load capacitance 20pF maximum. RDX and RDY output current must be limited to 100μA.
4. Damping resistors not required on ML4415R, 4416R.

ORDERING INFORMATION

PART NUMBER	PACKAGE	NUMBER OF CHANNELS
ML4415CQ	44-Lead PCC	15
ML4415RCQ	44-Lead PCC	15
ML4416CQ	44-Lead PCC	14 with $\overline{CS}$
ML4416RCQ	44-Lead PCC	14 with $\overline{CS}$

THERMAL CHARACTERISTICS

PIN COUNT	PACKAGE	θ_{JA}
44-Lead	PCC	60°C/W

Micro Linear

ML4417/ML4427

Zoned Bit Recording Circuit

GENERAL DESCRIPTION

The ML4417/27 is a bipolar monolithic integrated circuit that simplifies the design of zoned bit recording systems in hard disk drives. It contains a VCO capable of operating at frequencies up to 95 MHz, a charge pump, and the active electronics required for a loop filter to form a variable rate data encoding and decoding system.

The ML4417/27 also includes a code clock output and the dividers required for an interface clock output whose frequency is equal to the code clock output frequency divided by 1.5. This feature simplifies the use of RLL (1, 7) coding for improved storage density.

In addition, the ML4417/27 includes two uncommitted ECL to TTL level translators to simplify interfacing with TTL-based systems. The ML4417/27 is designed for operation from 12V and 5V supplies, but may be operated from a single 5V supply if desired.

The ML4417 has TTL-compatible logic input levels on the charge pump, and the ML4427 has a charge pump control input, which, when driven by a CMOS tri-state output, eliminates one logic interface line to the circuit.

FEATURES

- Wide VCO Range (3:1 Range to 95 MHz)
- Allows RLL (1, 7) or (2, 7) Encoding
- SO-16 (Narrow) Packaging
- Coarse and Fine VCO Control Inputs
- Two Uncommitted ECL to TTL Converters
- 12V, 5V or Single 5V Operation

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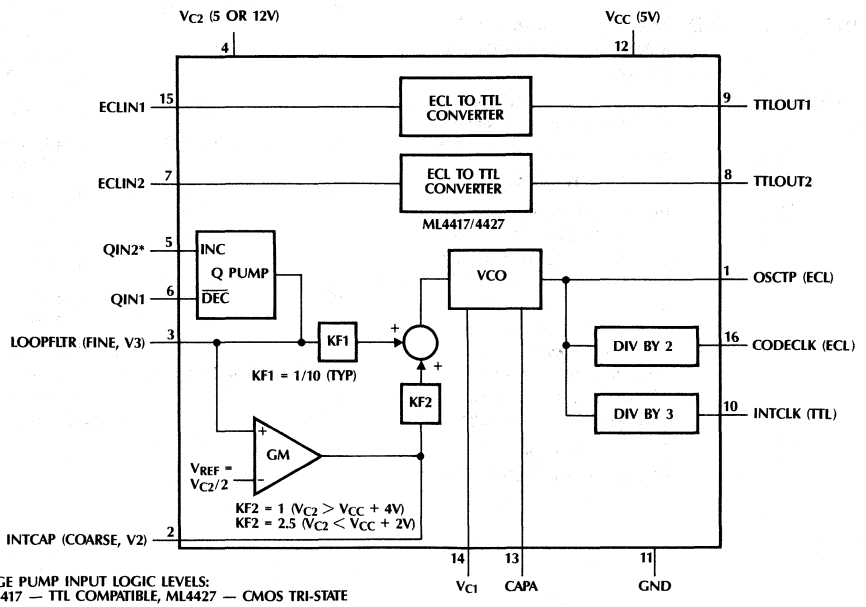
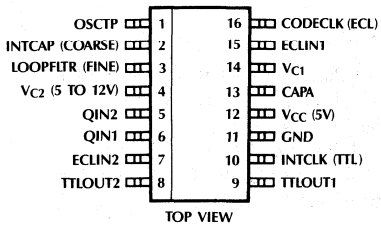
BLOCK DIAGRAM



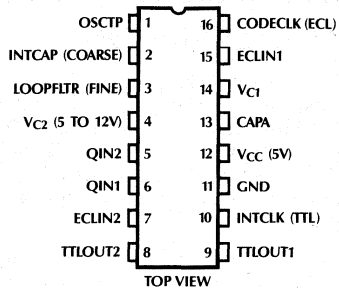
* CHARGE PUMP INPUT LOGIC LEVELS:
ML4417 — TTL COMPATIBLE, ML4427 — CMOS TRI-STATE

PIN CONNECTIONS

ML4417, ML4427
SOIC-16 (Narrow) Package



ML4417, ML4427
PDIP-16 Package
(Prototypes Only)



PIN DESCRIPTION

PIN NO.	NAME	FUNCTION
1	OSCTP (ECL)	Oscillator Test Point. An ECL output of the VCO that is useful for direct evaluation of the VCO output.
2	INTCAP (COARSE)	The coarse input for the loop filter time constant setting.
3	LOOPFLTR (FINE)	The fine input for loop filter time constant setting.
4	V_{C2}	Analog power supply input, nominal 5V or 12V.
5	QIN2	Increment input on the charge pump. This input is TTL-compatible on the ML4417. On the ML4427, it can be connected, along with pin 6, to a single CMOS tri-state output, eliminating one pin on the controlling gate array. (Active high)
6	QIN1	Decrement input on the charge pump. (Active low)
15, 7	ECLIN1, 2	ECL inputs for ECL to TTL level translators.
9, 8	TTLOUT1, 2	TTL outputs for ECL to TTL level translators.
10	INTCLK (TTL)	Interface clock output. This output is a TTL output at one third of the VCO frequency.
11	GND	Ground.
12	V_{CC} (5V)	Logic power supply input, nominally 5V.
13	CAPA	VCO capacitor connection. This capacitor determines the nominal VCO frequency.
14	V_{C1}	V_{C1} should be connected to a well-regulated 5V ± 5% supply.
16	CODECLK (ECL)	The code clock output. This is an ECL output at half the VCO frequency.

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage Range
- V_{C1} ..... –0.3 to V_{CC} + .3 VDC
- V_{C2} ..... –0.3 to 14 VDC
- V_{CC} ..... –0.3 to 6 VDC

Digital Inputs
- ECLIN1, 2 ..... –0.3 to V_{CC} + 0.3V
- QIN1, 2 ..... –0.3 to V_{CC} + 0.3V

Analog Inputs
- LOOPFLTR, INTCAP ..... –0.3 to V_{C2} + 0.3V
- CAPA ..... –0.3 to V_{C1} + 0.3V

Digital Outputs
- TTLOUT1, 2, OSCTP, CODECLK, INTCLK ..... –0.3 to V_{CC} + 0.3V

TYPICAL OPERATING CONDITIONS

Temperature Range ..... 0°C to +70°C
Analog Supply Voltage (V_{C2})* ..... 5 or 12V
Digital Supply Voltage (V_{CC}) 5V
V_{C1} 5V

* This supply voltage is designed for 5V or 12V operation. This data sheet specifies the ML4417/4427 for 12V operation. For 5V specification, please contact Micro Linear.

Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied. (All voltages are referenced to GND.)

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, V_{C2} = 12V ± 10%, V_{CC} = 5V ± 5%, V_{C1} = 5V ± 5%, T_A = 25°C.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Power Supply							
I_{CC}	V_{CC} Supply Current[1]	Pin 12			90.0		mA
I_{C1}	V_{C1} Supply Current	Pin 14			11.0		mA
I_{C2}	V_{C2} Supply Current	Pin 4			4.5		mA
Digital Inputs							
$V_{IH\ (ECL)}$	High Voltage ECL Input	Pin 15, V_{CC} = 5V		4.0			V
$V_{IL\ (ECL)}$	Low Voltage ECL Input	Pin 15, V_{CC} = 5V				3.6	V
$I_{IH\ (ECL)}$	High Current ECL Input	Pin 15, V_{CC} = 5V				1250	µA
$I_{IL\ (ECL)}$	Low Current ECL Input	Pin 15, V_{CC} = 5V		625		1000	µA
Digital Outputs (ECL are Open Emitter)							
$V_{OH\ (TTL)}$	High Voltage TTL Output	I_{OH} = –0.4mA	TTL $OUT_{1, 2, 3}$ Pins 8, 9, 10, V_{CC} = 5V	3.75			V
$V_{OL\ (TTL)}$	Low Voltage TTL Output	I_{OL} = 1.6mA				0.50	V
$V_{OH\ (ECL)}$	High Voltage ECL Output	I_{OH} = –4mA	ECL Code CLK Pin 16, V_{CC} = 5V	4.05	4.22	4.30	V
$V_{OL\ (ECL)}$	Low Voltage ECL Output	I_{OL} = –4mA		2.80	3.22	3.55	V
Voltage Controlled Oscillator (VCO) (Transfer Function Pin 2 to Pin 1 = 7.5MHz/Volt @ 10pF)							
f_{VCO}	VCO Range	C_{OSC} = 10pF Pin 14 to Pin 13 (Pin 2 = 1V to 11V, Pin 3 = 6V) (Pin 14 = V_{CC})			20–95		MHz
Charge Pump							
I_Q	Charge Pump Current	Pin 3			±125		µA
V_{QH}	Charge Pump Maximum Voltage	Pin 3			V_{C2}–1V		V
V_{QL}	Charge Pump Minimum Voltage	Pin 3			1.0		V
INC, $\overline{DEC}$ Inputs							
V_{IH}	High Voltage Input	Pin 6, V_{CC} = 5V		1.9		V_{CC}	V
V_{IL}	Low Voltage Input	Pin 6		0		0.8	V
V_{IH}	High Voltage Input	Pin 5 (ML4417), V_{CC} = 5V		1.9		V_{CC}	V
V_{IL}	Low Voltage Input	Pin 5 (ML4417)		0		0.8	V

Note 1: This value includes current consumed in 1KΩ terminating resistors from pins 1 and 16 to ground.

ELECTRICAL CHARACTERISTICS (Continued)

Unless otherwise specified, V_{C2} = 12V ± 10%, V_{CC} = 5V ± 5%, V_{C1} = 5V ± 5%, T_A = 25°C.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
INC, $\overline{DEC}$ Inputs (Continued)						
V_{IH}	High Voltage Input	Pin 5 (ML4427) see figure 2, V_{CC} = 5V	4.2		5.0	V
V_{IL}	Low Voltage Input	Pin 5 (ML4427) see figure 2, V_{CC} = 5V	0		3.1	V
I_{IH}	High Current Input	Pin 6, V_{IN} = 1.9V	–5.0		+1.0	µA
I_{IL}	Low Current Input	Pin 6, V_{IN} = 0V	–25		–1,9	µA
I_{IH}	High Current Input	Pin 5 (ML4417), V_{IN} = 5V	+30		+200	µA
I_{IL}	Low Current Input	Pin 5 (ML4417), V_{IN} = 0 → 0.9V	–25		+40	µA
I_{IH}	High Current Input	Pin 5 (ML4427), V_{IN} = 5V	+1.0		+20	µA
I_{IL}	Low Current Input	Pin 5 (ML4427), V_{IN} = 3.1V	–0.1		+7.0	µA
ECL Input 2 (Pin 7) at 25°C, 5MHz < f_{IN} < 35MHz, 40% < Duty Cycle < 60% (If Unused, Pin 7 = V_{CC})						
V_{IH}	High Voltage Input	V_{CC} = 5V	3.0	4.2	5.1	V
V_{IL}	Low Voltage Input	V_{CC} = 5V	2.5	3.4	4.6	V
V_A	Voltage Swing	V_{IH} – V_{IL}, V_{CC} = 5V	.5		2.0	V
I_{IN}	Input Current	DC Bias Value		35		µA
Transconductance Amplifier						
V_{REFI}	Inverting Input of Amplifier			$V_{C2}/2$		V
G_M	Transconductance	ΔI (Pin 2) ÷ ΔV (Pin 3)		27.5		µmho
I_{SAT}	Limiting Value of Output Current	Pin 2		±120		µA

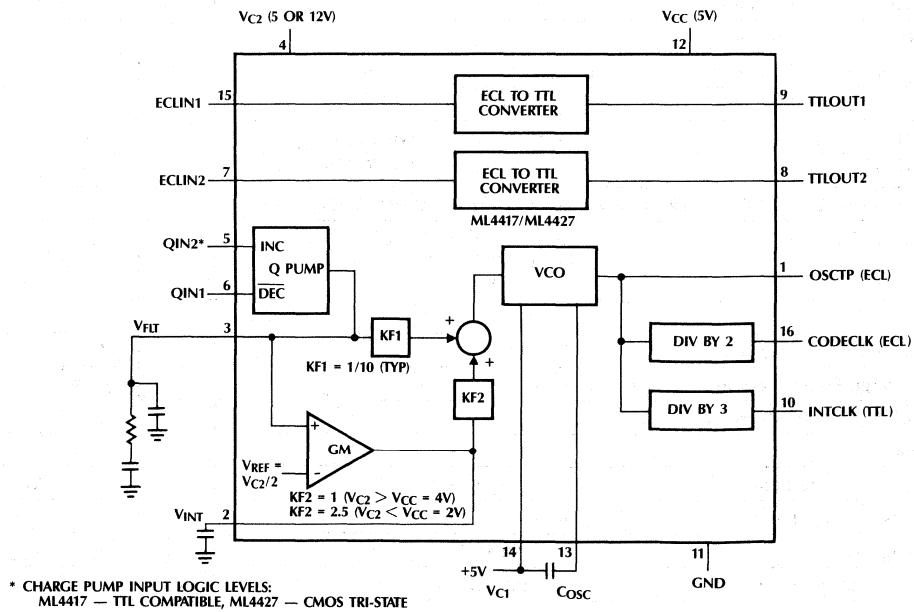


Figure 1. Typical Passive Component Connections

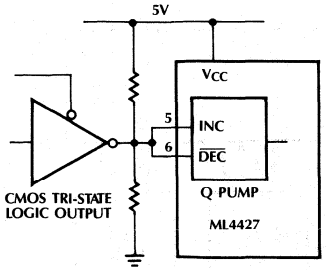


Figure 2.

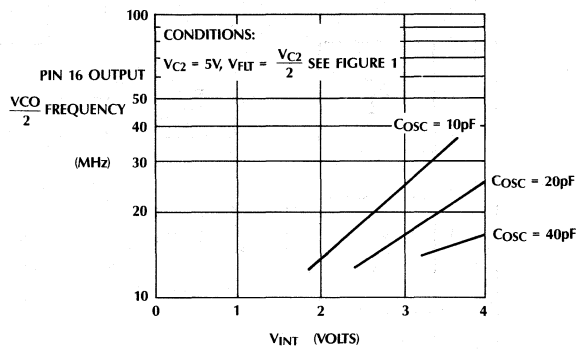
The ML4427 version has an input on pin 5 that allows a single-line control interface on the charge pump. By connecting pins 5 and 6 together, the charge pump can be controlled from a single CMOS tri-state output as follows: HI = increment, LO = decrement, tri-state = coast. The benefit is a savings of one output pin on a control gate array. A resistive termination to $V_{CC}/2$ is required to establish the logic level during tri-state, as shown.

TYPICAL PERFORMANCE CHARACTERISTICS

$\frac{VCO}{2}$ (MHz) vs. V_{INT}

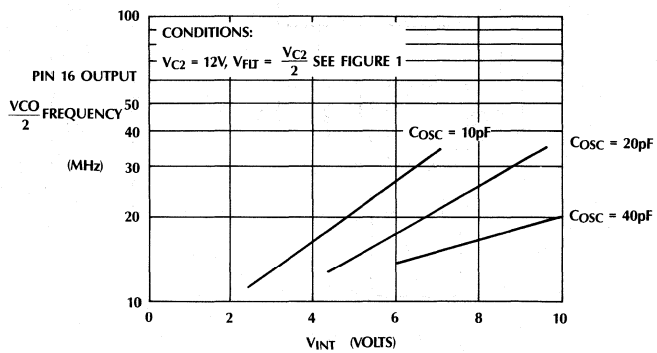
V_{C2} = 5V

(5V-Only Operation)



$\frac{VCO}{2}$ (MHz) vs. V_{INT}

V_{C2} = 12V



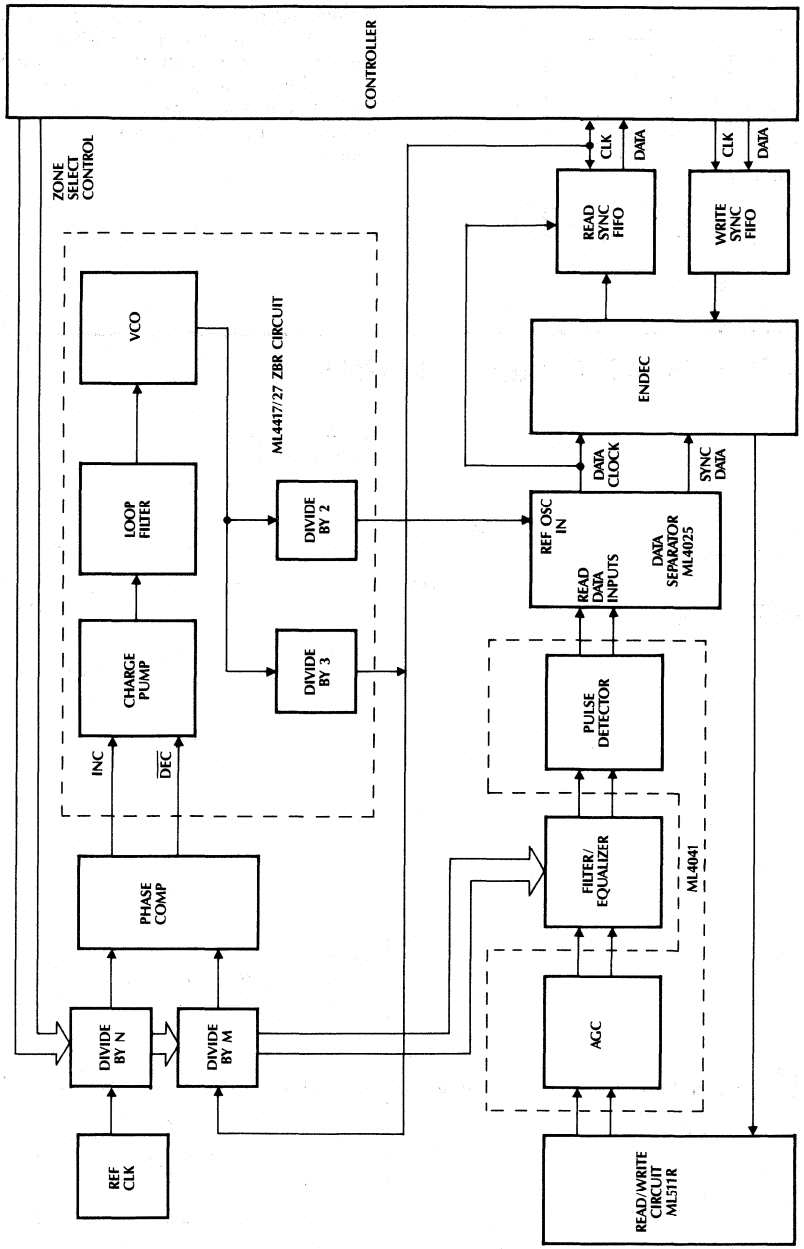


Figure 3. Read Channel Using ML4417/27 ZBR Circuit with RLL (1, 7) Encoding

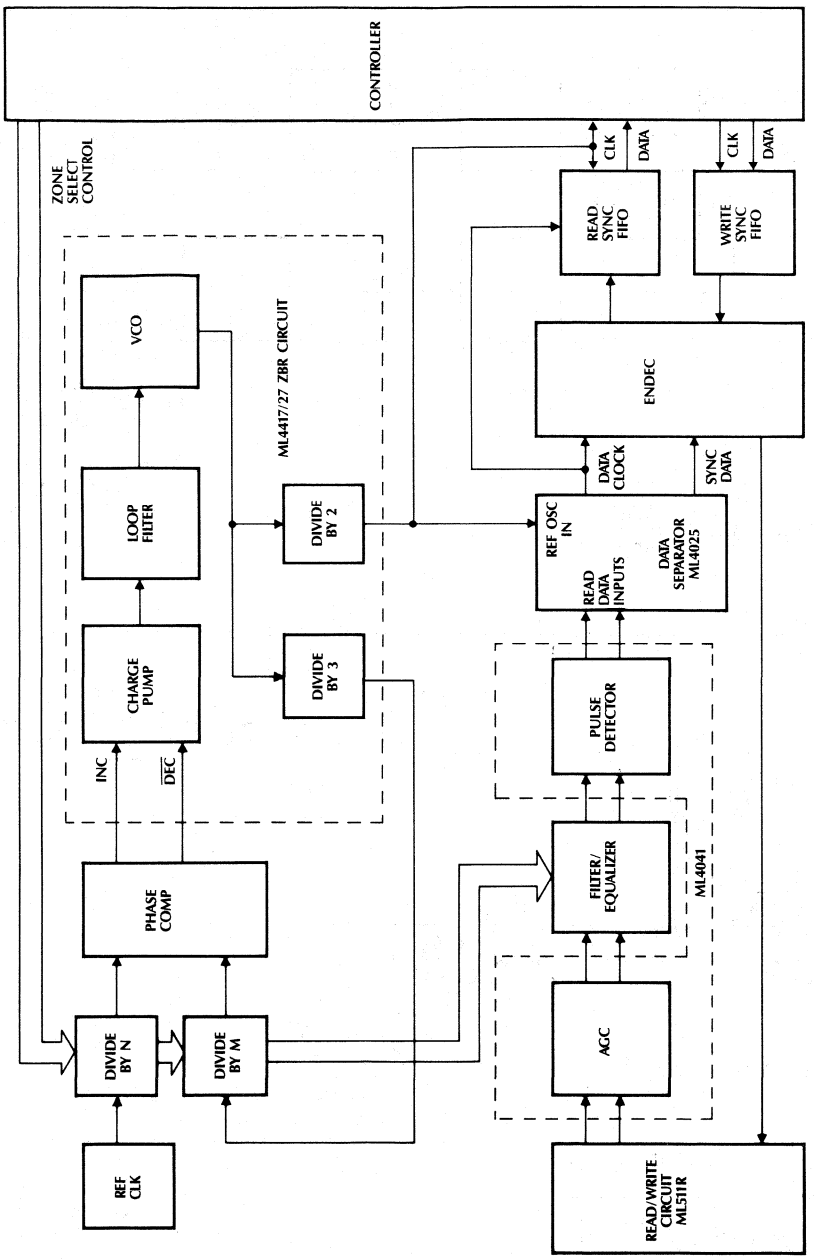
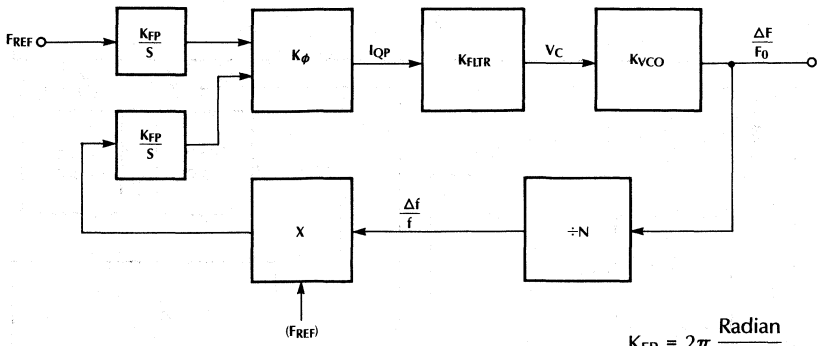


Figure 4. Read Channel Using ML4417/27 ZBR Circuit with RLL (2, 7) Encoding

4417/4427 LOOP RESPONSE

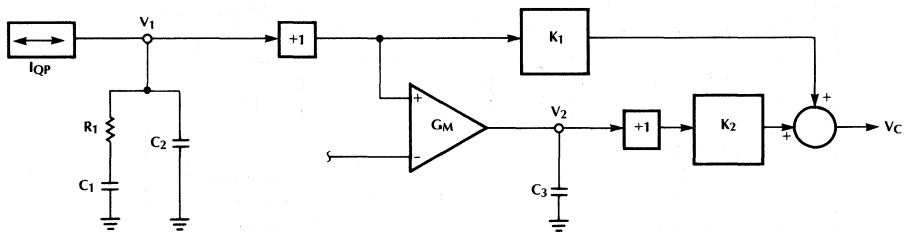


$$K_{FP} = 2\pi \frac{\text{Radian}}{\text{Hertz}}$$

$$K_{\phi} = \frac{.125\text{mA}}{2\pi} \frac{\text{Amp}}{\text{Radian}}$$

K_{FLTR} — To Be Derived, Units = $\frac{\text{Volts}}{\text{Amp}}$

$$K_{VCO} = \frac{100\%}{2.5\text{V}} \frac{\%}{\text{Volt}} \quad (C_{OSC} = 10\text{pF})$$



$$V_1 = I_{QP} * \frac{\left(R_1 + \frac{1}{SC_1}\right)\frac{1}{SC_2}}{R_1 + \frac{1}{SC_1} + \frac{1}{SC_2}} = I_{QP} * \frac{SR_1C_1 + 1}{S(C_1 + C_2)\left(SR_1\frac{C_1C_2}{C_1 + C_2} + 1\right)}$$

$$V_2 = V_1 * \frac{G_M}{SC_3},\ V_C = V_1K_1 + V_2K_2 = V_1\left(K_1 + \frac{G_MK_2}{SC_3}\right) = V_1\frac{S\frac{K_1}{K_2G_M}C_3 + 1}{S\frac{1}{G_MK_2}C_3}$$

$$\therefore \frac{V_C}{I_{QP}} = \frac{G_MK_2\,(SR_1C_1 + 1)\left(S\frac{K_1}{K_2G_M}C_3 + 1\right)}{S^2(C_1 + C_2)C_3\left(SR_1\frac{C_1C_2}{C_1 + C_2} + 1\right)}$$

$$= \frac{(SR_1C_1 + 1)\,(S * 3.6 * 10^3\,C_3 + 1)}{36 * 10^3\,S^2(C_1 + C_2)C_3\left(SR_1\frac{C_1C_2}{C_1 + C_2} + 1\right)} = K_{FLTR}$$

$$K_1 = .1\frac{V}{V}$$

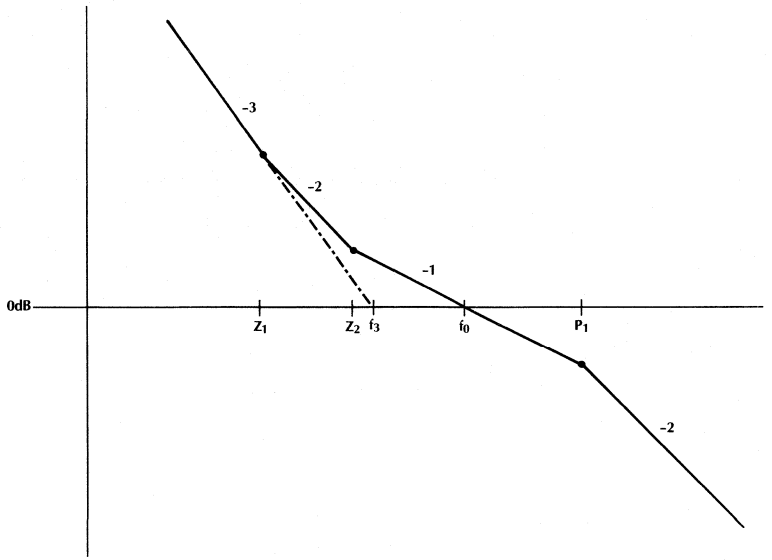
$$K_2 = 1\frac{V}{V}$$

$$G_M = 27.5 * 10^{-6}\frac{\text{Amp}}{\text{Volt}}$$

Thus complete open loop transfer function T_{OL}:

$$T_{OL} = \frac{K_{FP}}{S} * K_{\phi} * K_{FLTR} * K_{VCO} * F_{REF} = \frac{2\pi}{S} * \frac{.125 * 10^{-3}}{2\pi} * K_{FLTR} * \frac{1}{2.5} * F_{REF}$$

$$= \frac{K_{FLTR}}{S} * \frac{F_{REF}}{20 * 10^3} = \frac{(SR_1C_1 + 1)(S * 3.6 * 10^3 C_3 + 1) * F_{REF}}{S^3(C_1 + C_2)C_3\left(SR_1\frac{C_1C_2}{C_1 + C_2} + 1\right) * 720 * 10^6}$$



Must define desired F_{REF}, f_0, Z_2, P_1, Z_1; then can proceed with component value determination.

If $F_{OUT} = 36 * 10^6$, $N = 50$ (typical numbers), then $F_{REF} = 720 * 10^3$
Assume: $f_0 = 1000Hz$, $Z_2 = 250Hz$, $P_1 = 3000Hz$, $Z_1 = 45Hz$

1. Set Z_1 with C_3:

$$3.6 * 10^3 * C_3 = \frac{1}{2\pi Z_1} \longrightarrow C_3 = \frac{1}{2\pi * 45 * 3.6 * 10^3} = .982 * 10^{-6} \sim 1\mu F$$

2. Set –3 intercept frequency f_3 with $(C_1 + C_2)$: $f_3 = (Z_1Z_2f_0)^{1/3} = (11.25 * 10^6)^{1/3}$

$$\longrightarrow C_1 + C_2 = \frac{720 * 10^3}{(2\pi)^3 * 11.25 * 10^6 * 10^{-6} * 720 * 10^6} = .358 * 10^{-6}$$

3. Ratio $\frac{Z_2}{P_1} = \frac{R_1\left(\frac{C_1C_2}{C_1 + C_2}\right)}{R_1C_1} = \frac{C_2}{C_1 + C_2} \longrightarrow C_2 = (C_1 + C_2)\frac{Z_2}{P_1} = .358 * 10^{-6} * \frac{250}{3000} = .0298 * 10^{-6} \sim .030\mu F$

4. $C_1 = (C_1 + C_2) - C_2 = .358 * 10^{-6} - .030 * 10^{-6} = .328 * 10^{-6} \sim .33\mu F$

5. Set Z_2 with R_1: $R_1C_1 = \frac{1}{2\pi Z_2} \longrightarrow R_1 = \frac{1}{2\pi * 250 * .33 * 10^{-6}} = 1.929 * 10^3 \sim 1.91K$

ORDERING INFORMATION

PART NUMBER	PACKAGE	PIN COUNT	TEMPERATURE RANGE
ML4417CP	DIP-16	16	0°C to 70°C
ML4417CS	SO-16 (Narrow)	16	0°C to 70°C
ML4427CP	DIP-16	16	0°C to 70°C
ML4427CS	SO-16 (Narrow)	16	0°C to 70°C

Micro Linear

ML4431

Servo Demodulator

GENERAL DESCRIPTION

The ML4431 provides all of the analog circuitry necessary for the demodulation of di-bit servo signal information in Winchester disk drives. It interfaces to the servo head preamp and provides quadrature position signal outputs for the servo controller circuitry.

The ML4431 includes a high-performance 592-type input amplifier and differential AGC circuit. External logic is designed to meet the needs of the particular servo system utilizing the VCO and Charge Pump to create a PLL time base for Peak Detector gating. The SYNC output provides servo channel timing information for the logic.

The ML4431 has an ECL-type VCO, with an internal ECL-to-TTL converter for simplified interfacing.

The ML4431, when combined with the ML4402 Servo Driver, the ML4403, ML4413 Servo Controller and the ML4404 Trajectory Generator, provides a flexible closed-loop servo control system.

FEATURES

- Combines all analog di-bit demodulation circuitry
- Logic track-type switching can be used to minimize demodulator offset
- Exponential AGC characteristics makes AGC settling independent of input step size
- External loop compensation of analog blocks
- External digital circuitry allows flexible pattern format
- On-chip band gap voltage reference eliminates external referencing
- Operates from 5V and 12V power supplies
- Programmable Peak Detector Discharge Current
- Digitally-controlled AGC set point
- TTL output VCO
- AGC Sense switchable to "POSA only" or both "POSA and POSB"
- Compatible with Micro Linear's ML4403, ML4413 Servo Controller, ML4402 Servo Driver and ML4404 Trajectory Generator

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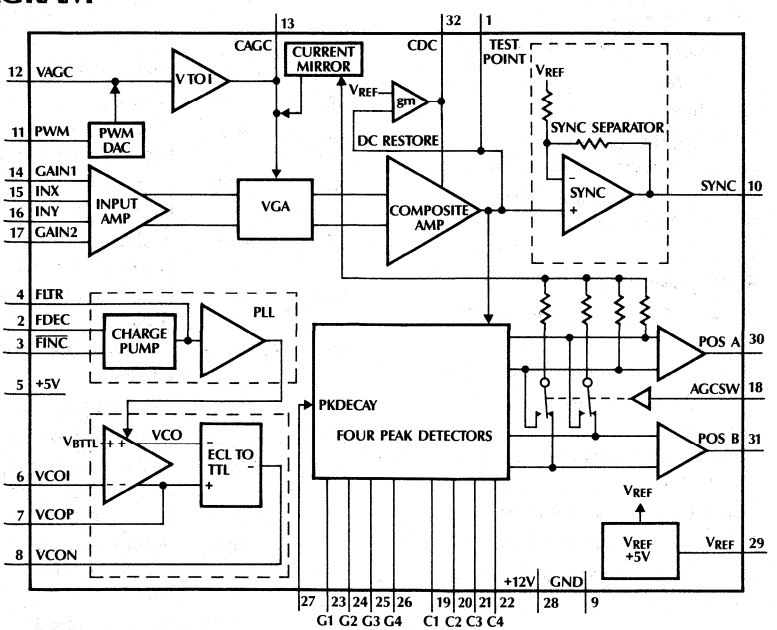
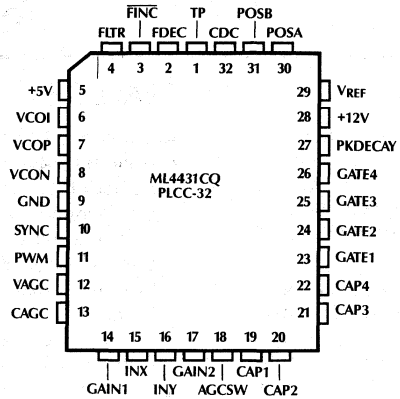
BLOCK DIAGRAM



PIN CONNECTIONS

ML4431 32-Pin PCC



PIN DESCRIPTION

PIN NO.	NAME	FUNCTION
1	TP	Composite test point, normally left unconnected.
2	FDEC	Charge pump frequency decrement input.
3	$\overline{\text{FINC}}$	Charge pump frequency increment input.
4	FLTR	PLL loop compensation terminal.
5	+5V	+5V supply.
6	VCOI	VCO input.
7	VCOP	VCO positive output, for capacitive feedback to VCOI.
8	VCON	VCO negative output, drives resistive feedback to VCOI.
9	GND	Ground.
10	SYNC	SYNC pulse output.
11	PWM	PWM DAC input to adjust AGC set point.
12	VAGC	AGC gain reference voltage input.
13	CAGC	External capacitor to set AGC response.
14	GAIN1	Input amplifier gain adjusting RC terminal 1
15	INX	X input into input amplifier.
16	INY	Y input into input amplifier.
17	GAIN2	Input amplifier gain adjusting RC terminal 2.
18	AGCSW	Selects between "POSA only" or "POSA and POSB" AGC sense operation. Logic "0" selects "POSA only" operation. Logic "1" selects "POSA and POSB" operation.
19	CAP1	Peak detector 1 capacitor.
20	CAP2	Peak detector 2 capacitor.
21	CAP3	Peak detector 3 capacitor.
22	CAP4	Peak detector 4 capacitor.
23	GATE1	Peak detector 1 gate input (TTL) Logic "1" enabled, "0" disabled.
24	GATE2	Peak detector 2 gate input (TTL) Logic "1" enabled, "0" disabled.
25	GATE3	Peak detector 3 gate input (TTL) Logic "1" enabled, "0" disabled.
26	GATE4	Peak detector 4 gate input (TTL) Logic "1" enabled, "0" disabled.
27	PKDECAY	Sets peak detector discharge current.
28	+12V	+12V supply.
29	V_{REF}	Voltage reference output.
30	POSA	Position output A. POSA = Peak Detector 1 – Peak Detector 2
31	POSB	Position output B. POSA = Peak Detector 3 – Peak Detector 4
32	CDC	External capacitor terminal to set DC restore response.

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

Power Supply Voltage Range, V_{CC} 14V
Input Voltages:
- GAIN1, GAIN2 ..... –0.3 to 8V
- C_{AGC} ..... –0.3 to 7.0V
- V_{AGC}, PWM, VCOI ..... –0.3 to 5.3V
- CAP1, CAP2, CAP3, CAP4 ..... –0.3 to 10V
- GATE1, GATE2, GATE3, GATE4, VCOP ..... –0.3 to 7.5V
- INX, INY, VCON, $\overline{FINC}$, FDEC, C_{DC}, C_{AGC}, FLTR ..... –0.3 to V_{CC} +0.3V

θ_{JA} for PLCC-32 ..... ≈60°C/Watt
Storage Temperature Range ..... –65°C to +150°C
Junction Temperature (T_{JMAX}) ..... 150°C
Lead Temperature (Soldering, 10 sec) ..... 260°C

OPERATING CONDITIONS

Temperature Range ..... 0°C to 70°C
Supply Voltage $V_{(+12V)}$ ..... $12V_{DC}$ ± 10%
Supply Voltage $V_{(+5V)}$ ..... $5V_{DC}$ ± 10%
Input Coupling Capacitance (C_I) 0.01μF
Input Amp Gain Capacitance (C_G) 0.047μF
Input Amp Gain Resistance (R_G) 1kΩ
AGC Response Compensation Capacitance (C_A) 0.018μF
Composite DC Restore Capacitance (C_D) 0.018μF
PLL Compensation Components:
- C_{CP1} 0.1μF
- C_{CP2} 1μF
- R_{CP} 910Ω

VCO Components:
- C_V 39pF
- R_V 1500Ω
- RL 680Ω

Peak Detector Capacitance (CAP1 thru CAP4) 270pF
On track Base-to-Peak Voltage at pin TP 1.75V
V_{GA} Gain Control Voltage (at pin C_{AGC}) ..... ≈2.4V
R_{SET} 330KΩ

ELECTRICAL CHARACTERISTICS

The following specifications apply over the recommended operating conditions of T_A = 0°C to 70°C, $V_{(+12V)}$ = 10.8 to 13.2V, $V_{(+5V)}$ = 4.5 to 5.5V, V_{VAGC} = 4.0V, and external components as recommended above, unless otherwise specified (See Note 1)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Power Supply						
I_{+12}	Supply Current	V_{+12} = 12V, V_{+5} = 5V		37	59	mA
I_{+5}	Supply Current	V_{+12} = 12V, V_{+5} = 5V		42	51	mA
TTL Inputs $\overline{FINC}$, FDEC, GATE1, GATE2, GATE3, GATE4, PWM, AGCSW						
V_{IH}	High Level Input Voltage		2.0			V
V_{IL}	Low Level Input Voltage				0.8	V
I_{IH}	High Level Input Current	V_{IH} = 2.4V	–1		30	μA
I_{IL}	Low Level Input Current	V_{IL} = 0.4V	–20		1	μA
SYNC Output						
V_{OL}	Low Level Output Voltage	I_{OL} = 1.6mA	0	0.35	0.5	V
V_{THR}	Positive going input threshold			V_{REF}+0.9		V
V_{THF}	Negative going input threshold			V_{REF}		V
$t_{PD}\pm$	Propagation Delay Rising, Falling	RL = 2k, C_L = 15pF		50		ns
VCON Output						
V_{OH}	High Level Output Voltage	I_{OH} = 50μA	2.4			V
V_{OL}	Low Level Output Voltage	I_{OL} = 1.6mA	0		0.5	V
VCO and Charge Pump Section						
I_{BIAS}	V_{COI} Input Bias Current		0	20	50	μA
I_{CH}, I_{DIS}	FLTR Charge and Discharge Current		330	450	590	μA
I_{CH}/I_{DIS}	FLTR Charge/Discharge Ratio		0.95	1.00	1.05	μA/μA
I_{OFF}	FLTR OFF State Current	$\overline{FINC}$ = 2.0, FDEC = 0.8	0	25	50	nA
F_{MAX}	MAX VCO Frequency to Maintain + and – 5% Control Range (Note 3)		20			MHz
V_{QH} (FLTR)	Charge Pump Maximum Voltage			$V_{(+12V)}$–1V		V
V_{QL} (FLTR)	Charge Pump Minimum Voltage			1.0		V

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ELECTRICAL CHARACTERISTICS (Continued)

The following specifications apply over the recommended operating conditions of T_A = 0°C to 70°C, $V_{(+12V)}$ = 10.8 to 13.2V, $V_{(+5V)}$ = 4.5 to 5.5V, V_{AGC} = 4.0V, and external components as recommended above, unless otherwise specified (See Note 1)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
VCO and Charge Pump Section (Continued)						
F_{VCO}	VCO Frequency Range (Note 3)	T_A = 25°C, V_{CC} = 12, V_{FLTR} = 6V, C_V = 30pF, R_V = 3.74KΩ, see figure 1	9.7	10.0	10.3	MHz
K_{VCO}	VCO Voltage to Frequency Factor			2		%/V
Input AMP, AGC AMP, and DC Restore						
R_{IN}	INX, INY Differential Input Resistance		7	10	14	kΩ
$I_{GAIN1,2}$	GAIN1, GAIN2 Bias Current		0.66	1.0	1.20	mA
R_{INAGC}	V_{AGC} Input Resistance		7	10	13	kΩ
G_{MAGC}	AGC Transconductance at C_{AGC}			370		μMHOS
R_{AGC}	Control Range of AGC Loop to Regulate Composite Amplitude to within 2% of Nominal			7/1		V/V
BW	Bandwidth from INX, INY to Composite (Note 4)		10	15		MHz
GMDCR	DC Restore Transconductance			500		μMHOS
Peak Detectors						
I_{CH}	Charge Current		5			mA
I_{DIS}	Discharge Current	T_A = 25°C, R_{SET} = 330K	10	15	20	μA
Voltage Reference						
V_{REF}	Reference Voltage	T_A = 25°C	4.75	5.00	5.25	V
TC	Tempco			50		ppm/°C
R_{OUT}	Load Regulation			2		mV/mA
PSRR	Line Regulation			10		mV/V
I_{SINK}	Maximum SINK Current		0.8			mA
Output Amplifiers (POSA, POSB)						
V_{OS}	Input Offset	V_{CAP}1–4 = 6V	–10	0	10	mV
A_V	Gain		1.15	1.20	1.25	V/V
A_{VA}/A_{VB}	Gain Tracking		–3	0	+3	%
V_{OUT}	Output Voltage Range		1.0		9.5	V
I_{SRC}	Output Source Current		5			mA
I_{SNK}	Output Sink Current		2			mA
SR	Slew Rate			2.5		V/μs
BW	3dB Gain Bandwidth			3		MHz

Note 1: 0°C to 70°C operating temperature range devices are 100% tested with temperature limits guaranteed by 100% testing, sampling, or correlation with worst-case test conditions.

Note 2: Typicals are parametric norm at 25°C.

Note 3: This parameter is guaranteed but not 100% tested and is not used in outgoing quality level calculations.

APPLICATION HINTS

Using a nominal on-track servo signal, amplitude adjustment should be made as follows:

1. Set composite signal amplitude, measured at pin TP, by adjusting voltage at pin V_{AGC} (approximately 4.7 volts). The composite signal should be set to 1.75 volts base to peak of an on-track position pulse (an off-track position pulse will be about 3.5 volts maximum).
2. Adjust Rg so that the VGA is in mid-range. This is determined by measuring the voltage at pin C_{AGC}; it should be approximately 0.9 volts. C_{AGC} voltage will vary approximately ±0.5 volts over the AGC range.

FUNCTIONAL DESCRIPTION

INPUT AMPLIFIER

The input amplifier is equivalent to a wide-band 592 type video amplifier and provides amplification and buffering to the AGC circuitry. The Inputs INX and INY, which must be AC coupled, accept the composite analog signal from the servo head differential preamplifier. Internal input termination resistors eliminate the need for external bias resistors. Prefiltering of the signal is normally desired to eliminate unwanted components. External components R_G and C_G determine the input amplifier's low frequency cutoff and gain as follows:

$$FC = \frac{1}{2\pi(R_G + 60\Omega)C_G} \qquad A_V = \frac{1700}{R_G + 60\Omega}$$

Where: C_G = External series capacitance between pins GAIN1 and GAIN2
R_G = External series resistance between pins GAIN1 and GAIN2

AUTOMATIC GAIN CONTROL (AGC)

The purpose of the AGC loop is to maintain a constant peak output voltage level at outputs POSA and POSB. This peak level is established by the reference voltage applied to pin V_{AGC}.

$$V_{P-P\ (Composite\ Position\ Pulses)} = K1 \times V_{AGC} + K2$$

Where: K1 = 0.65
K2 = .13 * V_{REF}

In this closed-loop system, the peak detector output voltages are fed back and combined with the V_{AGC} voltage to provide a gain control current. The current controls the variable gain amplifier (VGA) and is compensated at pin C_{AGC} to provide control of AGC bandwidth. The bandwidth of the entire AGC loop is determined by:

$$BW = \frac{K\ V_{VAGC}}{2\pi\ C_A}$$

Where: K = 2.8×10^{-4}
V_{VAGC} = External reference voltage at pin V_{AGC}
C_A = External capacitance at pin C_{AGC}

PWM CONTROL OF AGC SET POINT

The PWM input (pin 10) accepts a variable duty-cycle input to control the AGC set point. The relationship between duty-cycle and set point is:

100% duty-cycle ..... AGC set point is equal to V_{REF}.

0% duty-cycle ..... AGC set point equal to 0.6 × V_{REF}.

A filter capacitor from pin 11 to ground is required to filter the PWM signal. This capacitor should be sufficiently large relative to the 10KΩ nominal internal termination resistance at pin 11.

The AGC set point may be set manually via direct voltage control of pin 12 if desired. Pin 11 should be grounded in this case.

SWITCHING THE AGC SENSE RESISTORS

The AGCSW input (pin 17) allows selection of the AGC sense. The choices are:

AGCSW low ..... AGC senses POS A peak detector outputs only.

AGCSW high ..... AGC senses POS A and POS B peak detector outputs.

COMPOSITE AMPLIFIER

The input amplifier and AGC circuit of the ML4431 operate in a differential signal mode to provide good common mode and power supply rejection. The composite amplifier converts the differential signal into a buffered single-ended signal for the peak detector circuitry. The DC base line of the composite signal is equal to V_{REF}. The bandwidth of the DC restore function is controlled by capacitor C_D at pin C_{DC} with the following relationship:

$$BW = \frac{gm}{2\pi\ C_D}$$

Where: $gm = \frac{1}{2K\Omega}$
C_D = External capacitance at pin C_{DC}

The composite signal is available at pin TP and is normally left unconnected. For short circuit protection a 750Ω resistor is connected in series with pin TP internally.

SYNCHRONIZATION PULSE SEPARATOR

The SYNC pulse separator is a threshold comparator with hysteresis which passes pulses from the composite amplifier above a set threshold. It provides a buffered TTL output. The SYNC output, when gated through an external one-shot, is used to control the external gate timing and PLL logic.

PEAK DETECTOR

The peak detector circuit captures the peak signal amplitude of the di-bit pulses. The gates are controlled by inputs GATE1 through GATE4. Timing is established by the external logic circuitry. The external peak detector capacitors are connected from pins CAP1 through CAP4 to ground. The peak detector discharge rate (set by CAP1–CAP4 and current out of PKDECAY) determines the maximum track crossing rate during an access operation. The peak detector outputs are fed into internal differential amplifiers that calculate the track error signals and provide buffered outputs POSA and POSB as follows:

POSA = 1.20 (CAP1 – CAP2) + V_{REF}
POSB = 1.20 (CAP3 – CAP4) + V_{REF}

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PEAK DETECTOR DECAY RATE CONTROL

The decay rate of the peak detector can be programmed by changing the external resistor R_{SET} (pin 26, see connection diagram). The decay rate is determined by the discharge current for the hold capacitors C1 – C4. The relationship between the discharge current and R_{SET} is:

$$I_{DISCHARGE} = \frac{V_{REF}}{R_{SET}}$$

VOLTAGE CONTROLLED OSCILLATOR AND CHARGE PUMP

The VCO and external phase compare logic provide a time base for peak detector gate synchronization. Inputs FINC and FDEC provide increment and decrement signals to the charge pump for changing the oscillator frequency. The FINC and FDEC inputs gate the charge pump for the duration of the pulse width. The RC timing network formed by C_V and R_V at pins VCOI, VCON, and VCOP control the oscillators center frequency. (See Typical Performance Characteristics)

R_V should be greater than 1000Ω, Too low of a value will result in excessive power dissipation. RL should be about 680Ω.

The VCO output should only be taken from pin VCON. Charge pump capacitor C_{CP1} is connected from pin FLTR to ground. Components R_{CP} and C_{CP2} are also connected in series from pin FLTR to ground to provide VCO loop compensation.

INTERNAL VOLTAGE REFERENCE

V_{REF} is an internal band-gap voltage reference. It is buffered and available at pin V_{REF} and is used by the ML4402, ML4403, ML4404 and other chips requiring a 5 volt reference.

EXTERNAL LOGIC

The external logic provided by the user typically has a complexity of about 150 to 300 equivalent gates. Complexity and architecture depends on the users di-bit pattern and control function.

Note: Stray capacitance should be considered in applying the above relationships when low capacitor values are used. Stray capacitance of the integrated circuit terminal is typically about 2 to 3pF.

TYPICAL PERFORMANCE CHARACTERISTICS

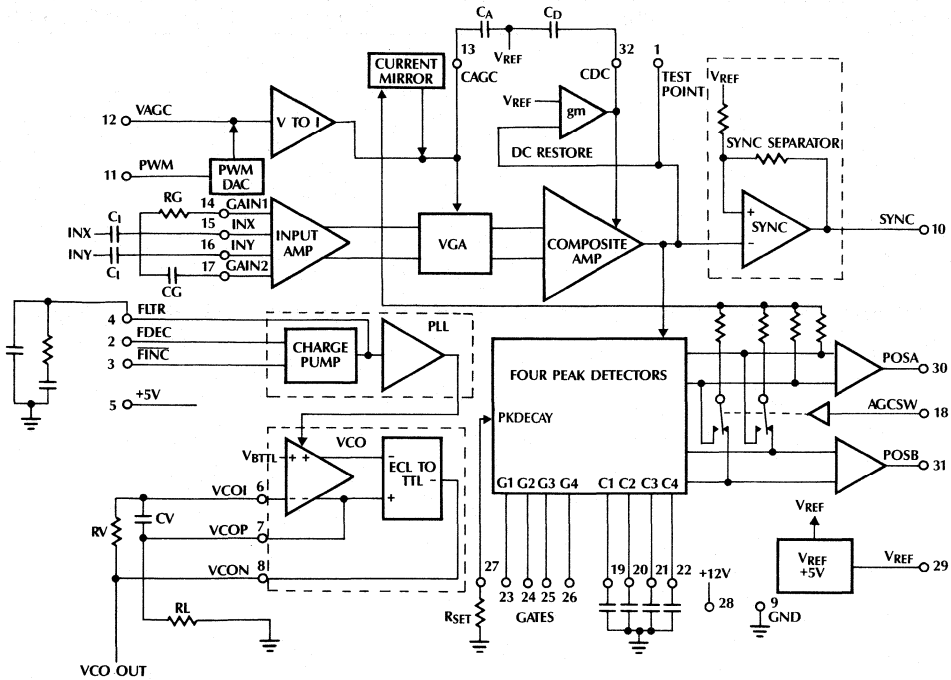
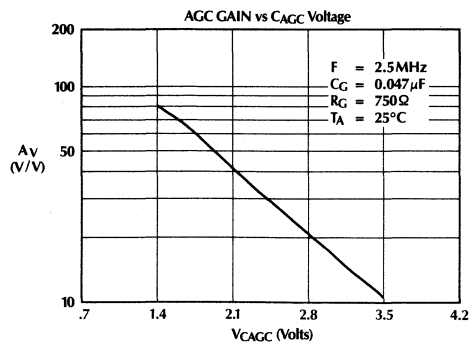


Figure 1. ML4431 Connection Diagram



ORDERING INFORMATION

ORDERING NUMBER	PACKAGE	PIN COUNT	TEMPERATURE RANGE
ML4431CQ	PLCC-32	32 pins	0°C to +70°C

Micro Linear

ML4510

5V Sensorless Spindle Motor Controller

GENERAL DESCRIPTION

The ML4510 provides complete commutation for delta or wye wound Brushless DC (BLDC) motors without the need for signals from Hall Effect sensors. This IC senses the back EMF of the 3 motor windings (no neutral required) to determine the proper commutation phase angle using phase lock loop techniques. This technique will commutate virtually any 3-phase BLDC motor and is insensitive to PWM noise and motor snubbing.

Included in the ML4510 is the circuitry necessary for a Hard Disk Drive microcontroller driven control loop. The ML4410 controls motor current with either a constant off-time PWM or linear current control driven by the microcontroller. Speed feedback for the micro is a stable digital frequency equal to the commutation frequency of the motor. All commutation is performed by the ML4510. Braking and Power Fail are also included in the ML4510.

Since the timing of the start-up sequencing is determined by external circuitry, the system can be optimized for a wide range of motors and inertial loads.

The ML4510 modulates the gates of external N-channel power MOSFETs to regulate the motor current. The IC drives external PNP transistors or P-channel MOSFETs directly. Special circuits are used to save base drive power at low load currents.

FEATURES

- Back-EMF Commutation Provides Maximum Torque for Minimum "Spin-Up" Time for Spindle Motors
- Accurate, Jitter-Free Phase Locked Motor Speed Feedback Output
- Operates on Single 5V Power Supply
- Linear or PWM Motor Current Control
- Easy Microcontroller Interface for Optimized Start-Up Sequencing and Speed Control
- Power Fail Detect Circuit
- Drives External N-Channel FETs and PNP's or P-Channel FETs

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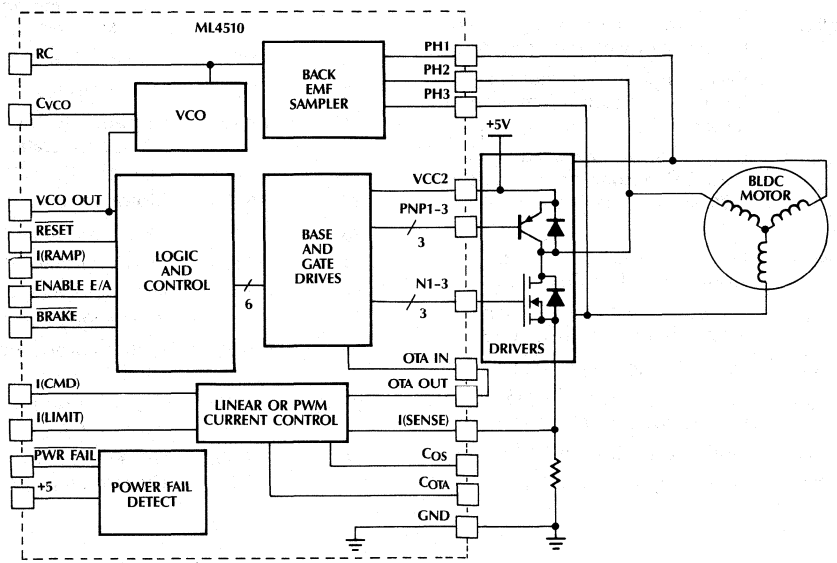
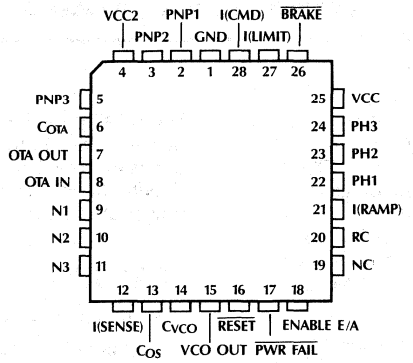
BLOCK DIAGRAM



PIN CONFIGURATION

ML4510
28-Pin PCC



TOP VIEW

PIN DESCRIPTION

PIN #	NAME	FUNCTION
1	GND	Signal and Power Ground.
2	PNP1	Drives the external PNP power transistor driving motor PH1.
3	PNP2	Drives the external PNP power transistor driving motor PH2.
4	VCC2	5V power.
5	PNP3	Drives the external PNP power transistor driving motor PH3.
6	C_{OTA}	Compensation capacitor for linear motor current amplifier loop.
7	OTA OUT	Output of motor current error amplifier, normally connected to OTA IN or to external MOSFET gate.
8	OTA IN	Driving voltage for N1–N3. Normally tied to OTA OUT.
9–11	N1, N2, N3	Drives the external N-channel MOSFETs for PH1, PH2, PH3.
12	I(SENSE)	Motor current sense input.
13	C_{OS}	Timing capacitor for fixed off-time PWM current control.
14	C_{VCO}	Timing capacitor for VCO.
15	VCO OUT	Logic output from VCO.
16	$\overline{\text{RESET}}$	Input which holds the VCO off and sets the ML4410 to the RESET condition.
17	$\overline{\text{PWR FAIL}}$	A "0" output indicates 5V is under-voltage.
18	ENABLE E/A	A "1" logic input enables the error amplifier and closes the back-EMF feedback loop.
19	NC	No Electrical Connection.
20	RC	VCO loop filter components.
21	I(RAMP)	Current into this pin sets the initial acceleration rate of the VCO during start-up.
22	PH1	Motor Terminal 1.
23	PH2	Motor Terminal 2.
24	PH3	Motor Terminal 3.
25	VCC	5V power supply. Terminal which is sensed for power fail.
26	BRAKE	A "0" activates the braking circuit.
27	$\overline{\text{I(LIMIT)}}$	Sets the threshold for the PWM comparator.
28	I(CMD)	Current Command for Linear Current amplifier.

Micro Linear

ML4568

Disk Pulse Detector + Embedded Servo Detector

GENERAL DESCRIPTION

The ML4568 is a hard disk pulse detector with two gated peak detectors to demodulate embedded servo information. The pulse detector section includes a wide bandwidth differential amplifier with automatic gain control (AGC), a precision full wave rectifier, time channel and gate channel. The embedded servo peak detector section includes a full-wave rectifier, two gated peak detectors, buffered peak detector outputs, and a difference output. A 2.25V bandgap reference is also included on-chip.

The ML4568 is a 5V-only upgrade for 8468-type devices. Upgraded features include increased data rate operation (to 24 MB/s with RLL(1, 7) coding), improve pulse pairing (1ns), and reduced power consumption (400mW typical) resulting from 5V-only operation.

The ML4568 pulse detector section detects amplitude peaks, producing a TTL-compatible output which accurately indicates the time position of signal peaks. In hard disk applications, these signal peaks represent flux reversals in the magnetic medium.

FEATURES

- 5V-only operation
- Low power consumption (400mW typical)
- Supports 24 MB/s RLL(1, 7) coding
- Less than ±1 ns Pulse Pairing
- Wide input signal amplitude range (10mV$_{PP}$ to 100mV$_{PP}$)
- On-chip differential gain controlled amplifier, differentiator, comparator gating circuitry, and output pulse generator
- Adjustable comparator hysteresis
- Dynamic hysteresis tracks signal amplitude
- AGC and differentiator time constants set by external components
- TTL compatible digital inputs and outputs
- Built in embedded servo detector
- On chip buffers provide low impedance servo output voltages
- User adjustable servo time constants

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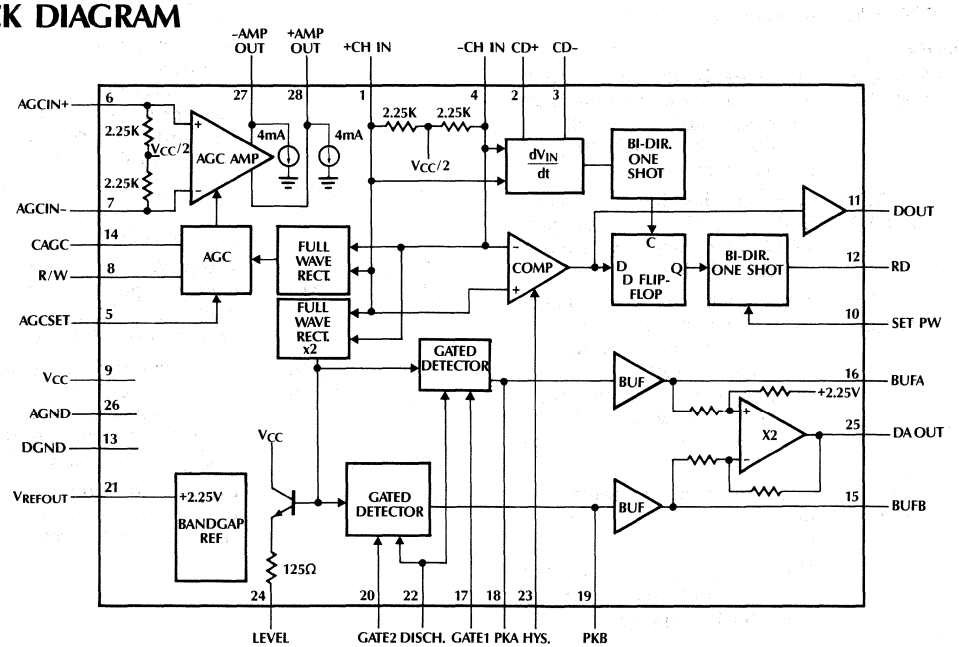
BLOCK DIAGRAM

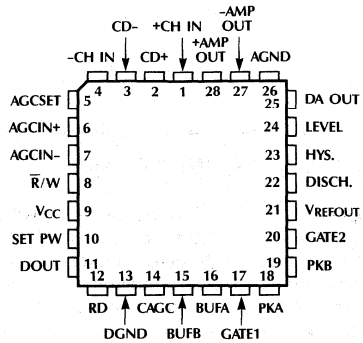


GENERAL DESCRIPTION (Continued)

The ML4568 also incorporates two gated detectors which detect embedded servo information, used for head positioning. The ML4568 provides two buffered low impedance voltage outputs which represent the peak detected level of each servo burst. The ML4568 also provides a buffered output that represents the voltage difference between the two servo channels, centered about V_{REF}.

PIN CONFIGURATION

PLCC-28



TOP VIEW

PIN DESCRIPTION

PIN #	NAME	FUNCTION
Power Supply		
9	V_{CC}	+5V ± 10% supply.
21	$V_{REF\ OUT}$	Internal 2.25 V reference voltage output.
26	ANALOG GROUND	Analog signals should be referenced to this pin.
13	DIGITAL GROUND	Digital signals should be referenced to this pin.
Analog Signals		
6 7	AMP IN+ AMP IN–	These are the differential inputs to the Amplifier. The output of the read/write head amplifier should be capacitively coupled to these pins.
28 27	AMP OUT+ AMP OUT–	These are the differential outputs of the Amplifier. These outputs should be capacitively coupled to the channel filter.
4 1	–CH IN +CH IN	These are the differential inputs to the time, gating and servo channels. These inputs must be capacitively coupled to the channel filter at the amp. outputs. The maximum differential peak-to-peak swing at this input is 1.5 V_{P-P}.
2 3	CD+ CD–	The external differentiator network is connected between these two pins.
23	HYS.	The DC voltage on this pin sets the amount of hysteresis on the differential comparator.

PIN #	NAME	FUNCTION
Analog Signals (Continued)		
24	LEVEL	This is a Peak Detector Output signal that is used in conjunction with the set hysteresis pin 23 to provide a dynamic hysteresis function.
5	AGCSET	The AGC circuit adjusts the gain of the gain controlled amplifier to make the differential peak to peak voltage at the Channel inputs equal to four times the DC voltage on this pin. $V_{AGCSET} = ½V_{CC} + ¼V_{PP}$ where V_{PP} is the peak-peak differential voltage on the channel input.
14	CAGC	The external capacitor for the AGC is connected between this pin and Analog Ground.
18 19	PKA PKB	The peak detected servo signal voltage appears across the RC networks connected from these pins to analog ground.
16 15	BUFA BUFB	These low impedance pins, output the DC level at pins 18 and 19 respectively, level shifted down by two diode drops.
25	DA OUT	This low impedance pin outputs the difference in voltage between pins 16 and 15 about a zero level set by the voltage on pin 21.

PIN DESCRIPTION (Continued)

PIN #	NAME	FUNCTION
Digital Signals		
10	SET PW	An external capacitor to control the pulse width of the Encoded Data Out (RD) is connected between this pin and Digital Ground. See Figure 1.
8	$\overline{R}$/W	If this pin is low, the Pulse Detector is in the read mode and the chip is active. When this pin goes high, the pulse detector is forced into a stand-by mode. This is a standard TTL input.
11	DOUT	This is the buffered, open collector, output of the differential comparator with hysteresis.
12	RD	This is the standard TTL output whose leading edge indicates the time position of the peaks.
Digital Signals (Continued)		
17	GATE 1	These inputs accept TTL levels. When a low level is present the embedded servo signal is allowed to charge the RC network at pins 18 and 19 respectively. A high level will force a hold condition of the DC voltage across the RC network and will also disable the servo channel.
20	GATE 2	
22	DISCH.	This input accepts a TTL level. A high level connects a 1.5K internal resistor to ground on pins 18 and 19.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage
Pin 9 ..... 14V
TTL Input Voltage
Pins 8, 17, 20, 22 ..... 5.5V
TTL Output Voltage
Pins 12, 11 ..... 5.5V
Input Voltage
Pins 23, 5 ..... 5.5V
Minimum Input Voltage
Pins 23, 5 ..... –0.5V
Differential Input Voltage
Pins 6–7, 4–1 ..... 3V or –3V
ESD susceptibility rating is to be determined
Storage Temperature ..... –65°C to +150°C
Lead Temperature (Soldering 10 sec.) ..... 300°C
Maximum Power Dissipation at 25°C:
PLCC Package (derate TBD mW/°C above 25°C) ... 500mW

OPERATING CONDITIONS

V_{CC} ..... 4.5V to 5.5V
Ambient Temperature, T_A ..... 0°C to +70°C

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ELECTRICAL CHARACTERISTICS

Over recommended operating conditions.
Set Hysteresis = 0V, $V_{PIN\ 17}$ = 2V, READ/WRITE = 0.4V, $V_{PIN\ 22}$ = 0.4V, unless otherwise noted.

Symbol	Pins	Parameter	Conditions	Min	Typ	Max	Units
Amplifier							
Z_{INAI}	6, 7	Amp In Impedance (Note 1)	T_A = 25°C	1.8	2.4	3.0	KΩ
A_{VMIN}	28, 27	Minimum Voltage Gain Differential	AC Output 3 V_{PP}		6	15	V/V
A_{VMAX}	28, 27	Maximum Voltage Gain Differential	AC Output 3 V_{PP}	250	300		V/V
Channel							
Z_{INCI}	4, 1	Channel Input Impedance	T_A = 25°C (Note 1)		2.5		KΩ
I_{CAGC^-}	14	Pin 14 Current which Charges C_{AGC}	$V_{PIN\ 14}$ = 2.2V	5.0	5.8		mA
I_{CAGC^+}	14	Pin 14 Current which Discharges C_{AGC}	$V_{PIN\ 14}$ = 2.2V		0.5	2	μA
I_{AGCSET}	5	AGCSET Input Bias Current			8	100	μA
I_{IL}	23	Set Hysteresis Input Bias Current	$V_{PIN\ 23}$ = 0			-20	μA
I_{CD}	2, 3	Current into Pin 2 and 3 that Discharges C_D		0.8	1.0		mA
HYS	23	Peak Hys. vs V_{HYS}	$V_{PIN\ 23}$ = 1V	0.25	0.4	0.55	V_{PK}/V_{DC}
Write Mode							
Z_{INAI}	6, 7	Amp In Impedance in Write Mode	$V_{PIN\ 8}$ = 2.0V		350	450	Ω
I_{AGC^-}	14	Pin 14 Current in Write Mode	$V_{PIN\ 8}$ = 2.0V, $V_{PIN\ 14}$ = 2.2V		0.2	1.0	μA
Digital Pins							
V_{IH}	8, 17, 20, 22	High Level Input Voltage		2			V
V_{IL}	8, 17, 20, 22	Low Level Input Voltage				0.8	V
I_{IH}	8, 17, 20, 22	High Level Input Current	V_{5V} = Max, V_I = 2.7V			20	μA
I_{IL}	8, 17, 20, 22	Low Level Input Current	V_{5V} = Max, V_I = 0.5V		140	200	μA
V_{OH}	12	High Level Output Voltage	V_{5V} = Min, I_{OH} = -400μA (Note 2)	2.4			V
V_{OL12}	12	Low Level Output Voltage	V_{5V} = Min, I_{OL} = 800μA (Note 2)			0.5	V
I_{LH}	11	High Level Output Leakage Current	$V_{PIN\ 11}$ = 5.5V Measure Current into Pin 11			10	μA
V_{OL11}	11	Low Level Output Voltage	$I_{PIN\ 11}$ = 800 μA			0.5	V
Servo Channel							
Z_{DIS}	18, 19	Discharge Impedance	$V_{PIN\ 22}$ = 2V (discharge) Force 2.5V on Pins 18 or 19	0.5	1.8	2.5	KΩ
V_{BOQ}	15, 16	Buffer Quiescent Output Level	$V_{PIN\ 17, 20, 22}$ = 0.4V, V_{CI} = 0V Pull 0mA from Pins 15 and 16	1.0	1.6	2.0	V
$V_{LEVEL\ Q}$	24	Level Quiescent Output Level	V_{CI} = 0V Pull 200μA from Pin 24		0.2	0.5	V
I_L	18, 19	Gated Off Leakage Current	$V_{PIN\ 22}$ = 0.4V, $V_{PIN\ 20}$ = $V_{PIN\ 17}$ = 2V Force 3V on Pin 18 or Pin 19	-1		1	μA

ELECTRICAL CHARACTERISTICS (Continued)

Over recommended operating conditions.
Set Hysteresis = 0V, $V_{PIN\ 17}$ = 2V, READ/WRITE = 0.4V, $V_{PIN\ 22}$ = 0.4V, unless otherwise noted.

Symbol	Pins	Parameter	Conditions	Min	Typ	Max	Units
Servo Channel (Continued)							
V_{OSBO}	16, 15	Buffer Output Offset Voltage for V_{CI} = $1V_{PK-PK}$	$V_{PIN\ 17, 20, 22}$ = 0.4V, $V_{PIN\ 1}$ = 2.75V Pull 0mA from Pins 15 and 16 $V_{PIN\ 4}$ = 2.25V, V_{OSBO} = $V_{PIN\ 16}$ – $V_{PIN\ 15}$		2	±15	mV
V_{OSYS}	25, 21	System Output Offset Voltage for V_{CI} = $0.75V_{PK-PK}$ Pull 0mA from Pin 25 V_{OSYS} = $V_{PIN\ 25}$ – $V_{PIN\ 21}$	$V_{PIN\ 17, 20, 22}$ = 0.4 $V_{PIN\ 1}$ = 2.688V, $V_{PIN\ 4}$ = 2.313V		±5	±20	mV
A_{VDA} (1V)	25, 21	Difference Amplifier Gain, 1V Differential Input	$V_{PIN\ 17, 20}$ = 2V $V_{PIN\ 19}$ = 1.5V, $V_{PIN\ 18}$ = 2.5V, $V_{PIN\ 22}$ = 0.4V	1.6	2	2.4	V/V
A_{VDA} (.5V)	25, 21	Difference Amplifier Gain, 0.5V Differential Input	$V_{PIN\ 17, 20}$ = 2V $V_{PIN\ 19}$ = 1.75V, $V_{PIN\ 18}$ = 2.25V, $V_{PIN\ 22}$ = 0.4V	1.6	2	2.4	V/V
GL_{DA}	25	Difference Amplifier Gain Linearity			0.2	2.5	%
Z_{LEVEL} SOURCE	24	Level Out Output Impedance	$V_{PIN\ 17, 20, 22}$ = 0.4V, V_{CI} = 0.75V Measure $V_{PIN\ 24}$ with 200μA and 3mA pulled out of the pin. Z_{LEVEL} = change in $V_{PIN\ 24}$ SOURCE 3mA – 0.2mA	100	180	250	Ω
AV_{GD} (1.5V)	15, 16	Gated Detector Gain for V_{CI} = $1.5V_{PK-PK}$	$V_{PIN\ 22, 20, 17}$ = 0.4V $V_{PIN\ 1}$ = 2.875V, $V_{PIN\ 4}$ = 2.125V	1.45	1.8	2.25	V/V
AV_{GD} (0.75V)	15, 16	Gated Detector Gain for V_{CI} = $0.75V_{PK-PK}$	$V_{PIN\ 22, 20, 17}$ = 0.4V $V_{PIN\ 1}$ = 2.688V, $V_{PIN\ 4}$ = 2.313V	1.45	1.7	2.25	V/V
AV_{LEVEL} (1.5V)	24	Level Voltage Gain For V_{CI} = $1.5V_{PK-PK}$	$V_{PIN\ 1}$ = 2.875V, $V_{PIN\ 4}$ = 2.125V	1.45	1.8	2.25	V/V
AV_{LEVEL} (0.75V)	24	Level Voltage Gain For V_{CI} = $0.75V_{PK-PK}$	$V_{PIN\ 1}$ = 2.687V, $V_{PIN\ 4}$ = 2.312V	1.6	1.9	2.4	V/V
GL_{GD}	15, 16	Gated Detector Gain Linearity			±0.1	±2.5	%
I_{CC}	9	V_{CC} Supply Current	V_{CC} = Max	40	90	110	mA
V_{REF}	21	V_{REF} Voltage		2.0	2.25	2.5	V

AC ELECTRICAL CHARACTERISTICS

Over Recommended Operating Temperature and Supply Range refer to AC Test Setup.
f = 2.5MHz unless otherwise indicated. PKA, PKB = 1KΩ + 10nF to GND.

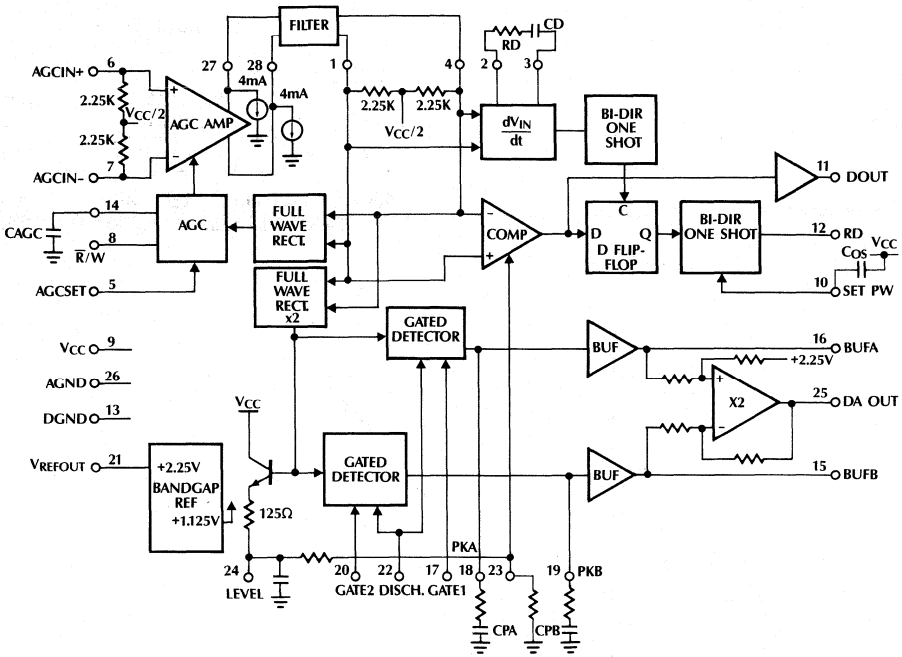
Symbol	Pins	Parameter	Conditions	Min	Typ	Max	Units
t_{CHARGE}	15, 16	Gated Detector Charge Time	V_{CI} = 1.5V_{PP}, $V_{PIN\ 22}$ = 0.3V, With PKA and PKB discharged, measure the time from Pin 17 or 20 going from 2V to 0.3V, to V_{BO1} or V_{BO2} respectively, reaching 90% of their final value		1.0		μs
$t_{DISCHARGE}$	15, 16	Gated Detector Discharge Time	V_{CI} = 1.5V_{PP}. With LP1 charged, measure the time from Pin 22 going from 0.3V to 2V, to the voltage at V_{BO1} or V_{BO2} reaching 90% of their final value		70		μs
t_{ON}	18, 19	Gated Detector Turn ON Time	V_{CI} = 0.35V_{DC}, $V_{PIN\ 22}$ = 0.3V. With LP1 discharged, measure the time from Pin 17 going from 2V to 0.3V, to the voltage on Pin 18 increasing 0.1V. Do a similar measurement with LP2, Pin 20 and Pin 19		0.2		μs
t_{OFF}	18, 19	Gated Detector Turn OFF Time	V_{CI} = 0.35V_{DC}, $V_{PIN\ 22}$ = 2V. Measure the time from Pin 17 going from 0.3V to 2V, to the voltage on Pin 18 decreasing by 0.1V. Do a similar measurement with Pins 20 and 19		0.4		μs
t_{PP}	12	Pulse Pairing ML4568-1	f = 2.5MHz and V_{CI} = 1V_{PP} differential			±1	ns
t_{PP}	12	Pulse Pairing ML4568-2	f = 2.5MHz and V_{CI} = 1V_{PP} differential			±3	ns

Notes:

1. The temperature coefficient of the input impedance is typically 0.05% per °C.
2. To prevent inductive coupling from the digital outputs to Amp In, the TTL outputs should not drive more than one ALS TTL load each. Pin 11 is an open collector output which is tested with an external 1K pullup resistor to the 5V supply.

ML4568 CONNECTION DIAGRAM

PLCC-28 Version



APPLICATION INFORMATION

SETTING THE OUTPUT PULSEWIDTH

The RD output pulsewidth is dependent on the value of C_{OS}, which is connected from pin 10 to V_{CC}. This relationship is shown in figure 1.

SELECTING C_D

The following table summarizes the maximum C_D value allowed for different data rates. These values are derived using

$$C_D \text{ (max)} = \frac{176}{f_{MAX}}$$

Data Rate	f_{MAX}	C_D (max)
7.5 MB/s	2.81 MHz	62.6 pF
24 MB/s	9 MHz	19.6 pF

Table 1. Maximum C_D Value Allowed for a 1.5 V_{P-P} Differential Signal Using RLL (1, 7) Code

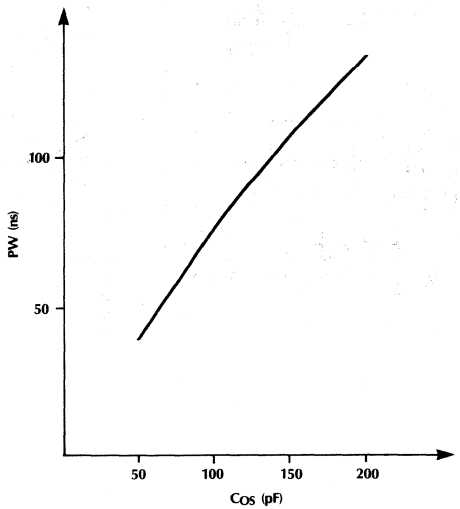


Figure 1. RD Output Pulsewidth as a Function of C_{OS}

ORDERING INFORMATION

PART NUMBER	PACKAGE	PULSE PAIRING
ML4568-1CQ	PLCC-28	±1 ns
ML4568-2CQ	PLCC-28	±3 ns

Micro Linear

ML8464B, ML8464C

Pulse Detector

GENERAL DESCRIPTION

The ML8464 is a Pulse Detector designed for use in magnetic disk applications to detect the amplitude peaks on the output of the read/write amplifier. These signal peaks are caused by flux reversal on the disk media, which when connected to the read/write amplifier result in an output consisting of a series of pulses of alternating polarity. The relative time position of these signal peaks is indicated by the leading edge of the TTL output pulses. The Pulse Detector accurately represents the time position of these peaks.

The ML8464 contains three major blocks. The amplifier block contains a wide bandwidth differential amplifier with Automatic Gain Control (AGC) and a precision full wave rectifier. The time channel block includes a programmable differentiator followed by a bidirectional one shot multivibrator. The gate channel block includes a differential comparator with programmable hysteresis, a D flip-flop and an output bi-directional one shot multivibrator. The ML8464C internally connects the time channel output to the D flip-flop.

FEATURES

- Wide differential input signal range 20–660 mV_{P-P}
- TTL compatible digital Inputs and Output
- Externally gain controlled input differential amplifier
- Variable hysteresis comparator with gating circuitry
- Differentiator with externally programmable time constants
- Standard 12V power requirement
- Available in 24-pin DIP package, or a 28-pin surface mount PCC
- Improved pulse pairing (±1 ns max.)
- Handles RLL (1, 7) or (2, 7) data to 24 MB/s

ML8464B FEATURES

- Direct replacement for DP8464B

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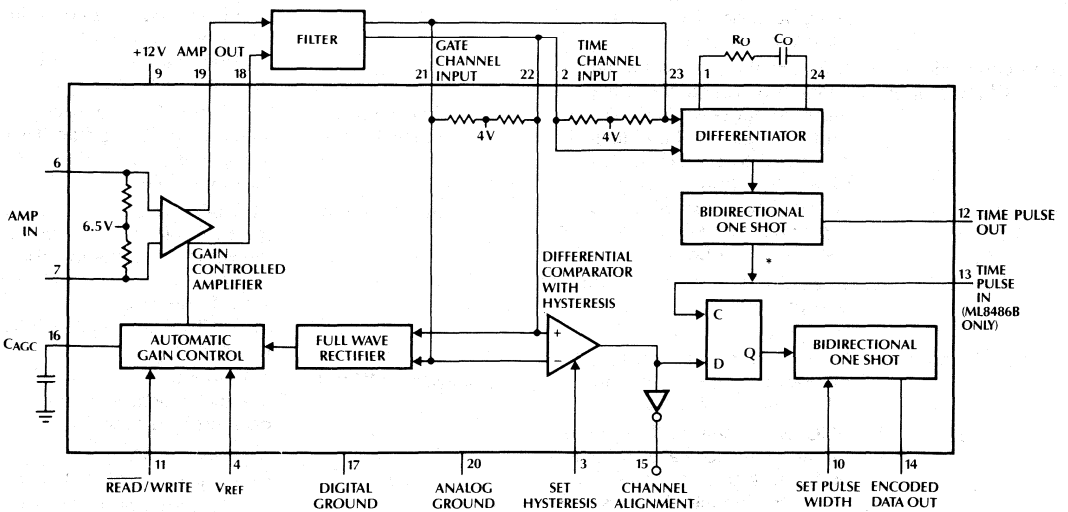
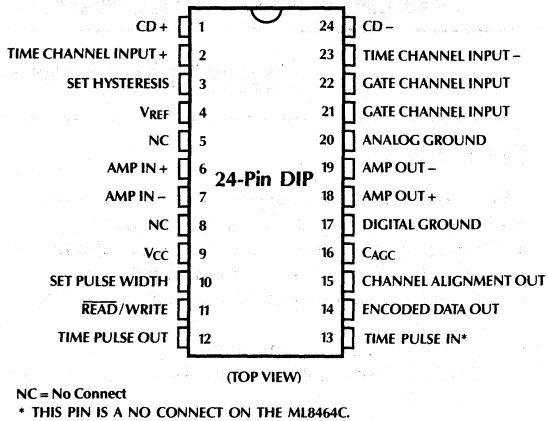
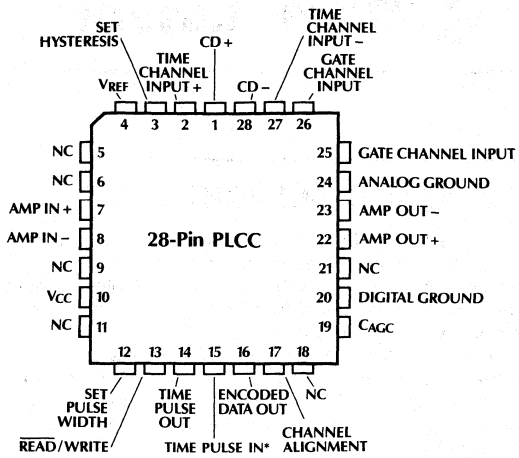
BLOCK DIAGRAM



PIN CONNECTIONS



NC = No Connect
* THIS PIN IS A NO CONNECT ON THE ML8464C.



PIN DESCRIPTION

NAME	FUNCTION
Amp In+, Amp In–	Differential inputs to the Amplifier. The output of the read/write head amplifier should be capacitively coupled to these pins.
Amp Out+, Amp Out–	Differential outputs of the Amplifier. These outputs should be capacitively coupled to the gating channel filter and to the time channel filter.
Gate Channel Inputs	Differential inputs to the AGC block and the gating channel. Must be capacitively coupled from the Amp Out.
Time Channel Input+, Time Channel Input–	Differential inputs to the time channel differentiator. A filter is required between these pins and Amp Out pins to band limit the noise and to correct for any phase distortion due to read circuitry. Also inputs must be capacitively coupled to prevent disturbing the DC input level.
CD+, CD–	External differentiator network is connected between these two pins.
Set Hysteresis	DC voltage on this pin sets the amount of hysteresis on the differential comparator.
V_{REF}	AGC circuit adjusts the gain of the amplifier to make the differential peak to peak voltage on the Gate Channel. Input is four times the DC voltage on this pin.
C_{AGC}	External capacitor between this pin and Analog ground is connected for the AGC.

NAME	FUNCTION
Set Pulse Width	External capacitor between this pin and Digital ground is connected to control the pulse width of the Encoded Data Out.
$\overline{\text{Read}}$/Write	TTL input. When low, the chip is in read mode and active. When High, the chip is forced into stand by mode.
Channel Alignment	Buffered output of the differential comparator with hysteresis. This output is TTL on the ML8464B, and is open emitter on ML8464C. The ML8464C is specified with a 2KΩ pull-down resistor to ground.
Time Pulse In (ML8464B only)	This is the TTL input to the clock of the D flip-flop. Usually it is connected to the Time Pulse Out pin.
Time Pulse Out	ML8464B: This is the TTL output from the bidirectional one shot following the differentiator. Usually it is connected to the Time Pulse In pin. ML8464C: Open emitter-follower test point.
Encoded Data Out	TTL output. Leading edge of this pin indicates the time position of the peaks.
V_{CC}	12V power supply.
GND	Digital ground. Digital signals should be referenced to this pin.
AGND	Analog ground. Analog signals should be referenced to this pin.

FUNCTIONAL DESCRIPTION

The output from the read/write amplifier is AC coupled to the amp input of the ML8464. The amplifier's output voltage is fed back via an external filter to an internal fullwave rectifier and compared against the external voltage on the V_{REF} pin. The AGC circuit adjusts the gain of the amplifier to make the peak to peak differential voltage on the Gate Channel Input four times the DC voltage on the V_{REF}. Typically the signal on the amp out will be set for $4V_{P-P}$ differential. Since the filter usually has a 6dB loss, the signal on the Gate Channel Input will be $2V_{P-P}$ differential. The user should therefore set 0.5V on V_{REF} which can be done with a simple voltage divider from the +12V supply or other suitable reference.

The peak detection is performed by feeding the output of the amplifier through an external filter to the differentiator. The differentiator output changes state when the input pulse changes direction, generally this will be at the peaks. However, if the signal exhibits shouldering, the differentiator will also respond to noise near the baseline. To avoid this problem, the signal is also fed to a gating channel which is used to define a level either side of the baseline. This gating channel is comprised of a differential comparator with hysteresis and a D flip-flop. The hysteresis for this comparator is externally set via the Set Hysteresis pin. In order to have data out, the input amplitude must first cross the hysteresis level which will change the logic level on the D input of the flip-flop. The peak of the input signal will generate a pulse out of the differentiator and bidirectional one shot. This pulse will clock the new data at the D input through to the output. In this way, when the differentiator is responding to noise at the baseline, the output of the D flip-flop is not changing since the logic level into the D input has not been changed. The comparator circuitry is therefore a gating channel which prevents any noise near the baseline from contaminating the data. The amount of hysteresis is twice the DC voltage on the Set Hysteresis pin. For instance, if the voltage on the Set Hysteresis pin is 0.3V, the differential AC signal across the gate channel input must be larger than 0.6V before the comparator will change states. In this case, the hysteresis is 30% of a 2V peak to peak differential signal at the gate channel input.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	14V
TTL Input Voltage	5.5V
TTL Output Voltage	5.5V
Input Voltage	5.5V
Differential Input Voltage	+3V
θ_{JA} for 24-Pin Plastic DIP (Copper Lead Frame)	60°C/Watt
θ_{JA} for 28-Pin PLCC (Copper Lead Frame)	60°C/Watt
Storage Temperature Range	–65°C to +150°C

Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

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DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions of T_A = 0 to 70°C, V_{CC} = 12.0V ± 10%, V_{REF} = 0.5V, Set Hysteresis = 0.3V, Read/Write = 0.8V unless otherwise noted. (All pin numbers refer to DIP package.)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
AMPLIFIER						
Z_{INAI}	Amp In Impedance	0.8	1.0	1.5	kΩ	
A_{VMIN}	Min Voltage Gain			6.0	V/V	AC Output $4V_{P-P}$ Differential
A_{VMAX}	Max Voltage Gain	180			V/V	AC Output $4V_{P-P}$ Differential
V_{CAGC}	Voltage on C_{AGC}	 2.8	4.5 3.4	5.5	V V	A_V = 6.0 A_V = 180
GATE CHANNEL						
Z_{INGCI}	Gate Channel Input Impedance	1.75	2.5	3.25	kΩ	
I_{CAGC^-}	Current that charges C_{AGC}	-1.5	-2.5	-3.5	mA	Pin 16 = 3.9V Pin 21 – Pin 22 = 1.3V
I_{CAGC^+}	Current that discharges C_{AGC}		1	5	μA	Pin 16 = 5.0V Pin 21 – Pin 22 = 0.7V
I_{VREF}	V_{REF} Input Bias Current		-0.01	-100	μA	
V_{THAGC}	AGC Threshold	0.88	1.0	1.12	V	Pin 16 = 4.2V See Note 1
I_{SH}	Set Hysteresis Bias Current		-60	-100	μA	
V_{THSH}	Set Hysteresis Threshold	0.48	0.6	0.72	V	See Note 2
TIME CHANNEL						
Z_{INTC}	Time Channel Input Impedance	3.5	5	6.5	kΩ	
I_{CD}	Current into pins 1 & 24 that discharges C_D	2.1	2.7	3.4	mA	
WRITE MODE						
Z_{INAI}	Amplifier Input Impedance in Write Mode	100		500	Ω	Pin 11 = 2V
I_{CAGC}	Pin 16 Current in Write Mode		1.0	5.0	μA	Pin 11 = 2V Pin 16 = 3.9V Pin 21 – Pin 22 = 1.3V
DIGITAL PINS						
V_{IH}	High Level Input Voltage	2.0			V	ML8464B: Pins 11, 13 ML8464C: Pin 11
V_{IL}	Low Level Input Voltage			0.8	V	
V_I	Input Clamp Voltage			-1.5	V	V_{CC} = 10.8V, I_I = -18mA
I_{IH}	High Level Input Current			20	μA	V_{CC} = 13.2V, V_I = 2.7V
I_I	Input Current at Maximum Input Voltage			1	mA	V_{CC} = 13.2V, V_I = 5.5V
I_{IL}	Low Level Input Current			-200	μA	V_{CC} = 13.2V, V_I = 0.5V
V_{OH}	High Level Output Voltage	2.4			V	V_{CC} = 10.8V, V_{IOH} = -40μA See notes 3, 7
V_{OL}	Low Level Output Voltage			0.5	V	V_{CC} = 10.8V, I_{OL} = 800μA, see note 7
I_{OSC}	Output Short Circuit Current			-100	mA	V_{CC} = 13.2V, V_O = 0V
I_{CC}	Supply Current		54	75	mA	V_{CC} = 13.2V

DC ELECTRICAL CHARACTERISTICS (Continued)

Over recommended operating conditions of T_A = 0 to 70°C, V_{CC} = 12.0V ± 10%, V_{REF} = 0.5V, Set Hysteresis = 0.3V, Read/Write = 0.8V unless otherwise noted. (All pin numbers refer to DIP package.)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
DIGITAL PINS (Continued)						
V_{OHCA}	Channel Alignment Pin V_{OH}					(Note 3)
	ML8464B	2.4			V	I_{OH} = –40μA
	ML8464C		1.6		V	2kΩ Load to GND
V_{OLCA}	Channel Alignment Pin V_{OL}					(Note 3)
	ML8464B			0.4	V	I_{OL} = 800μA
	ML8464C		1.0		V	2kΩ Load to GND
V_{OHTP}	Time Pulse Out Pin V_{OH}					
	ML8464B	2.4			V	10kΩ Load to GND
	ML8464C		9.6		V	10kΩ Load to GND
V_{OLTP}	Time Pulse Out Pin V_{OL}					
	ML8464B			0.4	V	10kΩ Load to GND
	ML8464C		8.6		V	10kΩ Load to GND

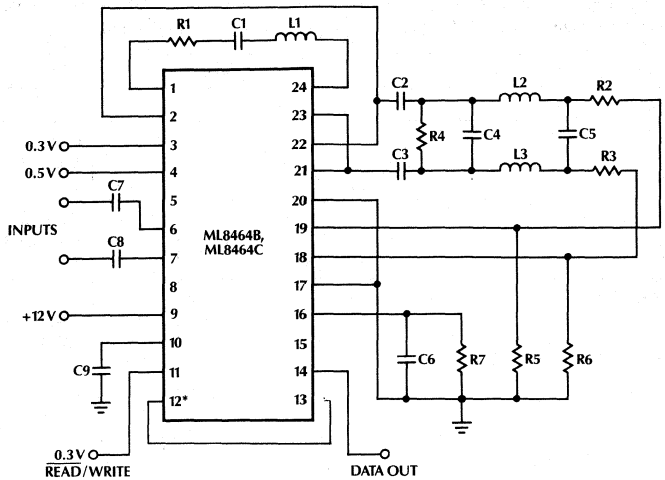
AC ELECTRICAL CHARACTERISTICS

Over recommended operating temperature and supply range of V_{CC} = 10.8 to 13.2V, T_A = 0 to 70°C.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
ML8464-1						
t_{P-P}	Pulse Pairing		±0.5	±1.0	ns	
ML8464-1.5						f = 2.5MHz
t_{P-P}	Pulse Pairing[6]		±0.8	±1.5	ns	V_{IN} = 40mV_{P-P} differential
ML8464-2						See note 4
t_{P-P}	Pulse Pairing		±1.5	±3.0	ns	

Note 1: The AGC threshold is defined as the voltage across the gate channel input when the voltage on C_{AGC} is 4.2V.
Note 2: The Set Hysteresis threshold is defined as the voltage across the gate channel input when the channel alignment output voltage changes state.
Note 3: To prevent inductive coupling from the digital outputs to amplifier inputs, the TTL outputs should not drive more than one ALS TTL load.
Note 4: The filter and differentiator network are described in the pulse pairing set-up.
Note 5: All limits are guaranteed by 100% testing or alternate methods.
Note 6: The 1.5 ns pulse pairing specification is available only on the ML8464C, not the ML8464B.
Note 7: ML8464B: Pins 12, 14, 15
ML8464C: Pins 14 and 15 only.

5



PULSE PAIRING SET UP

PARTS LIST

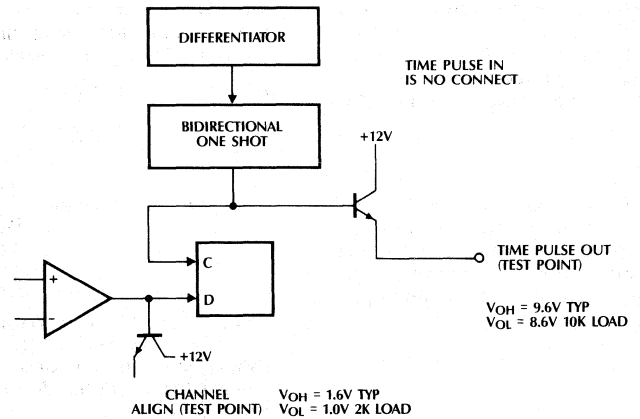
R1	220Ω	C1	82pF
R4	680Ω	C2, C3, C6	0.01μF
R2, R3	240Ω	C4	100pF
R5, R6	3.3kΩ	C5	15pF
R7	100kΩ	C7, C8	0.0022μF
L1	1.5μH	C9	47pF
L2, L3	4.7μH		

* The connection between pins 12 and 13 is required only for the ML8464B.

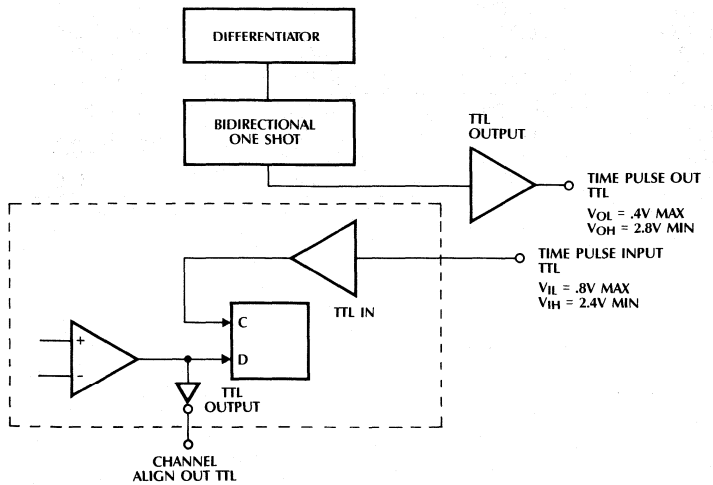
PULSE PAIRING MEASUREMENT

The scope probe is connected to pin 14 (Encoded Data Out) and triggered off of its positive edge. The trigger holdoff is adjusted so that the scope first triggers off the pulse associated with the positive peak and then off the pulse associated with the negative peak. Pulse pairing is displayed on the second pair of pulses on the display. If the second pair of pulses are separated by 6ns, then the pulse pairing for the part is ±3ns.

ML8464C



ML8464B



DIFFERENCES BETWEEN ML8464C AND ML8464B

THE EXTERNAL DELAY

The ML8464B open circuits the digital signal at pins 12 and 13. This allows for the insertion of an external delay filter. The ML8464C has no TTL buffers at these pins and closes the signal path internally bringing out a test point at pin 12. Hence, the ML8464 does not allow for the external delay.

TEST POINTS

The ML8464B has two TTL test points at pins 12 and 15. The ML8464C uses open emitter followers in an ECL configuration. Hence, the voltage levels are not similar at pins 12 and 15 on both devices. The typical voltage level at pins 12 are V_{OH} = 9.6V, V_{OL} = 8.6V and at pin 15 are V_{OH} = 1.6V, V_{OL} = 1.0V.

AGC GAIN CONTROL FACTOR

The AGC reference level is a DC voltage externally set at V_{REF} (pin 4). Increasing this DC voltage will increase the gain of the gain controlled amplifier.

AGC gain control factor =

$$\frac{V_{OUT\ PEAK} = \text{peak of the AGC amp}}{V_{REF}}$$

$$\text{AGC gain control factor} = \frac{2.5V_{PP}}{0.5V_{DC}} = 5 \text{ for ML8464B}$$

$$= \frac{2.0V_{PP}}{0.5V_{DC}} = 4 \text{ for ML8464C}$$

Thus, at V_{REF} = $0.5V_{DC}$, V_{OUT} AGC = 2.5V for ML8464B and 2.0V for ML8464C. This smaller signal amplitude should be taken into consideration at the hysteresis comparator. To set the desired amount of hysteresis, and external DC control voltage is used. The particular settings for V_{REF} and control voltage at pin 3 that optimizes the ML8464B performance may not necessarily optimize the ML8464C performance.

ORDERING INFORMATION

ORDERING NUMBER	PACKAGE	PIN COUNT	TEMPERATURE RANGE	PULSE PAIRING
ML8464C-1CP	Plastic DIP	24 Pins	0° to 70°C	±1ns
ML8464C-1CQ	PLCC	28 Pins	0° to 70°C	±1ns
ML8464C-1.5CP	Plastic DIP	24 Pins	0° to 70°C	±1.5ns
ML8464C-1.5CQ	PLCC	28 Pins	0° to 70°C	±1.5ns
ML8464C-2CP	Plastic DIP	24 Pins	0° to 70°C	±3ns
ML8464C-2CQ	PLCC	28 Pins	0° to 70°C	±3ns
ML8464B-1CP	Plastic DIP	24 Pins	0° to 70°C	±1ns
ML8464B-1CQ	PLCC	28 Pins	0° to 70°C	±1ns
ML8464B-2CP	Plastic DIP	24 Pins	0° to 70°C	±3ns
ML8464B-2CQ	PLCC	28 Pins	0° to 70°C	±3ns

Power Supply ICs

Section 6

Power Supplies
Selection Guide

Micro Linear offers high performance Switch Mode Power Supply IC controllers for PWM, Resonant and Power Factor Correction. These PWM IC's are the highest frequency IC's available and include unique features for enhanced stability, easy synchronization and improved fault management. These controller IC's can be tailored to meet your unique design requirements using Micro Linear's array-based Semi-Standard capability.

For Power Factor Correction, three IC's are available to meet the needs of a variety of different applications. Boost and Buck Boost dedicated PFC control IC's are available. Also, a new IC, the ML4819, combines a boost PFC stage with a Current Mode PWM control section. This new "Combo" controller is the first IC available which controls an entire PFC corrected power supply on a single chip.

Two new resonant controllers are now available, one for zero voltage switching and one multi-mode controller. Both IC's offer unique overload protection features, high current output drivers, and low cross conduction. The multi-mode controller supports both series resonant converters operating above resonance and ZCS topologies.

A new phase modulating soft switching controller, the ML4818 is also available. This new topology combines the low dynamic losses of resonant switching with the advantages of square wave PWM's low conduction losses and energy transfer efficiency.

These IC's are available in Commercial (0°C to 70°C), Industrial (–40°C to +85°C) and Military (–55°C to +125°C) temperature ranges in both DIP and Surface Mount packages.

POWER FACTOR CONTROLLERS

- **ML4812 General Purpose Boost Mode**
- **ML4813 Flyback Converter for Low Power Systems**
- **ML4819 Boost PFC and PWM "Combo"**

PULSE WIDTH MODULATION IC's

- 1 MHz Operation
- Voltage Mode or Current Mode Operation
- High Current (2A peak) High Speed Totem Pole Outputs
- Precision (+1%) 5.1V Reference
- Soft Start Latch Ensures Full Soft Start Cycle

HIGH FREQUENCY RESONANT CONTROLLERS

ML4815 Single Ended Zero Voltage Switching Controller

- Ideal for Low Input Voltage DC to DC Converter Modules
- Operation to 1.5MHz

ML4816 Multi-Mode Push-Pull Resonant Controller

- Supports All Major Topologies: ZVS and ZCS
- Constant Off-Time or Constant On-Time Control

ML4818 Phase Modulation Soft Switching Controller

- Four 2A Totem Pole Outputs
- Zero Voltage Switching
- Integrating Fault Detection

PWM CONTROLLER SELECTION GUIDE

FEATURE	ML4809	ML4810	ML4811	ML4817	ML4823	ML4825
Push/Pull	X	X	X			X
Single Ended				X	X	
Integrating Fault Detection		X	X			
Reset Delay			X	X		
OVP Comparator			X			
Precise Duty Cycle Limit				X		
Oscillator Sync Input			X			
VCO	X					
Blanker	X					
Slope Compensation	X					
Separate Error Amp	X					

Micro Linear

ML1825

High Frequency Power Supply Controller

GENERAL DESCRIPTION

The ML1825 High Frequency PWM Controller is an IC controller optimized for use in Switch Mode Power Supply designs running at frequencies to 1MHz. Propagation delays are minimal through the comparators and logic for reliable high frequency operation while slew rate and bandwidth are maximized on the error amplifier. This controller is designed to work in either voltage or current mode and provides for input voltage feed forward.

A 1V threshold current limit comparator provides cycle-by-cycle current limit while exceeding a 1.4V threshold initiates a soft-start cycle. The soft start pin doubles as a maximum duty cycle clamp. All logic is fully latched to provide jitter-free operation and prohibit multiple pulsing. An under-voltage lockout circuit with 800mV of hysteresis assures low startup current and drives the outputs low.

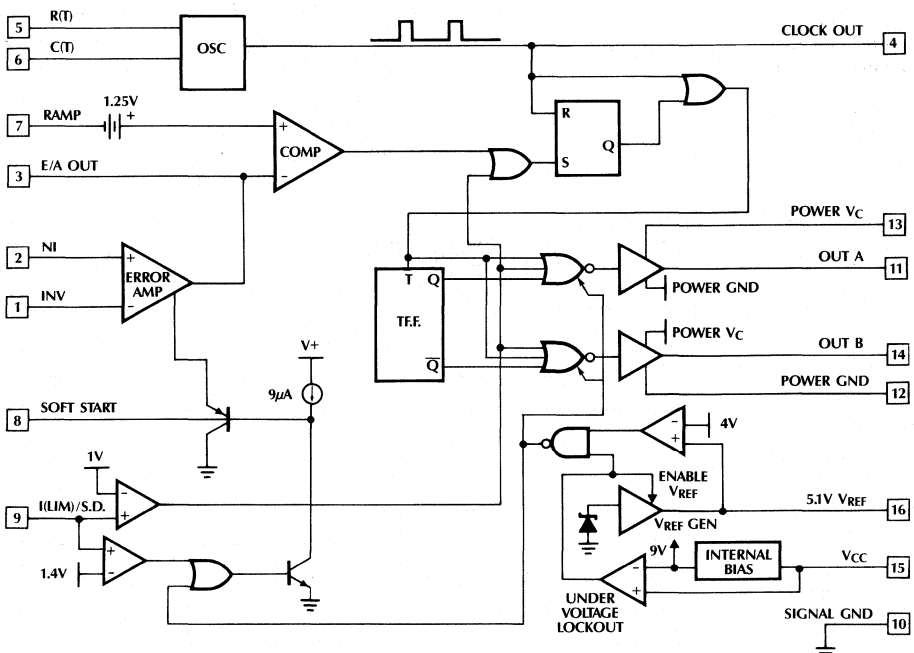
The ML1825 is fabricated on a 40V bipolar process from the FB3480 Power Supply Controller Array. Customized versions of this controller are therefore easily implemented. Please refer to the FB3480 datasheet for more information.

This controller is a pin for pin replacement for the UC1825 controller.

FEATURES

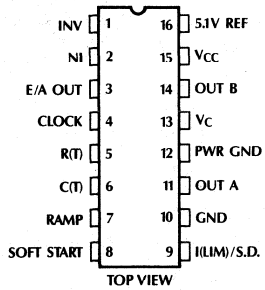
- Practical Operation at Switching Frequencies to 1.0MHz
- High Current (2A peak) Dual Totem Pole Outputs
- Wide Bandwidth Error Amplifier
- Fully Latched Logic with Double Pulse Suppression
- Pulse-by-Pulse Current Limiting
- Soft Start and Max. Duty Cycle Control
- Under Voltage Lockout with Hysteresis
- 5.1V, ±1% Trimmed Bandgap Reference
- Pin Compatible Replacement for UC1825

BLOCK DIAGRAM



PIN CONNECTION

ML1825
16-Pin DIP



PIN DESCRIPTION

PIN #	NAME	FUNCTION
1	INV	Inverting input to error amp.
2	NI	Non-inverting input to error amp.
3	E/A OUT	Output of error amplifier and input to main comparator.
4	CLOCK	Oscillator output.
5	R(T)	Timing Resistor for Oscillator — sets charging current for oscillator timing capacitor (pin 6).
6	C(T)	Timing Capacitor for Oscillator.
7	RAMP	Non-Inverting input to main comparator. Connected to C(T) for Voltage Mode operation or to current sense resistor for current mode.
8	SOFT START	Normally connected to Soft Start Capacitor.
9	I(LIM)/S.D.	Current limit sense pin. Normally connected to current sense resistor.
10	GND	Analog Signal Ground.
11	OUT A	High Current Totem pole output. This output is the first one energized after Power On Reset.
12	PWR GND	Return for the High Current Totem pole outputs.
13	V_C	Positive Supply for the High Current Totem pole outputs.
14	OUT B	High Current Totem pole output.
15	V_{CC}	Positive Supply for the IC.
16	5.1V REF	Buffered output for the 5.1V voltage reference.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (Pins 15, 13) 30V
Output Current, Source or Sink (Pins 11, 14)
  DC 0.5A
  Pulse (0.5μs) 2.0A
Analog Inputs
  (Pins 1, 2, 7) ..... –0.3V to 7V
  (Pins 9, 8) ..... –0.3V to 6V
Clock Output Current (Pin 4) ..... –5mA
Error Amplifier Output Current (Pin 3) 5mA
Soft Start Sink Current (Pin 8) 20mA
Oscillator Charging Current (Pin 5) ..... –5mA
Junction Temperature
  ML4825M ..... 150°C
  ML4825I, ML4825C ..... 125°C
Storage Temperature Range ..... –65°C to +150°C
Lead Temperature (Soldering 10 sec.) ..... +260°C
Thermal Resistance (θ_{JA})
  Ceramic DIP ..... 65°C/W

OPERATING CONDITIONS

Temperature Range
  ML1825M ..... –55°C to +125°C

Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, R_T = 3.65KΩ, C_T = 1000pF, T_A = Operating Temperature Range, V_{CC} = 15V.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Oscillator					
Initial Accuracy	T_J = 25°C, (note 1)	360	400	440	KHz
Voltage Stability	10V < V_{CC} < 30V, (note 1)		0.2	2	%
Temperature Stability	(note 1)		5		%
Total Variation	line, temp, (note 1)	340		460	KHz
Clock Out High		3.9	4.5		V
Clock Out Low			2.3	2.9	V
Ramp Peak	(note 1)	2.6	2.8	3.0	V
Ramp Valley	(note 1)	0.7	1.0	1.25	V
Ramp Valley to Peak	(note 1)	1.6	1.8	2.0	V
Reference Section					
Output Voltage	T_J = 25°C, I_O = 1mA	5.05	5.10	5.15	V
Line Regulation	10V < V_{CC} < 30V		2	20	mV
Load Regulation	1mA < I_O < 10mA		5	20	mV
Temperature Stability	–55°C < T_J < 150°C, (note 1)		.2	.4	%
Total Variation	line, load, temp (note 1)	5.0		5.20	V
Output Noise Voltage	10Hz to 10KHz		50		μV
Long Term Stability	T_J = 125°C, 1000 hrs, (note 1)		5	25	mV
Short Circuit Current	V_{REF} = 0V	–15	–50	–100	mA
Error Amplifier Section					
Input Offset Voltage				10	mV
Input Bias Current			.6	3	μA
Input Offset Current			.1	1	μA
Open Loop Gain	1 < V_O < 4V	60	95		dB

ELECTRICAL CHARACTERISTICS (Continued)

Unless otherwise specified, R_T = 3.65KΩ, C_T = 1000pF, T_A = Operating Temperature Range, V_{CC} = 15V.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Error Amplifier Section (Continued)					
CMRR	$1.5 < V_{CM} < 5.5V$	75	95		dB
PSRR	$10 < V_{CC} < 30V$	85	110		dB
Output Sink Current	$V_{PIN\ 3}$ = 1V	1	2.5		mA
Output Source Current	$V_{PIN\ 3}$ = 4V	-.5	-1.3		mA
Output High Voltage	$I_{PIN\ 3}$ = -0.5mA	4.0	4.7	5.0	V
Output Low Voltage	$I_{PIN\ 3}$ = 1mA	0	0.5	1.0	V
Unity Gain Bandwidth	(note 1)	3	5.5		MHz
Slew Rate	(note 1)	6	12		V/μs
PWM Comparator Section					
Pin 7 Bias Current	$V_{PIN\ 7}$ = 0V		-1	-5	μA
Duty Cycle Range		0		80	%
Pin 3 Zero DC Threshold	$V_{PIN\ 7}$ = 0V	1.1	1.25		V
Delay to Output	(note 1)		50	80	ns
Soft-Start Section					
Charge Current	$V_{PIN\ 8}$ = 0.5V	3	9	20	μA
Discharge Current	$V_{PIN\ 8}$ = 1V	1			mA
Current Limit/Shutdown Section					
Pin 9 Bias Current	$0V < V_{PIN\ 9} < 4V$			+15	μA
Current Limit Threshold		.9	1	1.1	V
Shutdown Threshold		1.25	1.4	1.55	V
Delay to Output	(note 1)		50	80	ns
Output Section					
Output Low Level	I_{OUT} = 20mA		.25	.4	V
	I_{OUT} = 200mA		1.2	2.2	V
Output High Level	I_{OUT} = -20mA	13.0	13.5		V
	I_{OUT} = -200mA	12.0	13.0		V
Collector Leakage	V_C = 30V		100	500	μA
Rise/Fall Time	C_L = 1000pF, (note 1)		30	60	ns
Under-Voltage Lockout Section					
Start Threshold		8.8	9.2	9.6	V
UVLO Hysteresis		.4	.8	1.2	V
Supply Current					
Start Up Current	V_{CC} = 8V		1.1	2.5	mA
I_{CC}	$V_{PIN\ 1,\ 7,\ 9}$ = 0V, $V_{PIN\ 2}$ = 1V,		22	33	mA

Note 1: This parameter not 100% tested in production but guaranteed by design.

FUNCTIONAL DESCRIPTION

OSCILLATOR

The ML1825 oscillator charges the external capacitor (C_T) with a current (I_{SET}) equal to $3/R_{SET}$. When the capacitor voltage reaches the upper threshold (Ramp Peak), the comparator changes state and the capacitor discharges to the lower threshold (Ramp Valley) through Q1. While the capacitor is discharging, Q2 provides a high pulse.

The Oscillator period can be described by the following relationship:

$$T_{OSC} = T_{RAMP} + T_{DEADTIME}$$

where: $T_{RAMP} = C$ (Ramp Valley to Peak)/I_{SET}

and: $T_{DEADTIME} = C$ (Ramp Valley to Peak)/I_{Q1}

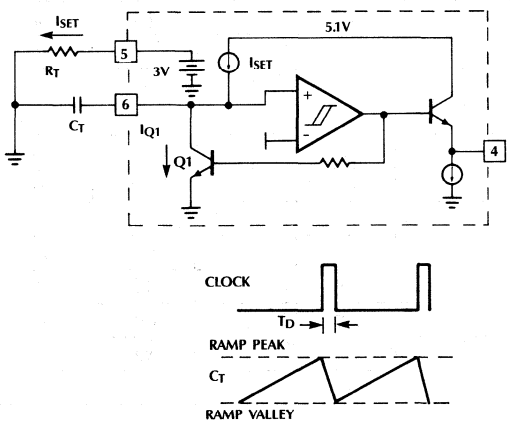


Figure 1. Oscillator Block Diagram

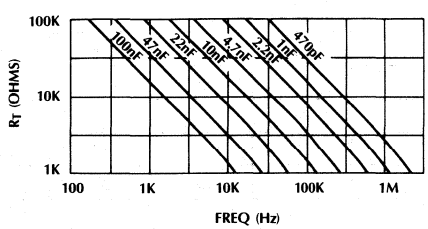


Figure 2. Oscillator Timing Resistance vs Frequency

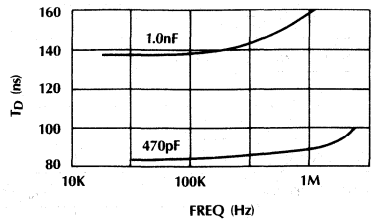


Figure 3. Oscillator Deadtime vs Frequency

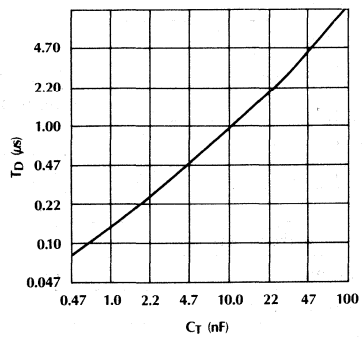


Figure 4. Oscillator Deadtime vs C(T) (3KΩ ≤ R(T) ≤ 100KΩ)

ERROR AMPLIFIER

The ML1825 error amplifier is a 5.5MHz bandwidth 12V/µs slew rate op-amp with provision for limiting the positive output voltage swing (Output Inhibit line) for ease in implementing the soft start function.

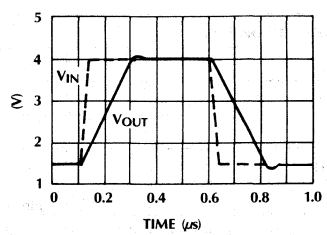


Figure 5. Unity Gain Slew Rate

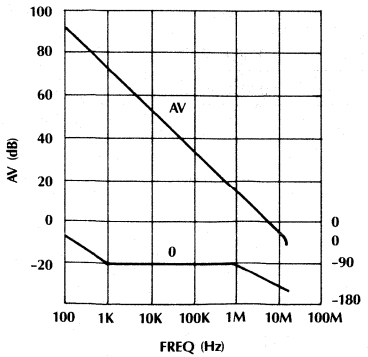


Figure 6. Open Loop Frequency Response

OUTPUT DRIVER STAGE

The ML1825 Output Driver is a 2A peak output high speed totem pole circuit designed to quickly switch the gates of capacitive loads, such as power MOSFET transistors.

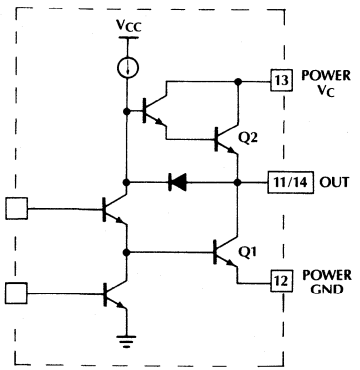


Figure 7. Simplified Schematic

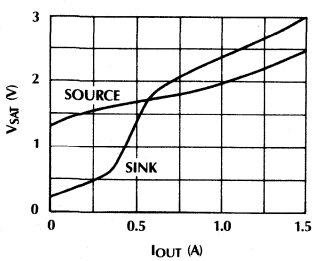


Figure 8. Saturation Curves

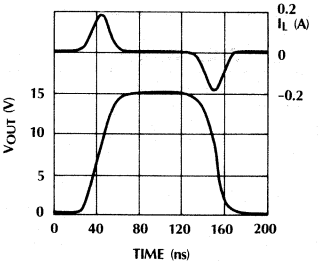


Figure 9. Rise/Fall Time (C_L = 1000pF)

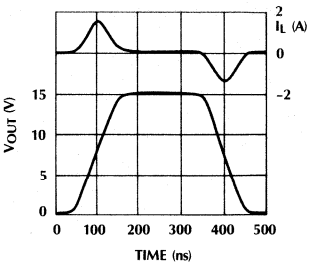


Figure 10. Rise/Fall Time (C_L = 10,000pF)

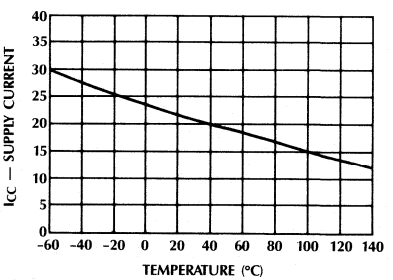


Figure 11. Supply Current vs Temperature

SOFT START AND CURRENT LIMIT

The ML1825 employs two current limits. When the voltage at pin 9 exceeds 1V, the outputs are immediately shut off and the cycle is terminated for the remainder of the oscillator period by resetting the RS flip flop.

If the output current is rising quickly such that the voltage on pin 9 reaches 1.4V before the outputs have turned off, a soft start cycle is initiated and the soft start capacitor (pin 8) is discharged. The duty cycle on start up is limited by limiting the output voltage of the error amplifier voltage to the voltage at pin 8.

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ML1825MJ	–55°C to +125°C	Hermetic DIP

ML4809

High Frequency PWM Controller

GENERAL DESCRIPTION

The ML4809 High Frequency PWM Controller is a full-featured IC controller optimized for use in Switch Mode Power Supply designs running at frequencies to 1MHz. Propagation delays are minimized while slew rate and bandwidth are maximized for reliable high frequency operation. This controller is designed to work in either voltage or current mode and provides for input voltage feed forward.

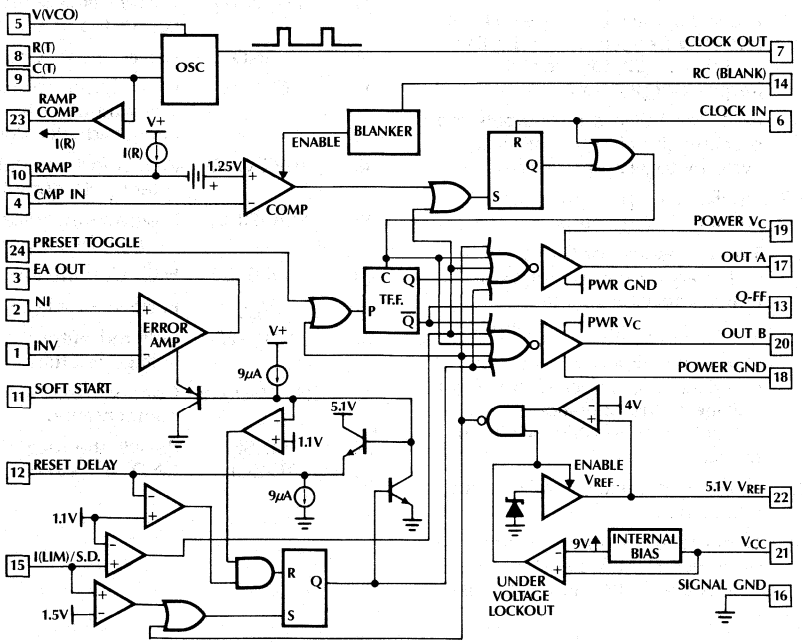
A 1.1V threshold current limit comparator provides cycle-by-cycle current limit while exceeding a 1.5V threshold initiates a soft-start cycle. The soft start pin doubles as a maximum duty cycle clamp. All logic is fully latched to provide jitter-free operation and prohibit multiple pulsing. An under-voltage lockout circuit with 7V of hysteresis assures low startup current and drives the outputs low.

The ML4809 is fabricated on a 40V bipolar process from the FB3480 Power Supply Controller Array. Customized versions of this controller are easily implemented. This controller is similar to the UC1825 controller, however the ML4809 includes many features not found on the 1825. These features are set in *Italics.*

FEATURES

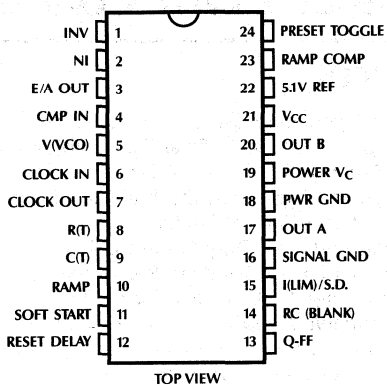
- Practical Operation at Switching Frequencies to 1.0MHz
- High Current (2A peak) Dual Totem Pole Outputs
- Wide Bandwidth Error Amplifier
- Fully Latched Logic with Double Pulse Suppression
- Pulse-by-Pulse Current Limiting
- Soft Start and Max. Duty Cycle Control
- 5.1V, ±1% Trimmed Bandgap Reference
- *Under Voltage Lockout: 16V Start with 7V Hysteresis*
- *Programmable Ramp Compensation Circuit*
- *VCO Input for Synchronization or Frequency Control*
- *External Clock Input for Synchronization*
- *Toggle Preset for Synchronization*
- *Comparator Blanker for Better Noise Immunity/Stability*
- *Separate Error Amplifier Output Pin for Loop Filtering Versatility*
- *Fast Shut Down Path from Current Limit to Outputs*
- *Outputs Preset to Known Condition After Under Voltage Lockout*
- *Soft Start Latch Ensures Full Soft Start Cycle*
- *Programmable Soft Start Delay*

BLOCK DIAGRAM



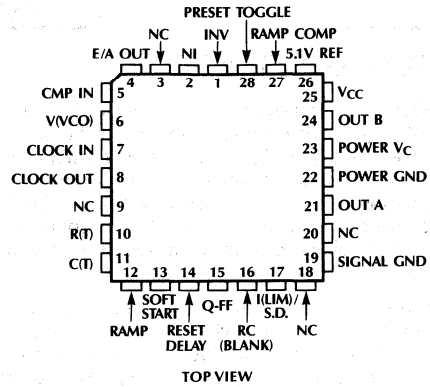
PIN CONNECTIONS

ML4809
24-Pin DIP



TOP VIEW

ML4809
28-Pin PCC



TOP VIEW

PIN DESCRIPTION

PIN #	NAME	FUNCTION
1	INV	Inverting input to error amp.
2	NI	Non-inverting input to error amp.
3	E/A OUT	Output of error amplifier.
4	CMP IN	Main Comparator Input.
5	V(VCO)	A control voltage input which sets the VCO frequency. May be tied to 5.1V REF (22) for fixed frequency operation.
6	CLOCK IN	A "1" level blanks the outputs and prepares the chip for the next cycle by toggling the T flip flop.
7	CLOCK OUT	Oscillator output. This is an emitter follower output.
8	R(T)	Timing Resistor for Oscillator — sets charging current for oscillator timing capacitor (pin 9).
9	C(T)	Timing Capacitor for Oscillator.
10	RAMP	Non-Inverting input to main comparator. Connected to C(T) for Voltage Mode operation or to current sense resistor for current mode.
11	SOFT START	Normally connected to Soft Start Capacitor.
12	RESET DELAY	Connect to capacitor for time delay before new soft-start cycle begins after 1.4V current limit is reached.
13	Q-FF	An Emitter Follower output which is High for B active.
14	RC (BLANK)	Connect resistor and capacitor to ground for blanker function.
15	I(LIM)/S.D.	Current limit sense pin. Normally connected to sense resistor.
16	GND	Analog Signal Ground.
17	OUT A	High Current Totem pole output. This output is the first one energized after Power On Reset.
18	PWR GND	Return for the High Current Totem pole outputs.
19	POWER V_C	Positive Supply for the High Current Totem pole outputs.
20	OUT B	High Current Totem pole output.
21	V_{CC}	Positive Supply for the IC.
22	5.1V REF	Buffered output for the 5.1V voltage reference.
23	RAMP COMP	Connect resistor to GND for ramp compensation.
24	PRESET TOGGLE	Presets the toggle flip-flop. Tie to GND to disable.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (Pins 21, 19) 36V
Output Current, Source or Sink (Pins 17, 20)
DC 0.5A
Pulse (0.5μs) 2.0A
Input Voltage
(Pins 1, 2, 4, 5, 10) ..... -0.3V to 7V
(Pins 8, 9, 11, 12, 15, 24) ..... -0.3V to 6V
Logic Output Current (Pins 7, 13) ..... -5mA
Blanker Charge Current (Pin 14) ..... -5mA
Error Amplifier Output Current (Pin 3) 5mA
Soft Start Sink Current (Pin 11) 20mA
Oscillator Charging Current (Pin 8) ..... -5mA
Junction Temperature
ML4809M ..... 150°C
ML4809I, ML4809C ..... 125°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering 10 sec.) ..... +260°C

Thermal Resistance (θ_{JA})
Plastic DIP ..... 50°C/W
Ceramic DIP ..... 55°C/W
Plastic Chip Carrier (PCC) ..... 55°C/W

OPERATING CONDITIONS

Temperature Range
ML4809M ..... -55°C to +125°C
ML4809I ..... -40°C to +85°C
ML4809C ..... 0°C to +70°C

Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, R_T = 6.2KΩ, C_T = 1000pF, V(VCO) = V_{REF}, R_L (Pins 7, 13) = 5KΩ, T_A = Operating Temperature Range, V_{CC} = 15V. (note 3)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
Oscillator						
Initial Accuracy		T_J = 25°C, (note 1)	360	400	440	KHz
Voltage Stability		10V < V_{CC} < 30V, (note 1)		0.2	2	%
Temperature Stability		(note 1)			5	%
Total Variation		line, temp, (note 1)	340		460	KHz
Clock Out High			3.9	4.5		V
Clock Out Low				2.3	2.9	V
Ramp Peak		(note 1)	2.6	2.8	3.0	V
Ramp Valley		(note 1)	0.7	1.0	1.25	V
Ramp Valley to Peak		(note 1)	1.6	1.8	2.0	V
V(VCO) Control Range			1		5.5	V
Reference Section						
Output Voltage	ML4809C	T_J = 25°C, I_O = 1mA	5.00	5.10	5.20	V
	ML4809M, ML4809I		5.05	5.10	5.15	V
Line Regulation		10V < V_{CC} < 30V		2	20	mV
Load Regulation		1mA < I_O < 10mA		5	20	mV
Temperature Stability		-55°C < T_J < 150°C, (note 1)		.2	.4	mV/°C
Total Variation	ML4809C	line, load, temp, (note 1)	4.95		5.25	V
	ML4809M, ML4809I		5.0		5.20	V
Output Noise Voltage		10Hz to 10KHz		50		μV
Long Term Stability		T_J = 125°C, 1000 hrs, (note 1)		5	25	mV
Short Circuit Current		V_{REF} = 0V	-15	-50	-100	mA
Under-Voltage Lockout Section						
Start Threshold			15	16	17	V
UVLO Hysteresis			6.5	7	7.5	V

ELECTRICAL CHARACTERISTICS (Continued)

Unless otherwise specified, R_T = 6.2KΩ, C_T = 1000pF, V(VCO) = V_{REF}, R_L (Pins 7, 13) = 5KΩ, T_A = Operating Temperature Range, V_{CC} = 15V. (note 3)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
Error Amplifier Section						
Input Offset Voltage	ML4809C				15	mV
	ML4809M, ML4809I				10	mV
Input Bias Current				.6	3	μA
Input Offset Current				.1	1	μA
Open Loop Gain		$1 < V_O < 4V$	60	96		dB
CMRR		$1.5 < V_{CM} < 5.5V$	75	95		dB
PSRR		$10 < V_{CC} < 30V$	80	110		dB
Output Sink Current		$V_{PIN\ 3}$ = 1V	1	2.5		mA
Output Source Current		$V_{PIN\ 3}$ = 4V	-.5	-1.3		mA
Output High Voltage		$I_{PIN\ 3}$ = -0.5mA	4.0	4.7	5.0	V
Output Low Voltage		$I_{PIN\ 3}$ = 1mA	0	0.5	1.0	V
Unity Gain Bandwidth		(note 1)	3	5.5		MHz
Slew Rate		(note 1)	6	12		V/μs
PWM Comparator Section						
Pin 10 Bias Current		$V_{PIN\ 10}$ = 0V, $V_{PIN\ 23}$ = open, $V_{PIN\ 9}$ = 2V		-1	-5	μA
Duty Cycle Range			0		75	%
Pin 4 Zero DC Threshold		$V_{PIN\ 7}$ = 0V	1.1	1.25		V
Delay to Output		(note 1)		50	80	ns
Ramp Compensation						
Pin 10 Current		$V_{PIN\ 9}$ = 2V, $R_{PIN\ 23}$ = 6.8KΩ	265	295	325	μA
Soft-Start/Reset Delay Section						
Charge Current (Pin 11)		$V_{PIN\ 11}$ = 0.5V	3	9	20	μA
Discharge Current (Pin 11)		$V_{PIN\ 11}$ = 1V	1			mA
Discharge Current (Pin 12)		$V_{PIN\ 12}$ = 1V	3	9	20	μA
Charge Current (Pin 11)		$V_{PIN\ 12}$ = 0.5V	1			mA
Current Limit/Shutdown Section						
Pin 15 Bias Current	ML4809C	$0V < V_{PIN\ 15} < 4V$			+15	μA
	ML4809M, ML4809I	$0V < V_{PIN\ 15} < 4V$			+10	μA
Current Limit Threshold			1.0	1.1	1.2	V
Shutdown Threshold			1.35	1.50	1.65	V
Delay to Output		(note 1)		40	70	ns
Blanker Section						
T_{BLANK}		(note 1), RC = 5.1KΩ, 68pF	80	100	120	ns

ELECTRICAL CHARACTERISTICS (Continued)

Unless otherwise specified, R_T = 6.2KΩ, C_T = 1000pF, V(VCO) = V_{REF}, R_L (Pins 7, 13) = 5KΩ, T_A = Operating Temperature Range, V_{CC} = 15V. (note 3)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Output Section					
Output Low Level	I_{OUT} = 20mA		.25	.4	V
	I_{OUT} = 200mA		1.2	2.2	V
Output High Level	I_{OUT} = -20mA	13.0	13.5		V
	I_{OUT} = -200mA	12.0	13.0		V
Collector Leakage	V_C = 30V		100	500	μA
Rise/Fall Time	C_L = 1000pF, (note 1)		30	60	ns
Logic Inputs/Outputs					
Pin 24 Threshold	(note 2)		V_{REF} - .98		V
Pin 13 V_{OH}	(note 2)		V_{REF} - .65		V
Pin 13 V_{OL}	(note 2)		V_{REF} - 1.3		V
Supply Current					
Start Up Current	V_{CC} = 8V		1.1	2.5	mA
I_{CC}	$V_{PIN\ 1,\ 10,\ 15}$ = 0V, $V_{PIN\ 2}$ = 1V, T_A = 25°C		29	38	mA

Note 1: This parameter not 100% tested in production but guaranteed by design.

Note 2: The thresholds on the logic input pins are set by a reference generator that is: $V_{TH} = V_{REF} - (1.5 * V_{BE})$. The logic outputs swing from: $V_{OH} = V_{REF} - V_{BE}$ to $V_{OL} = V_{REF} - 2 * V_{BE}$. V_{BE} is nominally .65V and varies with temperature. Logic inputs and outputs will track each other with temperature variation.

Note 3: Since the Under Voltage Lockout start-up threshold is 16V, the supply is first raised to 20V to activate the IC and then lowered to 15V to conduct the electrical testing.

FUNCTIONAL DESCRIPTION

OSCILLATOR

The ML4809 Voltage Controlled Oscillator charges the external capacitor (C_T) with a current (I_{CHARGE}) equal to V(VCO)/R_T. When the capacitor voltage reaches the upper threshold (Ramp Peak), the comparator changes state and the capacitor discharges to the lower threshold (Ramp Valley) through Q1. While the capacitor is discharging, Q2 provides a high pulse. For Fixed Frequency Operation, V(VCO) can be tied to V_{REF}.

The Oscillator period can be described by the following relationship:

$$T_{OSC} = T_{RAMP} + T_{DEADTIME}$$

where: T_{RAMP} = C (Ramp Valley to Peak)/I_{CHARGE}

and: $T_{DEADTIME}$ = C (Ramp Valley to Peak)/I_{DIS}

An approximate expression for the oscillator frequency in fixed frequency operation (where V(VCO) = V_{REF}) is:

$$F_{OSC} \approx \frac{2.48}{R_T C_T}$$

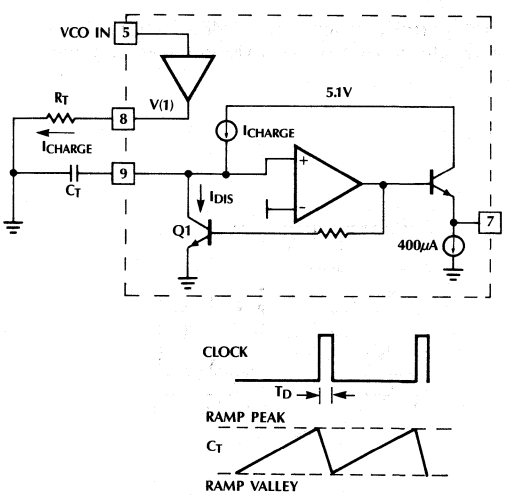


Figure 1. Oscillator Block Diagram

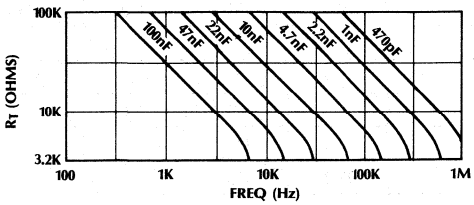


Figure 2. Timing Resistance vs Frequency (V(VCO) = 5.1V)

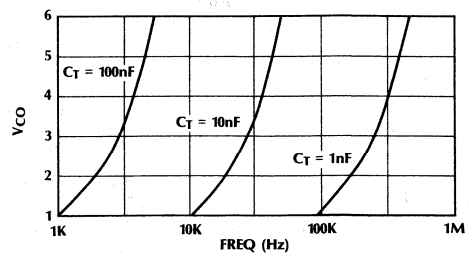


Figure 3. Oscillator Frequency vs V(VCO) (RC = 6.2KΩ, 1000pF)

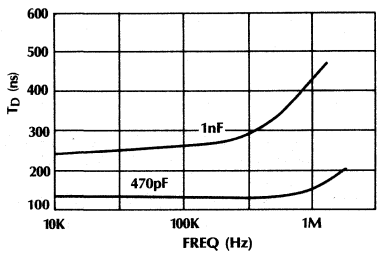


Figure 4. Oscillator Deadtime vs Frequency (V(VCO) = 5.1V)

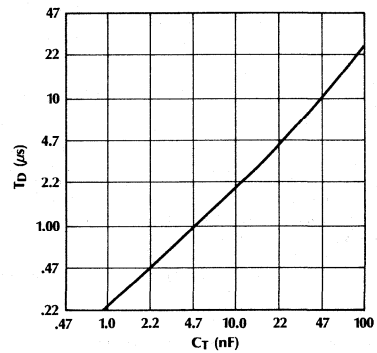


Figure 5. Oscillator Deadtime vs C(T) (3KΩ ≤ R(T) ≤ 100KΩ)

ERROR AMPLIFIER

The ML4809 error amplifier is a 3.5MHz bandwidth 6V/μs slew rate op-amp with provision for limiting the positive output voltage swing (Output Inhibit line) for ease in implementing the soft start function.

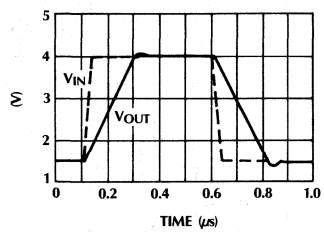


Figure 6. Unity Gain Slew Rate

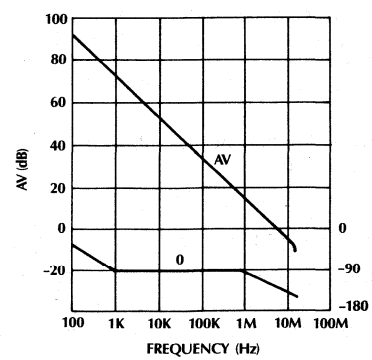


Figure 7. Open Loop Frequency Response

OUTPUT DRIVER STAGE

The ML4809 Output Driver is a 2A peak output high speed totem pole circuit designed to drive capacitive loads, such as power MOSFET transistors.

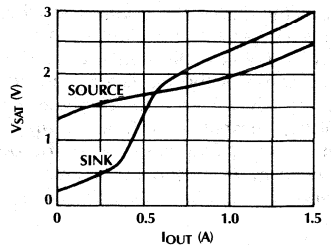


Figure 8. Saturation Curves

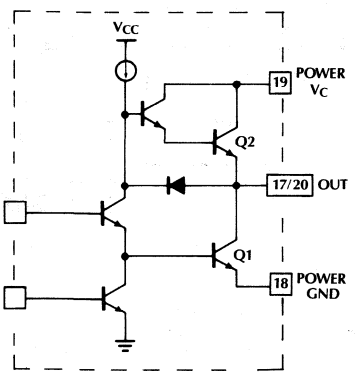


Figure 9. Simplified Schematic

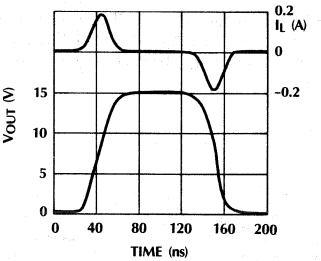


Figure 10a. Rise/Fall Time (C_L = 1000pF)

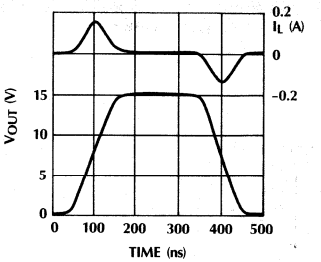


Figure 10b. Rise/Fall Time (C_L = 10000pF)

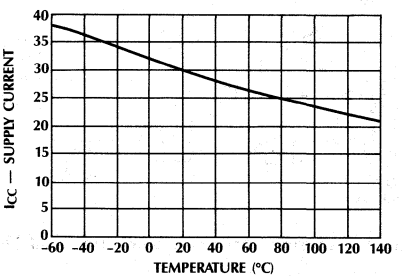


Figure 11. Supply Current vs. Temperature

SOFT START, CURRENT LIMIT, AND RESET DELAY

The ML4809 employs two current limits. When the voltage at pin 15 (I(LIM)/S.D.) exceeds 1.1V, the outputs immediately pull low and the cycle is terminated for the remainder of the oscillator period by resetting the RS flip flop.

If the output current is rising quickly (usually due to transformer saturation) such that the voltage on pin 15 reaches 1.5V before the outputs have turned off, a soft start cycle is initiated. The soft start capacitor (pin 11) is discharged and outputs are held "off" until the voltage at pin 11 reaches 1.1V, ensuring a complete soft start cycle. The duty cycle on start up is limited by limiting the output voltage of the error amplifier voltage to the voltage at pin 11.

The ML4809 also includes a delay circuit which inhibits the outputs from coming on until a time determined by the RESET DELAY capacitor on pin 12. This capacitor is normally charged to a voltage equal to $V_{PIN\ 11}$ – .7V and is limited to V_{REF}. After the 1.5V limit is reached, the capacitor is allowed to slowly discharge through the 9μA current sink. When this capacitor and the Soft Start Capacitor both have discharged to 1.1V, the outputs are enabled and the new soft start cycle begins. During Under Voltage Lockout, both capacitors will be discharged to prepare for a new cycle.

Since the emitter follower which drives pin 12 presents a load on Pin 11, the Soft Start Capacitor's effective value will be increased by:

$$C_{EFFECT} = C_{PIN\ 11} + (C_{PIN\ 12}/\beta)$$

where β varies from 50 to 250. Should this cause unacceptable variation on the soft start capacitor value, this effect can be mitigated by connecting a resistor from V_{REF} to pin 11 to charge the Soft Start Cap (select a resistor which keeps the charge current below 2mA).

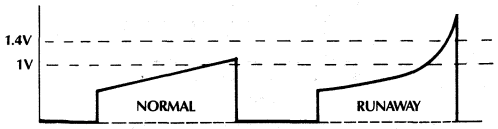


Figure 12. Normal (Cycle by Cycle) and "Runaway" Current Timing

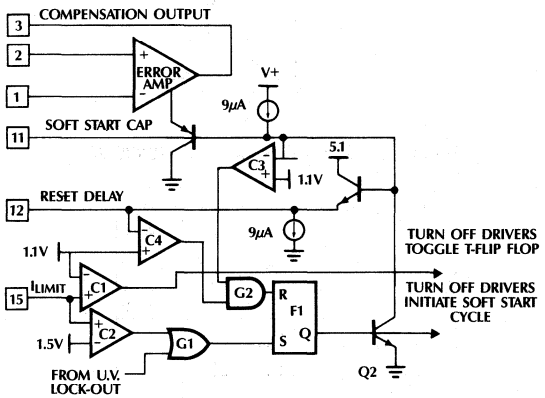


Figure 13. Current Limit, Soft Start and Reset Delay

UNDERVOLTAGE LOCKOUT

In the circuit in Figure 14, the ML4809 remains in a low quiescent drain (1.1mA) during T1 while C1 charges through R(S) to 16V. After V_{CC} rises to 16V the ML4809 begins running. C1 provides the energy needed to run the gate drive and ML4809 until the auxiliary winding can provide sustaining energy for the control circuit, preventing C1 from draining below the 9V lockout threshold. The 7V of hysteresis in the Undervoltage Lockout circuit allows the ML4809 to start from a bleed resistor/capacitor easily. While the ML4809 is in the standby (Lockout) condition, OUTA and OUTB will be pulled low.

RAMP COMPENSATION

In order to allow stable operation of a current mode regulator above 50% duty cycle, some of the oscillator ramp needs to be added to the current signal.

Notice that the waveform of (1) and the waveform of ramp (2) have different average current values. (1) is an example of a waveform for high line and (2) an example of low line. Since the controllers all regulate based on the peak value of the current in the circuit, and the control variable really wants to be the average current, adding some of the oscillator ramp to comparator input (shown here for clarity as a subtraction of the comparator reference input, which is the output of the error amplifier) allows the peak current control to more closely approximate the average current.

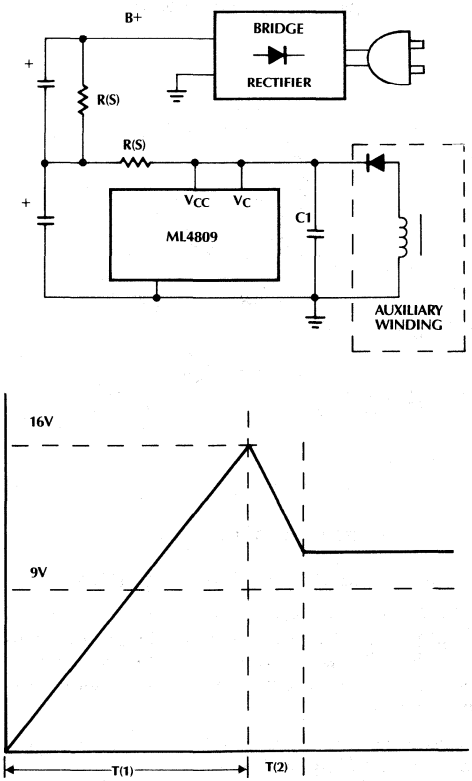


Figure 14. Typical Off-Line Start-Up Circuit and Timing

In the actual implementation, an external resistor (pin 23) sets a current which will be equal to $V_{RAMP}/R1$ and will appear on the comparator input pin. Since the sense resistor is a low impedance point, putting another resistor (R2) in series with the V_{SENSE} pin (10) causes a voltage to add to the ramp voltage which is equal to V_{RAMP} (R2/R1).

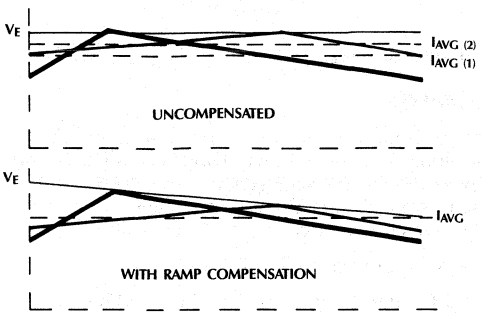


Figure 15. The Effect of Ramp Compensation

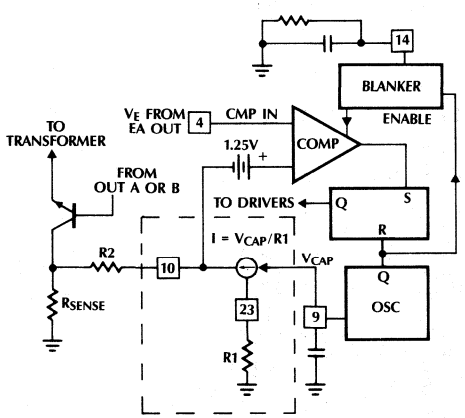


Figure 16. Ramp Compensation and Blanker Block Diagram

MAIN COMPARATOR BLANKER

When CMP IN (EA OUT) is at a low level, spikes which occur on RAMP (which is connected to a current sense resistor or transformer) when the power MOSFETs first turn on can cause the cycle to terminate early. The result of early termination can cause instabilities. Three problems occur which all contribute to this spike.

1. Inductance in the sense resistor.
2. Inter-winding capacitance in the transformer.
3. Reverse recovery current in the rectifier in the opposite FET intrinsic diode (or from the secondary diodes).

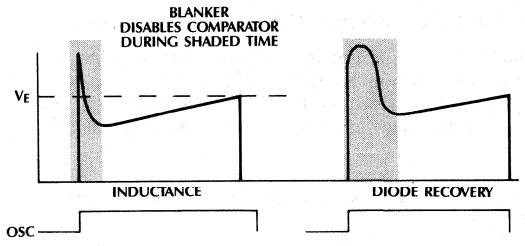


Figure 17. Unintended Early Cycle Termination

The first two problems usually cause a fairly short spike which is easy to filter out with just a simple RC before the comparator input without causing unacceptable phase delay at the input, since there is not much area underneath the spike. The third problem can have significant energy, and a filter with a low enough pole to reduce the "spike" to a level low enough not to cause early cycle termination would cause excessive phase shift.

The solution is to provide a blanking pulse to the comparator at the beginning of the cycle. The width of this pulse is programmed by an external RC. When CLOCK IN is high, a buffer in the ML4809 charges the capacitor on pin 14 to 4V. When CLOCK goes low, the capacitor discharges through the external resistor. The outputs are held low until the voltage at pin 14 falls below 3.2V. The buffer driving pin 14 is limited to 5mA output current. The Blanking period can be calculated by the expression:

$$T_{BLANK} \approx \frac{R_{BLANK}C_{BLANK}}{2.83}$$

SYNCHRONIZATION INPUTS AND OUTPUTS

When using the Clock (pin 7) or Q (pin 13) outputs, a 5KΩ pull down resistor is recommended. These outputs are open emitters. Clock has an internal (375μA) current sink load while Q is unloaded. Both will exhibit significant timing skew due to PC board capacitance if not loaded.

Clock Output and External Clock Input

Used to synchronize multiple supplies. For synchronized operation of multiple ML4809's, tie the CLOCK OUT from the "master" to the CLOCK IN of the slaves.

Toggle Preset and Q Output

In multiple supply systems, this is important for synchronization. To synchronize multiple chips, connect the Q output from the "master" ML4809 to the Preset Input of the "slave" in a "daisy chain". For non-synchronized operation this input would be connected to GND.

OTHER FEATURES

Fast Shut Down Path from Current Limit to Outputs

Provides a 30ns path to the outputs which begins to turn off the outputs while the longer latching path is propogating. In a normal UC1825, it can be as much as 80ns until the over-current condition shuts down the outputs.

Separate Error Amplifier Output Pin for Loop Filtering Versatility

This is especially useful for:

1. Diagnostic purposes, to see what the chip is really doing, it is useful to break the feedback loop.
2. High power supplies — current sharing: In system design with more than one supply running, in order to ensure that the supplies share current equally it is often necessary to have a "master" circuit control the PWM operation of each of the "slaves". This is most easily accomplished by an "or" (where the lowest output dominates) of the Error Amp outputs, which is impossible if the output of the amp is internally connected to the input of the comparator.

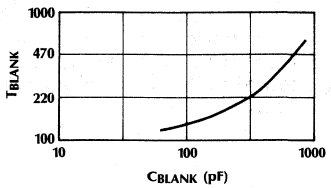


Figure 18. T_{BLANK} vs. C_{BLANK} (R_{BLANK} = 5.1KΩ)

APPLICATIONS

Figure 19 shows the ML4809 in a push-pull non-isolated application. Note the Schottky Diodes on pins 17 and 20. These diodes are necessary in order to prevent transients from driving these pins negative with respect to GND which would cause the IC to malfunction.

Care should be exercised in layout:

1. Avoid Ground Loops. Use "star" grounding.
2. Bypass the V_{CC} line with a high frequency capacitor which is physically close to the IC.
3. Avoid running signal lines near power lines.
4. Employ "ground planing".

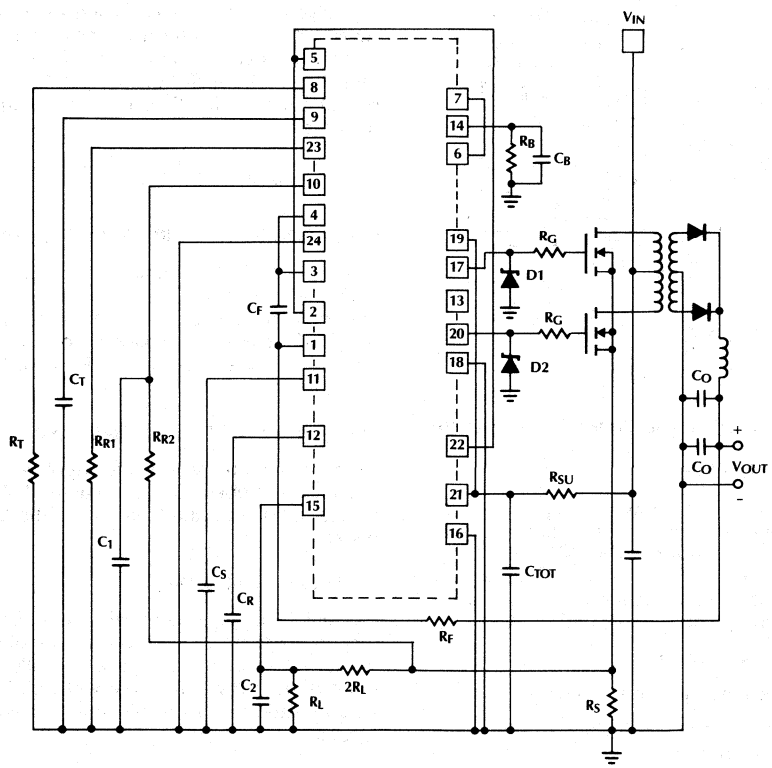


Figure 19. ML4809 Typical Application

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ML4809CP	0°C to +70°C	Molded DIP
ML4809CQ	0°C to +70°C	Molded PCC
ML4809IP	–40°C to +85°C	Molded DIP
ML4809IQ	–40°C to +85°C	Molded PCC
ML4809MJ	–55°C to +125°C	Hermetic DIP

Micro Linear

ML4810, ML4811

High Frequency Power Supply Controller

GENERAL DESCRIPTION

The ML4810 and ML4811 High Frequency PWM Controllers are optimized for use in Switch Mode Power Supply designs running at frequencies to 1MHz. The ML4810/11 contain a unique overload protection circuit which helps to limit stress on the output devices and reliably performs a soft-start reset. Propagation delays are minimal through the comparators and logic for reliable high frequency operation and slew rate and bandwidth are maximized on the error amplifier. These controllers are designed to work in either voltage or current mode and provide for input voltage feed forward.

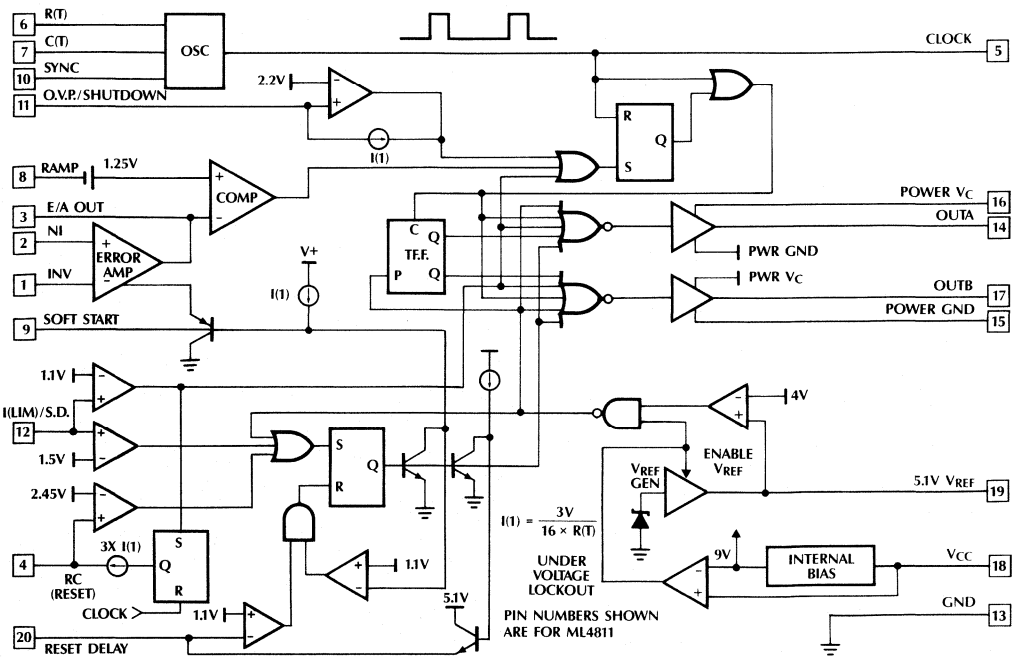
A 1.1V threshold current limit comparator provides a cycle-by-cycle current limit. An integrating circuit "counts" the number of times the 1.1V limit was reached. A soft-start cycle is initiated if the cycle-by-cycle current limit is repeatedly activated. A reset delay function is provided on the ML4811. All logic is fully latched to provide jitter-free operation and prevent multiple pulsing. An under-voltage lockout circuit with 7V of hysteresis assures low startup current and drives the outputs low during fault condition.

The ML4810/11 are fabricated on a 40V bipolar process from the FB3480 Power Supply Controller Array. Customized versions of this controller can therefore be easily implemented. Please refer to the FB3480 datasheet for more information. These controllers are similar to the UC1825 controller, however these controllers include many features not found on the 1825. These features are set in *Italics*.

FEATURES

- *Integrating Soft Start Reset*
- High Current (2A peak) Dual Totem Pole Outputs
- Practical Operation to 1MHz (f_{OSC})
- 5.1V, ±1% Trimmed Bandgap Reference
- *Under Voltage Lockout with 7V Hysteresis*
- *Soft Start Reset Delay* (ML4811)
- *Oscillator Synchronization Function* (ML4811)
- *Soft Start latch ensures full soft start cycle*
- *Outputs pull low for undervoltage lockout*
- *Accurately controlled Oscillator ramp discharge current*
- *All timing currents "slaved" to R(T) for precise control*

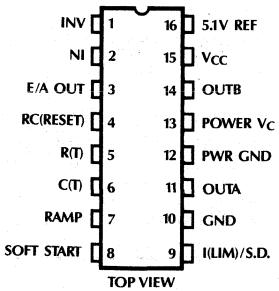
ML4811 BLOCK DIAGRAM



Micro Linear

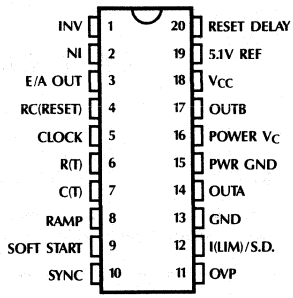
PIN CONNECTIONS

ML4810
16-Pin DIP



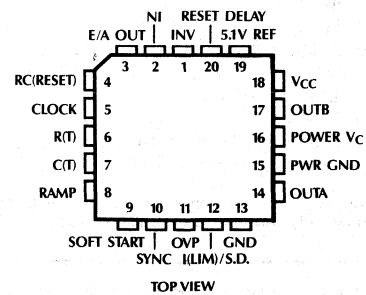
TOP VIEW

ML4811
20-Pin DIP



TOP VIEW

ML4811
20-Pin PCC



TOP VIEW

PIN DESCRIPTION (Pin numbers shown for ML4811)

PIN NO.	NAME	FUNCTION
1	INV	Inverting input to error amp
2	NI	Non-inverting input to error amp
3	E/A Out	Output of error amplifier and input to main comparator
4	RC(RESET)	Timing elements for Integrating Soft Start reset
5	CLOCK	Oscillator output.
6	R(T)	Timing Resistor for Oscillator — sets charging current for oscillator timing capacitor (Pin 6)
7	C(T)	Timing Capacitor for Oscillator
8	RAMP	Non-Inverting input to main comparator. Connected to C(T) for Voltage Mode operation or to current sense resistor for current mode
9	SOFT START	Normally connected to Soft Start Capacitor
10	SYNC	A high going pulse terminates the PWM cycle and discharges C(T)
11	OVP	Exceeding 2.5V terminates the PWM cycle and inhibits the outputs
12	I(LIM)/S.D.	Current limit sense pin. Normally connected to current sense resistor
13	GND	Analog Signal Ground
14	OUTA	High Current Totem pole output. This output is the first one energized after Power On Reset
15	PWR GND	Return for the High Current Totem pole outputs
16	V_C	Positive Supply for the High Current Totem pole outputs
17	OUTB	High Current Totem pole output
18	V_{CC}	Positive Supply for the IC
19	5.1V REF	Buffered output for the 5.1V voltage reference
20	RESET DELAY	Timing Capacitor to determine the amount of delay between fault

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (Pins 18, 16) 30V
Output Current, Source or Sink (Pins 14, 17)
DC 0.5A
Pulse (0.5μS) 2.0A
Analog Inputs
(Pins 1, 2, 8) ..... –0.3V to 7V
(Pins 9, 10, 11, 12, 20) ..... –0.3V to 6V
Clock Output Current (Pin 5) ..... –5mA
Error Amplifier Output Current (Pin 3) 5mA
Junction Temperature
ML4811M ..... 150°C
ML4811I, ML4810C, ML4811C ..... 125°C
Storage Temperature Range ..... –65°C to +150°C
Lead Temperature (Soldering 10 sec.) ..... +260°C
Thermal Resistance (θ_{JA})
Plastic DIP ..... 65°C/W
Ceramic DIP ..... 65°C/W
Plastic Chip Carrier (PCC) ..... 60°C/W

OPERATING CONDITIONS

Temperature Range
ML4811M ..... –55°C to +125°C
ML4811I ..... –40°C to +85°C
ML4810C, ML4811C ..... 0°C to +70°C

Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied. Pin numbers given for ML4811.

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, R_T = 3.65KΩ, C_T = 1000pF, T_A = Operating Temperature Range, V_{CC} = 15V.

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
Oscillator						
Initial Accuracy		T_J = 25°C (note 1)	360	400	440	KHz
Voltage Stability		10V < V_{CC} < 30V, (note 1)		0.2	2	%
Temperature Stability		(note 1)			5	%
Total Variation		line, temp. (note 1)	340		460	KHz
Clock Out High			3.9	4.5		V
Clock Out Low				2.3	2.9	V
Ramp Peak		(note 1)	2.6	2.8	3.0	V
Ramp Valley		(note 1)	0.7	1.0	1.25	V
Ramp Valley to Peak		(note 1)	1.6	1.8	2.0	V
Sync Input Threshold			0.8	1.0	1.2	V
Sync Input Current		$V_{PIN\ 10}$ = 4V				μA
Reference Section						
Output Voltage	ML4810/11C	T_J = 25°C, I_O = 1mA	5.00	5.10	5.2	V
	ML4811M, ML4811I		5.05	5.10	5.15	V
Line Regulation		10V < V_{CC} < 30V		2	20	mV
Load Regulation		1mA < I_O < 10mA		5	20	mV
Temperature Stability		–55°C < T_J < 150°C, (note 1)		.2	.4	%
Total Variation	ML4810/11C	line, load, temp. (note 1)	4.95		5.25	V
	ML4811M, ML4811I		5.0		5.20	V
Output Noise Voltage		10Hz to 10KHz		50		μV
Long Term Stability		T_J = 125°C, 1000 Hrs (note 1)		5	25	mV
Short Circuit Current		V_{REF} = 0V	–15	–50	–100	mA
Under-Voltage Lockout Section						
Start Threshold			15	16	17	V
UVLO Hysteresis			6.5	7	7.5	V
Supply Current						
Start Up Current		V_{CC} = 8V		2	3	mA
I_{CC}		$V_{PIN\ 1,\ 7,\ 9}$ = 0V, $V_{PIN\ 2}$ = 1V, T_A = 25°C		32	42	mA

ELECTRICAL CHARACTERISTICS (Continued)

Unless otherwise specified, R_T = 3.65KΩ, C_T = 1000pF, T_A = Operating Temperature Range, V_{CC} = 15V.

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
Error Amplifier Section						
Input Offset Voltage	ML4810/11C				15	mV
	ML4811M, ML4811I				10	mV
Input Bias Current				.6	3	μA
Input Offset Current				.1	1	μA
Open Loop Gain		$1 < V_O < 4V$	60	96		dB
CMRR		$1.5 < V_{CM} < 5.5V$	75	95		dB
PSRR		$10 < V_{CC} < 30V$	75	90		dB
Output Sink Current		$V_{PIN\ 3}$ = 1V	1	2.5		mA
Output Source Current		$V_{PIN\ 3}$ = 4V	-.5	-1.3		mA
Output High Voltage		$I_{PIN\ 3}$ = -0.5mA	4.0	4.7	5.0	V
Output Low Voltage		$I_{PIN\ 3}$ = 1mA	0	0.5	1.0	V
Unity Gain Bandwidth		(note 1)	3	5.5		MHz
Slew Rate		(note 1)	6	12		V/μs
PWM Comparator Section						
Pin 8 Bias Current		$V_{PIN\ 8}$ = 0V		-1	-5	μA
Duty Cycle Range			0		75	%
Pin 3 Zero DC Threshold			1.1	1.25		V
Delay to Output		(note 1)		50	80	ns
Soft-Start Section						
Charge Current (Pin 9)		$V_{PIN\ 9}$ = 1V, $V_{PIN\ 12}$ = 0, $V_{PIN\ 4}$ = 0	40	50	60	μA
Discharge Current (Pin 9)		$V_{PIN\ 9}$ = 3V, $V_{PIN\ 4} > 2.5$	1	5		mA
		$V_{PIN\ 9}$ = 3V, $V_{PIN\ 12} > 1.65$, $V_{PIN\ 4} < 2$	1	5		mA
Charge Current (Pin 20)		$V_{PIN\ 20}$ = 1V	1	5		mA
Discharge Current (Pin 20)		Requires external discharge resistor		0		μA
Current Limit/Shutdown Section						
Pin 12 Bias Current	ML4810/11C	$0V < V_{PIN\ 12} < 4V$			+15	μA
	ML4811M, ML4811I	$0V < V_{PIN\ 12} < 4V$			+10	μA
Current Limit Threshold			1.0	1.1	1.2	V
Reset Threshold (Pin 12)		$V_{PIN\ 4} < 2V$	1.35	1.50	1.65	V
Delay to Output		(note 1)		40	70	ns
Pin 4 Charging Current		$V_{PIN\ 12}$ = 2V	120	150	180	μA
Restart Threshold (Pin 4)			2	2.45	3	V
OVP Shutdown Threshold (Pin 11)			1.8	2.2	2.6	V
OVP Input Current		$V_{PIN\ 11}$ = 3V	40	50	60	μA
Output Section						
Output Low Level		I_{OUT} = 20mA		.25	.4	V
		I_{OUT} = 200mA		1.2	2.2	V
Output High Level		I_{OUT} = -20mA	13.0	13.5		V
		I_{OUT} = -200mA	12.0	13.0		V
Collector Leakage		V_C = 30V		100	500	μA
Rise/Fall Time		C_L = 1000pF, (note 1)		30	80	ns

Note 1: This parameter not 100% tested in production but guaranteed by design.

FUNCTIONAL DESCRIPTION

SOFT START AND CURRENT LIMIT — INTEGRATING SOFT START RESET

The ML4810/11 offers a unique system of fault detection and reset. Most PWM controllers use a two threshold method which relies on the buildup of current in the output inductor during a fault. This buildup occurs because:

1. Inductor di/dt is a small number when the switch is off under load fault (short circuit) conditions, since V_L is small.
2. Some energy is delivered to the inductor since the IC must first detect the over-current because there is a finite delay before the output switch can turn off.

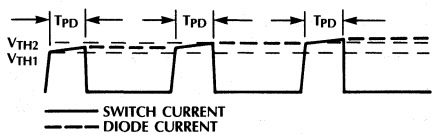


Figure 1. Current Waveforms for Slow Turn-Off System with Load Fault

This scheme was adequate for controllers with longer comparator propagation delays and turn-off delays than is desirable in a high frequency system. For systems with low propagation delays, very little energy will be delivered to the inductor and the current "ratcheting" described above will not occur. This results in the controller never detecting the load fault and continuing to pump full current to the load indefinitely, causing heating in the output rectifiers and inductor.

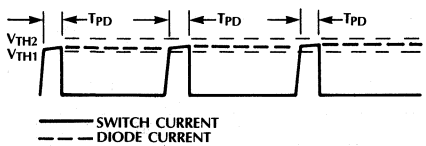


Figure 2. Current Waveforms for High Speed System with Load Fault

A method of circumventing this problem involves "counting" the number of times the controller terminates the PWM cycle due to the cycle by cycle current limit.

When the switch current crosses the 1.1V threshold A1 signals the F1 to terminate the cycle and sets F3, which is reset at the beginning of the PWM cycle. The output of F3 turns on a current source to charge C2. When, after several cycles, C2 has charged to 2.45V, A5 turns on F2 to discharge soft start capacitor C1. Charge is continually bled from C2 by R1. If a current surge is short lived (for instance a disk drive start-up or a board being plugged into a live rack) the control can "ride

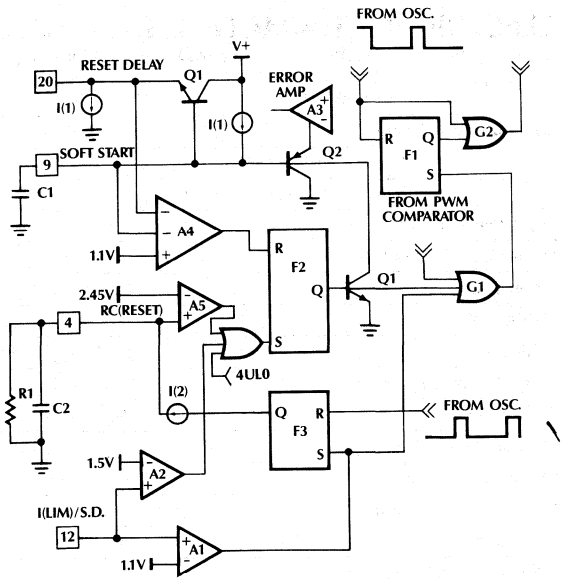


Figure 3. Integrating Soft Start Reset

out" the surge with the switch protected by the cycle by cycle limit. R1 and C1 can be selected to track diode heating, or to ride out various system surge requirements as required.

If the high current demanded is caused by a short circuit, the duty cycle will be short and the output diodes will carry the current for the majority of the PWM cycle. C2 charges fastest for low duty cycles (since F3 will be on for a longer time) providing for quicker shutdown during short-circuit when the output diodes are being maximally stressed.

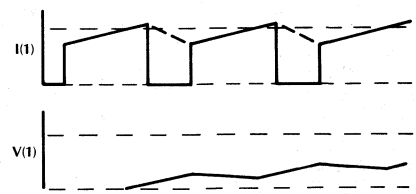


Figure 4. Switching Current and Pin 4 Voltage — Normal

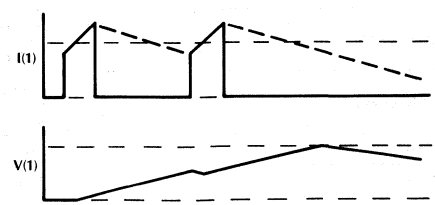


Figure 5. Switching Current and Pin 4 Voltage — Load Fault

OSCILLATOR

The ML4811 oscillator charges the external capacitor (C_T) with a current (I_{SET}) equal to $3/R_T$. When the capacitor voltage reaches the upper threshold (Ramp Peak), the comparator changes state and the capacitor discharges to the lower threshold (Ramp Valley) through Q1. While the capacitor is discharging, Q2 provides a high pulse. A discharge of the oscillator can be initiated by applying a high level to the Sync pin. A short pulse of a frequency higher than the oscillator's free running frequency can be used to synchronize the ML4811 to an external clock. The pulse can be equal to the desired deadtime (T_D) or the deadtime can be determined by I_{DIS} and C_T, whichever is greater.

The Oscillator period can be described by the following relationship:

$$T_{OSC} = T_{RAMP} + T_{DEADTIME}$$

where: T_{RAMP} = C (Ramp Valley to Peak)/I_{SET}
and: $T_{DEADTIME}$ = C (Ramp Valley to Peak)/I_{Q1}

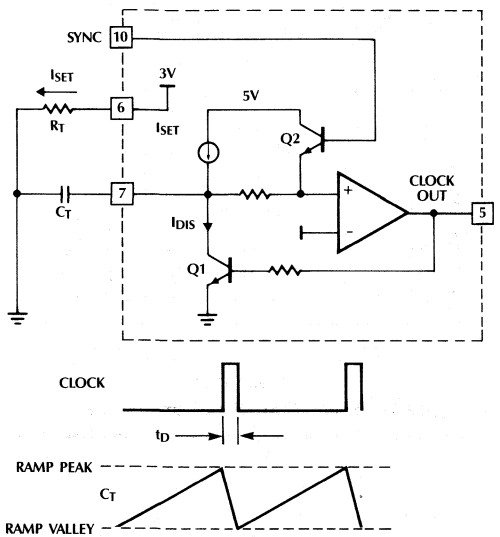


Figure 6. Simplified Oscillator Block Diagram and Timing

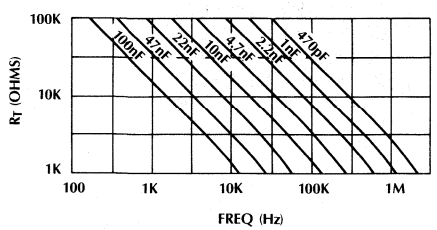


Figure 7. Oscillator Timing Resistance vs. Frequency

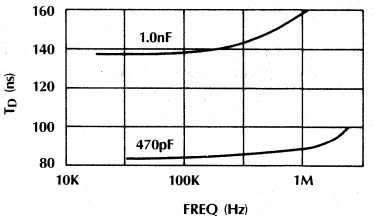


Figure 8. Oscillator Deadtime vs Frequency

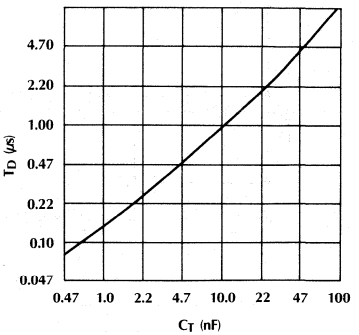


Figure 9. Oscillator Deadtime vs C(T) ($3 \leq R(T) \leq 100K\Omega$)

ERROR AMPLIFIER

The ML4811 error amplifier is a 5.5MHz bandwidth 12V/µsec slew rate op-amp with provision for limiting the positive output voltage swing (Output Inhibit line) for ease in implementing the soft start function.

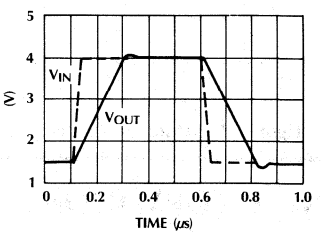


Figure 10. Unity Gain Slew Rate

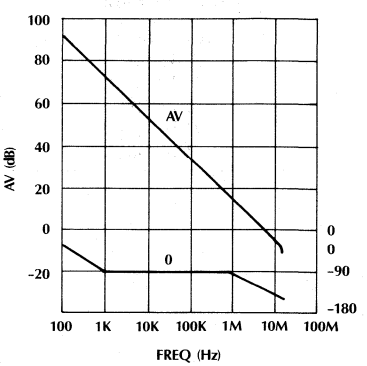


Figure 11. Open Loop Frequency Response

OUTPUT DRIVER STAGE

The ML4811 Output Driver is a 2A peak output high speed totem pole circuit designed to quickly switch the gates of capacitive loads, such as power MOSFET transistors.

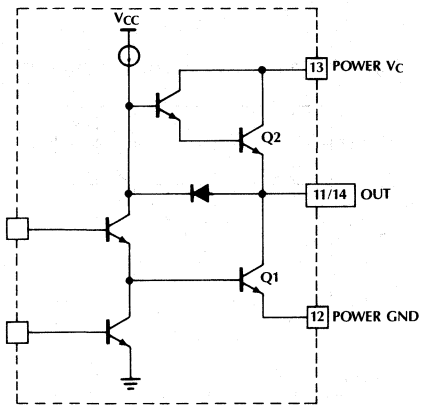


Figure 12. Simplified Schematic

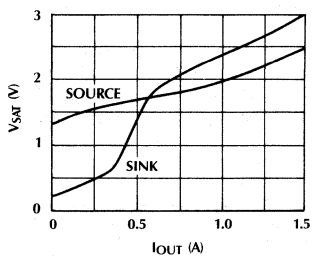


Figure 13. Saturation Curves

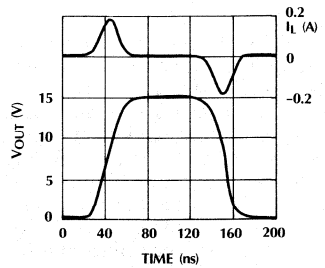


Figure 14. Rise/Fall Time (C_L = 1000pF)

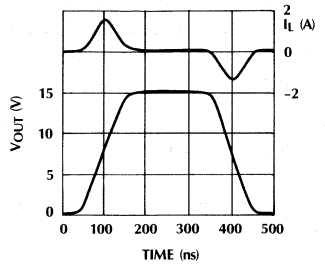


Figure 15. Rise/Fall Time (C_L = 10,000pF)

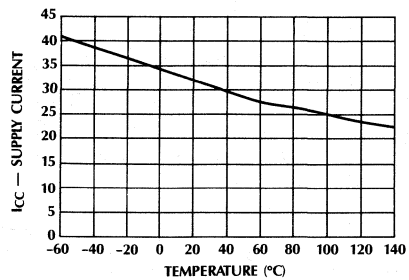


Figure 16. Suppy Current vs. Temperature

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ML4810CP	0°C to +70°C	16-Pin MOLDED DIP
ML4811CP	0°C to +70°C	20-Pin MOLDED DIP
ML4811CQ	0°C to +70°C	20-Pin MOLDED PCC
ML4811IP	–40°C to +85°C	20-Pin MOLDED DIP
ML4811IQ	–40°C to +85°C	20-Pin MOLDED PCC
ML4811MJ	–55°C to +125°C	20-Pin HERMETIC DIP

ML4812

Power Factor Controller

GENERAL DESCRIPTION

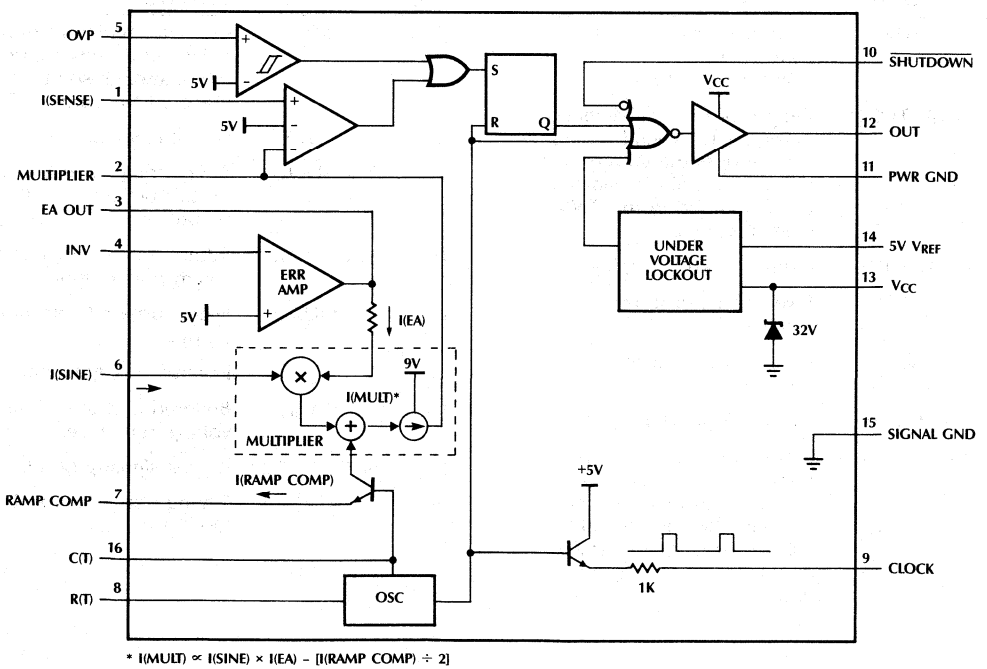
The ML4812 is designed to optimally facilitate a "boost" type power factor correction system. Special care has been taken in the design of the ML4812 to increase system noise immunity. The circuit includes a precision reference, multiplier, error amplifier, over-voltage protection, ramp compensation, as well as a high current output. In addition, start-up is simplified by an under-voltage lockout circuit with 6V hysteresis.

In a typical application, the ML4812 functions as a current mode regulator. The current which is necessary to terminate the cycle is a product of the sinusoidal line voltage times the output of the error amplifier which is regulating the output DC voltage. Ramp compensation is programmable with an external resistor, to provide stable operation when the duty cycle exceeds 50%.

FEATURES

- Precision buffered 5V reference (±0.5%)
- Current Input Multiplier reduces external components and improves noise immunity
- Programmable Ramp Compensation circuit
- 1A Peak Current Totem-Pole Output Drive
- Over-Voltage comparator eliminates output "runaway" due to load removal
- Wide common mode range in current sense comparators for better noise immunity
- Large oscillator amplitude for better noise immunity

BLOCK DIAGRAM (Pin Out shown is for DIP)

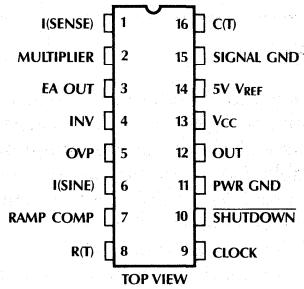


* I(MULT) ∝ I(SINE) × I(EA) − [I(RAMP COMP) ÷ 2]

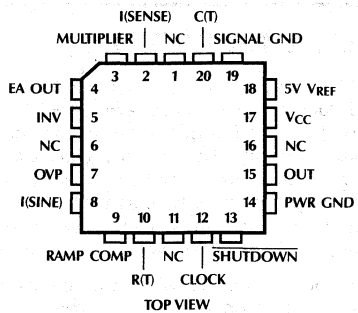
PATENTED

PIN CONNECTIONS

ML4812
16-Pin DIP



ML4812
20-Pin PCC



PIN DESCRIPTION (DIP)

PIN NO.	NAME	FUNCTION
1	I(SENSE)	Input from the Current Sense Transformer (T1) to the PWM comparator (+).
2	MULTIPLIER	Output of Current Multiplier. A resistor to ground on this pin converts the current to a voltage. This pin is clamped to 5V and tied to the PWM comparator (–).
3	EA OUT	Output of error amplifier.
4	INV	Inverting input to error amplifier.
5	OVP	Input to over voltage comparator.
6	I(SINE)	Current Multiplier Input.
7	RAMP COMP	Buffered output from the Oscillator Ramp [C(T)]. A resistor to ground sets the current which is internally subtracted from the product of I(SINE) and I(EA) in the multiplier.
8	R(T)	Oscillator timing resistor pin. A 5V source sets a current in the external resistor which is mirrored to charge C(T).
9	CLOCK	Digital clock output.
10	$\overline{\text{SHUTDOWN}}$	A TTL compatible low level on this pin turns off the output.
11	PWR GND	Return for the High Current Totem pole output.
12	OUT	High Current Totem pole output.
13	V_{CC}	Positive Supply for the IC.
14	5V V_{REF}	Buffered output for the 5V voltage reference.
15	SIGNAL GND	Analog signal ground.
16	C(T)	Timing Capacitor for the Oscillator.

ABSOLUTE MAXIMUM RATINGS

Supply Current (I_{CC}) 30mA
Output Current, Source or Sink (Pin 12)
DC 1.0A
Output Energy (capacitive load per cycle) 5μJ
Multiplier I(SINE) Input (pin 6) 1.2mA
Error Amp Sink Current (pin 3) 10mA
Oscillator Charge Current 2mA
Analog Inputs (pins 1, 4, 5) ..... –0.3V to 5.5V
Junction Temperature ..... 150°C
Storage Temperature Range ..... –65°C to +150°C
Lead Temperature (soldering 10 sec.) ..... +260°C

Thermal Resistance (θ_{JA})
Plastic Chip Carrier (PCC) — Q ..... 60°C/W
Plastic DIP — P ..... 65°C/W
Ceramic DIP — J ..... 65°C/W

OPERATING CONDITIONS

Temperature Range
ML4812C ..... 0°C to +70°C
ML4812I ..... –40°C to +85°C
ML4812M ..... –55°C to +125°C

Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, R_T = 14KΩ, C_T = 1000pF, T_A = Operating Temperature Range, V_{CC} = 15V (note 2), Pin numbers refer to 16-pin DIP package.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Oscillator					
Initial Accuracy	T_J = 25°C	91	98	105	KHz
Voltage Stability	12V < V_{CC} < 18V		0.3		%
Temperature Stability			2		%
Total Variation	line, temp.	90		108	KHz
Ramp Valley to Peak			3.3		V
R(T) Voltage		4.8	5.0	5.2	V
Discharge Current (pin 8 open)	T_J = 25°C, $V_{PIN\ 16}$ = 2V	7.8	8.4	9.0	mA
	$V_{PIN\ 16}$ = 2V	7.3	8.4	9.3	V
Clock Out Voltage Low	R_L = 16KΩ		0.2	0.5	V
Clock Out Voltage High	R_L = 16KΩ	3.0	3.5		V
Reference Section					
Output Voltage	T_J = 25°C, I_O = 1mA	4.95	5.00	5.05	V
Line Regulation	12V < V_{CC} < 25V		2	20	mV
Load Regulation	1mA < I_O < 20mA		2	20	mV
Temperature Stability			0.4		%
Total Variation	line, load, temp	4.9		5.1	V
Output Noise Voltage	10Hz to 10KHz		50		μV
Long Term Stability	T_J = 125°C, 1000 Hrs (note 1)		5	25	mV
Short Circuit Current	V_{REF} = 0V	–30	–85	–180	mA
Error Amplifier Section					
Input Offset Voltage				±15	mV
Input Bias Current			–0.1	–1.0	μA
Open Loop Gain	1 < $V_{PIN\ 3}$ < 5V	60	75		dB
PSRR	12V < V_{CC} < 25V	60	75		dB
Output Sink Current	$V_{PIN\ 3}$ = 1.1V, $V_{PIN\ 4}$ = 6.2V	2	12		mA
Output Source Current	$V_{PIN\ 3}$ = 5.0V, $V_{PIN\ 4}$ = 4.8V	–0.5	–1.0		mA
Output High Voltage	$I_{PIN\ 3}$ = –0.5mA, $V_{PIN\ 4}$ = 4.8V	5.3	5.5		V
Output Low Voltage	$I_{PIN\ 3}$ = 1mA, $V_{PIN\ 4}$ = 6.2V		0.5	1.0	V
Unity Gain Bandwidth			1.0		MHz

ELECTRICAL CHARACTERISTICS (Continued)

Unless otherwise specified, R_T = 14KΩ, C_T = 1000pF, T_A = Operating Temperature Range, V_{CC} = 15V (note 2), Pin numbers refer to 16-pin DIP package.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Multiplier					
I(SINE) Input Voltage	I(SINE) = 500μA	.4	.7	.9	V
Output Current (pin 2)	I(SINE) = 500μA, PIN 4 = V_{REF} – 20mV	460	480	510	μA
	I(SINE) = 500μA, PIN 4 = V_{REF} + 20mV		3	10	μA
	I(SINE) = 1mA, PIN 4 = V_{REF} – 20mV	900	950	1020	μA
	I(SINE) = 500μA, PIN 4 = V_{REF} – 20mV, $I_{PIN\ 7}$ = 50μA		455		μA
Bandwidth			200		KHz
PSRR	12V < V_{CC} < 25V		70		dB
OVP Comparator					
Input Offset Voltage	Output Off	–25		+5	mV
Hysteresis	Output On	95	105	115	mV
Input Bias Current			–0.3	–3	μA
Propagation Delay			150		nS
PWM Comparator: I(SENSE)					
Input Offset Voltage				±15	mV
Input Offset Current				±1	mV
Input Common Mode Range		–0.2		5.5	V
Input Bias Current			–2	–10	μA
Propagation Delay			150		nS
I_{LIMIT} Trip Point	$V_{PIN\ 2}$ = 5.5V	4.8	5	5.2	V
Output Section					
Output Voltage Low	I_{OUT} = –20mA		0.1	0.4	V
	I_{OUT} = –200mA		1.6	2.2	V
Output Voltage High	I_{OUT} = 20mA	13	13.5		V
	I_{OUT} = 200mA	12	13.4		V
Output Voltage Low in UVLO	I_{OUT} = –10mA, V_{CC} = 8V		0.1	0.8	V
Output Rise/Fall Time	C_L = 1000pF		50		nS
Shut Down Input	V_{IH}	2.0			V
	V_{IL}			0.8	V
	I_{IL}, $V_{PIN\ 10}$ = 0V			–1.5	mA
	I_{IH}, $V_{PIN\ 10}$ = 5V			10	μA
Under-Voltage Lockout					
Start-Up Threshold		15	16	17	V
Shut-Down Threshold		9	10	11	V
V_{REF} Good Threshold			4.4		V
Total Device					
Supply Current	Start-Up, V_{CC} = 14V, T_J = 25°C		.8	1.2	mA
	Operating, T_J = 25°C		20	25	mA
Internal Shunt Zener Voltage	I_{CC} = 30mA	25	30	34	V

Note 1: This parameter not 100% tested in production but guaranteed by design.

Note 2: V_{CC} is raised above the Start-Up Threshold first to activate the IC, then returned to 15V.

FUNCTIONAL DESCRIPTION

OSCILLATOR

The ML4812 oscillator charges the external capacitor (C_T) with a current (I_{SET}) equal to $5/R_{SET}$. When the capacitor voltage reaches the upper threshold, the comparator changes state and the capacitor discharges to the lower threshold through Q1. While the capacitor is discharging, Q2 provides a high pulse.

The Oscillator period can be described by the following relationship:

$$T_{OSC} = T_{RAMP} + T_{DEADTIME}$$

where:

$$T_{RAMP} = \frac{C_T \times V_{RAMP\ VALLEY\ TO\ PEAK}}{I_{SET}}$$

and:

$$T_{DEADTIME} = \frac{C_T \times V_{RAMP\ VALLEY\ TO\ PEAK}}{8.4mA - I_{SET}}$$

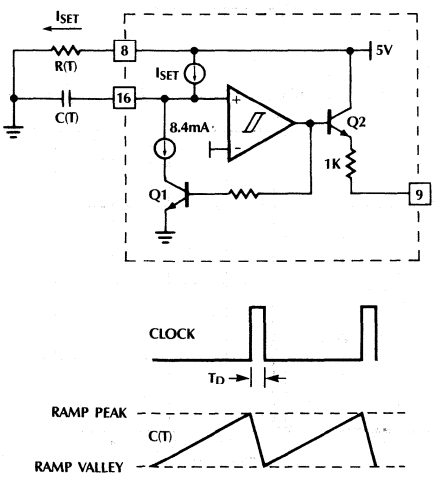


Figure 1. Oscillator Block Diagram

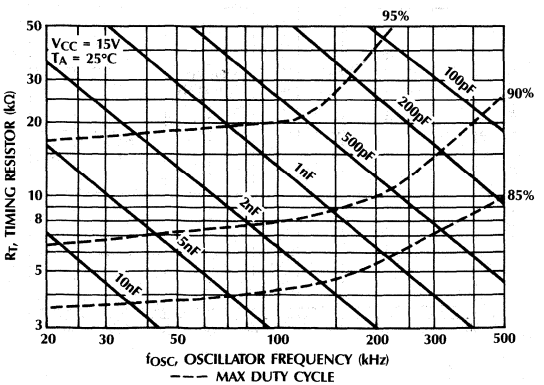


Figure 2. Oscillator Timing Resistance vs. Frequency

OUTPUT DRIVER STAGE

The ML4812 Output Driver is a 1A peak output high speed totem pole circuit designed to quickly drive capacitive loads, such as power MOSFET gates.

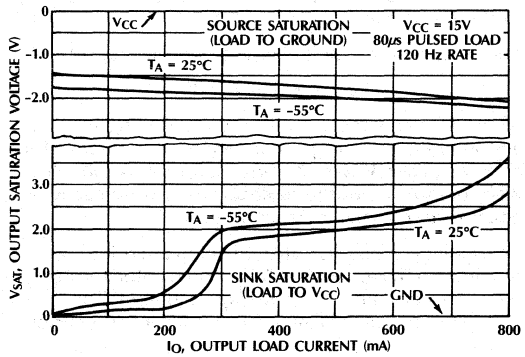


Figure 3. Output Saturation Voltage vs. Output Current

ERROR AMPLIFIER

The ML4812 error amplifier is a high open loop gain, wide bandwidth, amplifier.

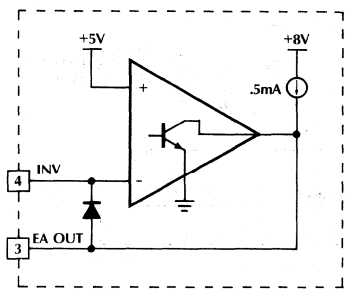


Figure 4. Error Amplifier Configuration

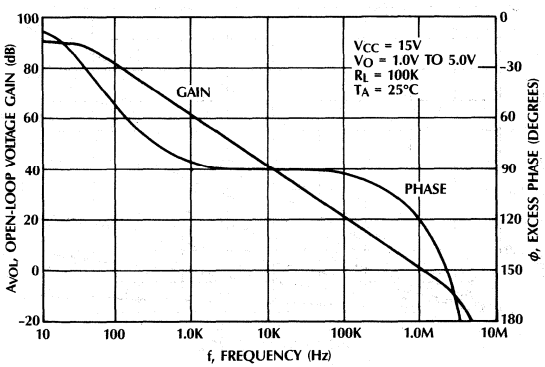


Figure 5. Error Amplifier Open-Loop Gain and Phase vs. Frequency

MULTIPLIER

The ML4812 multiplier is a linear current input multiplier to provide high immunity to the disturbances caused by high power switching. The rectified line input sine wave is converted to a current via a dropping resistor. In this way, small amounts of ground noise produce an insignificant effect on the reference to the PWM comparator.

The output of the multiplier is a current proportional to:

$$I_{OUT} \propto I(SINE) \times I(EA)$$

where I(SINE) is the current in the dropping resistor, and I(EA) is a current proportional to the output of the error amplifier. When the error amplifier is saturated high, the output of the multiplier is approximately equal to the I(SINE) input current.

The multiplier output current is converted into the reference voltage for the PWM comparator through a resistor to ground on the multiplier output. The multiplier output is clamped to 5V to provide current limiting.

Ramp compensation is accomplished by subtracting 1/2 of the current flowing out of pin 7 through a buffer transistor driven by C(T) which is set by an external resistor.

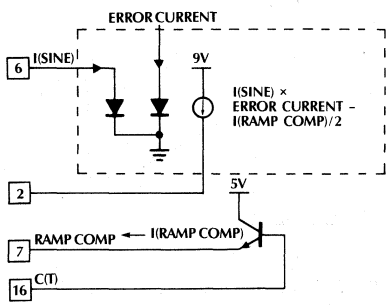


Figure 6. Multiplier Block Diagram

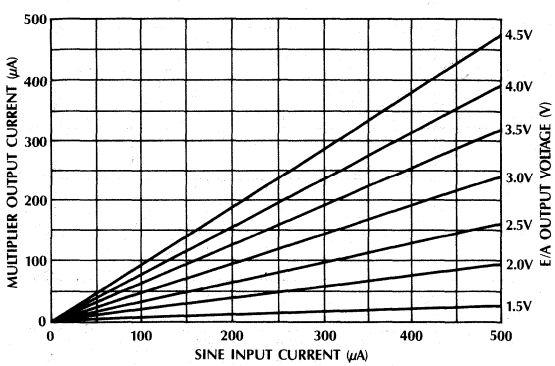


Figure 7. Multiplier Linearity

UNDER VOLTAGE LOCKOUT

On power-up the ML4812 remains in the UVLO condition; output low and quiescent current low. The IC becomes operational when V_{CC} reaches 16V. When V_{CC} drops below 10V, the UVLO condition is imposed. During the UVLO condition, the 5V V_{REF} pin is "off", making it usable as a "flag" for starting up a downstream PWM converter.

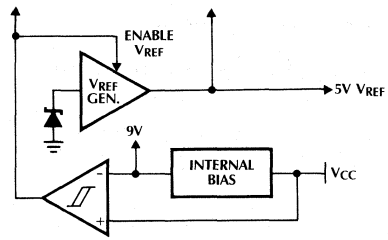


Figure 8. Under-Voltage Lockout Block Diagram

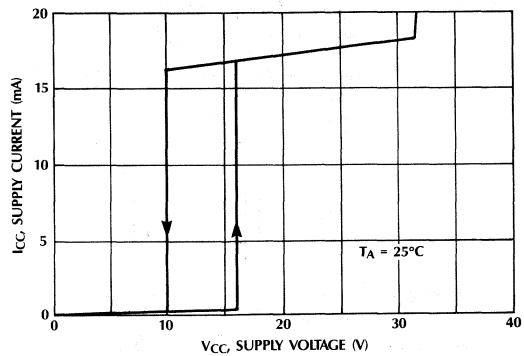


Figure 9a. Total Supply Current vs. Supply Voltage

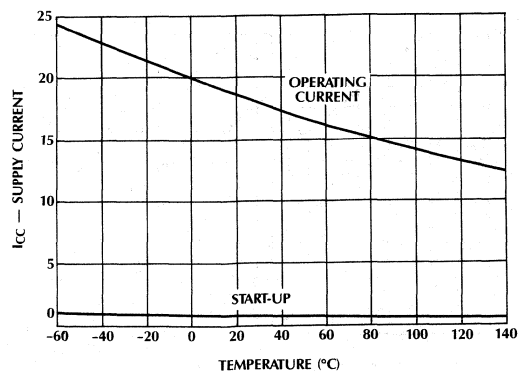


Figure 9b. Supply Current (I_{CC}) vs. Temperature

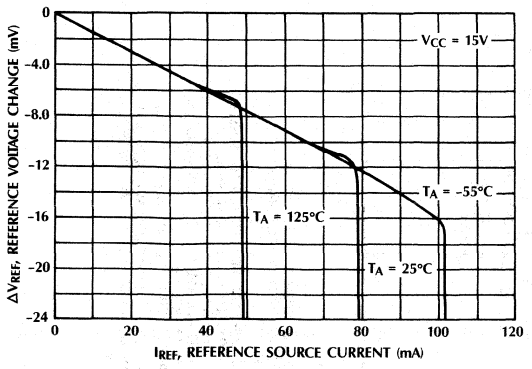


Figure 10. Reference Load Regulation

APPLICATIONS

INPUT INDUCTOR (L1) SELECTION

The central component in the regulator is the input boost inductor. The value of this inductor controls various critical operational aspects of the regulator. If the value is too low, the input current distortion will be high and will result in low power factor and increased noise at the input. This will require more input filtering. In addition, when the value of the inductor is low the inductor dries out (runs out of current) at low currents. Thus the power factor will decrease at lower power levels and/or higher line voltages. If the inductor value is too high, then for a given operating current the required size of the inductor core will be large and/or the required number of turns will be high. So a balance must be reached between distortion and core size.

One more condition where the inductor can dry out is analyzed below where it is shown to be maximum duty cycle dependent.

For the boost converter at steady state:

$$V_{OUT} = \frac{V_{IN}}{1 - D_{ON}} \quad (1)$$

Where D_{ON} is the duty cycle $[T_{ON}/(T_{ON} + T_{OFF})]$. The input boost inductor will dry out when the following condition is satisfied:

$$V_{IN}(t) < V_{OUT} \times (1 - D_{ON}) \quad (2)$$

or

$$V_{INDRY} = [1 - D_{ON}\ (max)] \times V_{OUT} \quad (3)$$

V_{INDRY}: Voltage where the inductor dries out.
V_{OUT}: Output dc voltage.

Effectively, the above relationship shows that the resetting volt-seconds are more than setting volt-seconds. In energy transfer terms this means that less energy is stored in the inductor during the ON time than it is asked to deliver during the OFF time. The net result is that the inductor dries out.

The recommended maximum duty cycle is 95% at 100KHz to allow time for the input inductor to dump its energy to the output capacitors.

For example:

if: V_{OUT} = 380V and
D_{ON} (max) = 0.95

then substituting in (3) yields V_{INDRY} = 20V. The effect of drying out is an increase in distortion at low voltages.

For a given output power, the instantaneous value of the input current is a function of the input sinusoidal voltage waveform, i.e. as the input voltage sweeps from zero volts to a maximum value equal to its peak so does the current.

The load of the power factor regulator is usually a switching power supply which is essentially a constant power load. As a result, an increase in the input voltage will be offset by a decrease in the input current.

By combining the ideas set forth above, some ground rules can be obtained for the selection and design of the input inductor:

Step 1: Find minimum operating current.

$$I_{IN}(min)_{PEAK} = \frac{1.414 \times P_{IN}(min)}{V_{IN}(max)} \quad (4)$$

$V_{IN}(max)$ = 260V
$P_{IN}(min)$ = 50W
then: $I_{IN}(min)_{PEAK}$ = 0.272A

Step 2: Choose a minimum current at which point the inductor current will be on the verge of drying out. For this example 40% of the peak current found in step 1 was chosen.

then: I_{LDRY} = 100mA

Step 3: The value of the inductance can now be found using previously calculated data.

$$L1 = \frac{V_{INDRY} \times D_{ON}(max)}{I_{LDRY} \times f_{OSC}} \quad (5)$$

$$= \frac{20V \times 0.95}{100mA \times 100KHz} = 2mH$$

The inductor can be allowed to decrease in value when the current sweeps from minimum to maximum value. This allows the use of smaller core sizes. The only requirement is that the ramp compensation must be adequate for the lower inductance value of the core so that there is adequate compensation at high current.

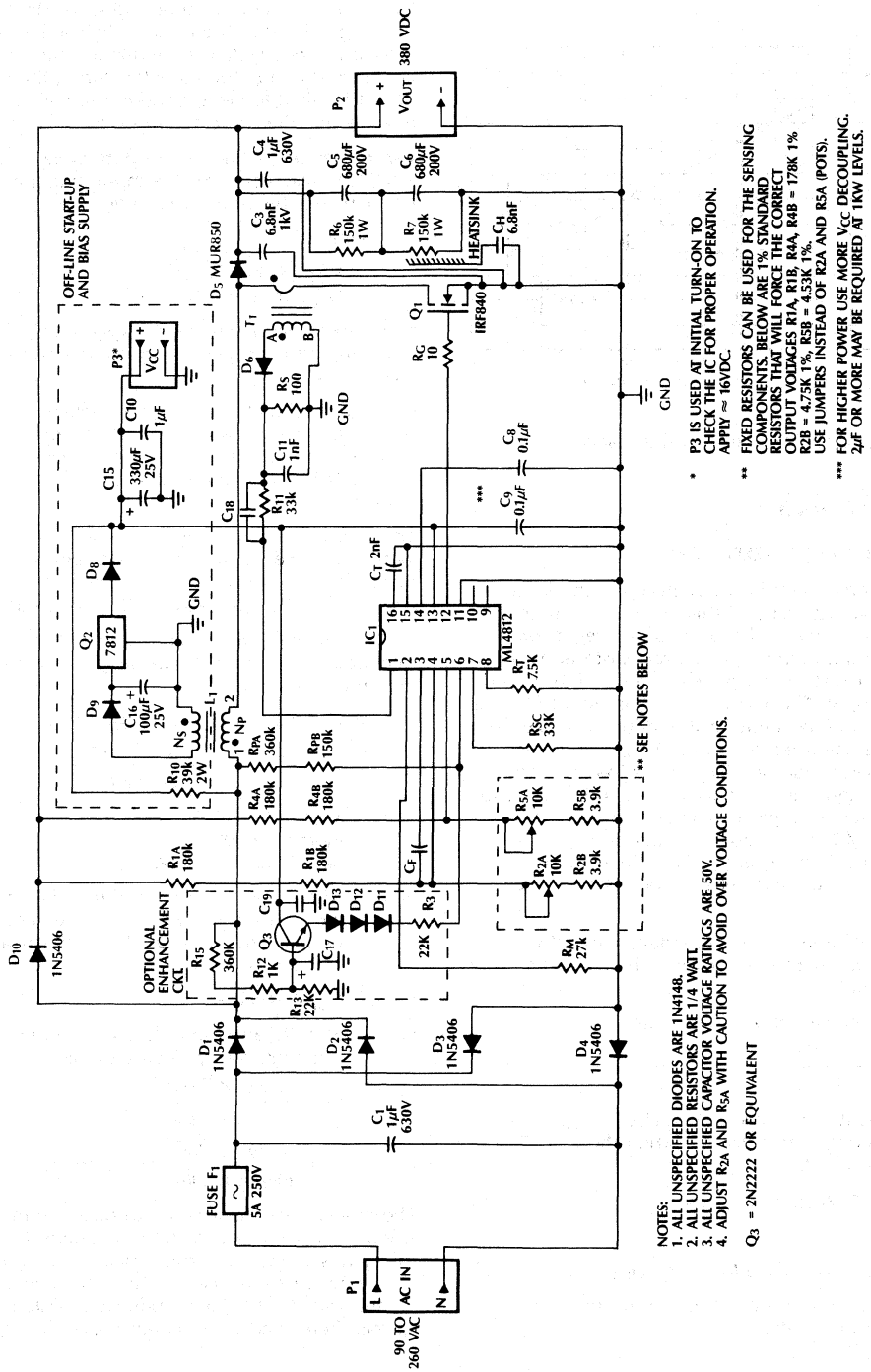


Figure 11. Typical Application, 200W Power Factor Correction Circuit

Step 4: The presence of the ramp compensation will change the dry out point, but the value found above can be considered a good starting point. Based on the amount of power factor correction the above value of L1 can be optimized after a few iterations.

Gapped Ferrites, Molypermalloy, and Powdered Iron cores are typical choices for core material. The core material selected should have a high saturation point and acceptable losses at the operating frequency.

One ferrite core that is suitable at around 200W is the #4229PL00-3C8 made by Ferroxcube. This ungapped core will require a total gap of 0.180" for this application.

OSCILLATOR COMPONENT SELECTION

The oscillator timing components can be calculated by using the following expression:

$$f_{OSC} = \frac{1.36}{R_T \times C_T} \quad (6)$$

For example:

Step 1: At 100KHz with 95% duty cycle T_{OFF} = 500ns calculate C_T using the following formula:

$$C_T = \frac{T_{OFF} \times I_{DIS}}{V_{OSC}} = 1000pF \quad (7)$$

Step 2: Calculate the required value of the timing resistor.

$$R_T = \frac{1.36}{f_{OSC} \times C_T} = \frac{1.36}{100KHz \times 1000pF} \quad (8)$$

$$= 13.6K\Omega \text{ choose } R_T = 14K\Omega.$$

CURRENT SENSE AND SLOPE (RAMP) COMPENSATION COMPONENT SELECTION

Slope compensation in the ML4812 is provided internally. Rather than adding slope to the noninverting input of the PWM comparator it is actually subtracted from the voltage present at the inverting input of the PWM comparator. The amount of slope compensation should be at least 50% of the downslope of the inductor current during off time as reflected to the inverting input of the PWM comparator. Note that slope compensation is required only when the inductor current is continuous and the duty cycle is more than 50%. The downslope of the inductor current at the verge of discontinuity can be found using the expression given below:

$$\frac{di_L}{dt} = \frac{V_{OUT} - V_{IN\ DRY}}{L} = \frac{380V - 20V}{2mH} \quad (9)$$

$$= 0.18\ A/\mu s$$

The downslope as reflected to the input of the PWM comparator is given by:

$$S_{PWM} = \frac{V_{OUT} - V_{IN\ DRY}}{L} \times \frac{R_S}{N_C} \quad (10)$$

Where R_S is the current sense resistor and N_C is the turns ratio of the current transformer (T1) used. In general, current transformers simplify the sensing of switch currents especially at high power levels where the use of sense resistors is complicated by the amount of power they have to dissipate. Normally the primary side of the transformer consists of a single turn and the secondary consists of several turns of either enameled magnet wire or insulated wire. The diameter of the ferrite core used in this example is 0.5" (SPANG/Magnetics F41206-TC). The rectifying diode at the output of the current transformer can be a 1N4148 for secondary currents up to 75mA average.

Sense FETs or resistive sensing can also be used to sense the switch current, the sensed signal has to be amplified to the proper level before it is applied to the ML4812.

The value of the ramp compensation (SC_{PWM}) as seen at the inverting terminal of the PWM comparator is:

$$SC_{PWM} = \frac{2.5 \times R_M}{R_T \times C_T \times R_{SC}} \quad (11)$$

The required value for R_{SC} can therefore be found by equating:

$$SC_{PWM} = A_{SC} \times S_{PWM}$$

where A_{SC} is the amount of slope compensation and solving for R_{SC}.

The value of R_M (pin 2) depends on the selection of R_P (pin 6)

$$R_P = \frac{V_{IN}(max)_{PEAK}}{I_{SINE}(peak)} = \frac{260 \times 1.414}{0.5mA} = 750K \quad (12)$$

$$R_M = \frac{V_{CLAMP} \times R_P}{V_{IN}(min)_{PEAK}} = \frac{4.9 \times 750K}{90 \times 1.414} = 28.8K \quad (13)$$

The peak of the inductor current can be found approximately by:

$$I_{LPEAK} = \frac{1.414 \times P_{OUT}}{V_{IN}(min)_{RMS}} = \frac{1.414 \times 200}{90} = 3.14A \quad (14)$$

Selection of N_C which depends on the maximum switch current, assume 4A for this example is 80 turns.

$$R_S = \frac{V_{CLAMP} \times N_C}{I_{LPEAK}} = \frac{4.9 \times 80}{4} = 100\Omega \quad (15)$$

Where R_S is the sense resistor, and V_{CLAMP} is the current clamp at the inverting input of the PWM comparator. This clamp is internally set to 5V. In actual application it is a good idea to assume a value less than 5V to avoid unwanted current limiting action due to component tolerances. In this application V_{CLAMP} was chosen as 4.9V.

Having calculated R_S the value S_{PWM} and of R_{SC} can now be calculated:

$$S_{PWM} = \frac{380V - 20}{2mH} \times \frac{100}{80} = 0.225V/\mu s$$

$$R_{SC} = \frac{2.5 \times R_M}{A_{SC} \times S_{PWM} \times R_T \times C_T} \quad (16)$$

$$R_{SC} = \frac{2.5 \times 28.8K}{0.7 \times (.225 \times 10^6) \times 14K \times 1nF} = 33K$$

The following values were used in the calculation:

R_M = 28.8K A_{SC} = 0.7
R_T = 14K C_T = 1nF

VOLTAGE REGULATION COMPONENTS

The values of the voltage regulation loop components are calculated based on the operating output voltage. Note that voltage safety regulations require the use of sense resistors that have adequate voltage rating. As a rule of thumb if 1/4W resistors are available, two of them should be used in series. The input bias current of the error amplifier is approximately 0.5μA, therefore the current available from the voltage sense resistors should be significantly higher than this value. Since two 1/4W resistors have to be used the total power rating is 1/2W. The operating power is set to be 0.4W then with 380V output voltage the value can be calculated as follows:

$$R_1 = (380V)^2/0.4W = 360K \quad (17)$$

Choose two 178K, 1% connected in series.

Then R_2 can be calculated using the formula below:

$$R_2 = \frac{V_{REF} \times R_1}{V_{OUT} - V_{REF}} = \frac{5V \times 356K}{380V - 5V} = 4.747K \quad (18)$$

Choose 4.75K, 1%. One more critical component in the voltage regulation loop is the feedback capacitor for the error amplifier. The voltage loop bandwidth should be set such that it rejects the 120Hz ripple which is present at the output. If this ripple is not adequately attenuated it will cause distortion on the input current waveform. Typical bandwidths range anywhere from a few Hertz to 15Hz. The main compromise is between transient response and distortion. The feedback capacitor can be calculated using the following formula:

$$C_F = \frac{1}{3.142 \times R_1 \times BW} \quad (19)$$

$$C_F = \frac{1}{3.142 \times 356K \times 2Hz} = 0.44\mu F$$

OVERVOLTAGE PROTECTION (OVP) COMPONENTS

The OVP loop should be set so that there is no interaction with the voltage control loop. Typically it should be set to a level where the power components are safe to operate. Ten to fifteen volts above V_{OUT} seems to be adequate. This sets the maximum transient output voltage to about 395V.

By choosing the high voltage side resistor of the OVP circuit the same way as above i.e. R_4 = 356K then R_5 can be calculated as:

$$R_5 = \frac{V_{REF} \times R_4}{V_{OVP} - V_{REF}} = \frac{5V \times 356K}{395V - 5V} = 4.564K \quad (20)$$

Choose 4.53K, 1%.

Note that R_1, R_2, R_4 and R_5 should be tight tolerance resistors such as 1% or better.

CONTROLLER SHUTDOWN

The ML4812 provides a shutdown pin which could be used to shutdown the IC. Care should be taken when this pin is used because power supply sequencing problems could arise if another regulator with its own bootstrapping follows the ML4812. In such a case a special circuit should be used to allow for orderly start up. One way to accomplish this is by using the reference voltage of the ML4812 to inhibit the other controller IC or to shut down its bias supply current.

OFF-LINE START-UP AND BIAS SUPPLY GENERATION

The ML4812 can be started using a "bleed resistor" from the high voltage bus. After the voltage on pin 13 (V_{CC}) exceeds 16V, the IC starts up. The energy stored on the 330μF, C15, capacitor supplies the IC with running power until the supplemental winding on L1 can provide the power to sustain operation.

The values of the start-up resistor R10 and capacitor C15 may need to be optimized depending on the application. The charging waveform for the secondary winding of L1 is an inverted chopped sinusoid which reaches its peak when the line voltage is at its minimum. In this example, C9 = .1μF, C15 = 330μF, D8 = 1N4148 R10 = 39K, 2W.

ENHANCEMENT CIRCUIT

The theory of operation of the power factor enhancement circuit (inside the dotted lines) in Figure 11 is described in APPLICATION NOTE 11 in detail. It improves the power factor and lowers the input current harmonics. Note that the circuit meets the proposed IEC 555 specifications (with the enhancement) on the harmonics with a large margin while correcting the input power factor to better than 0.99 under most steady state operating conditions.

CONSTRUCTION AND LAYOUT TIPS

High frequency power circuits require special care during breadboard construction and layout. Double sided printed circuit boards with ground plane on one side are highly recommended. All critical switching leads (power FET, output diode, IC output and ground leads, bypass capacitors) should be kept as small as possible. This is to minimize both the transmission and pick-up of switching noise.

There are two kinds of noise coupling; inductive and capacitive. As the name implies inductive coupling is due to fast changing (high di/dt) circulating switching currents. The main source is the loop formed by Q1, D5, and C3–C4. Therefore this loop should be as small as possible, and the above capacitors should be good high frequency types.

The second form of noise coupling is due to fast changing voltages (high dv/dt). The main source in this case is the drain of the power FET. The radiated noise in this case can be minimized by insulating the drain of the FET from the heatsink and then tying the heatsink to the source of the FET with a high frequency capacitor (C_H in Figure 11).

The IC has two ground pins named PWR GND and Signal GND. These two pins should be connected together with a very short lead at the printed circuit board exit point. In general grounding is very important and ground loops should be avoided. Star grounding schemes are preferred.

Component Values/Bill of Materials for Figure 11

Reference	Description
C1, C4	1μF, 630V Film (250 VAC)
C3, C_H	6.8nF 1KV Ceramic disk
C5, C6	680μF 200V Electrolytic
C8, C9	.1μF 50V Ceramic
C10, C19	1μF 50V Ceramic
C11	.001μF 50V Ceramic
C15	330μF 25V Electrolytic
C16	100μF 25V Electrolytic
C17	10μF 25V Electrolytic
C_F	.47μF 50V Ceramic
C_T	.002μF 50V Ceramic
D1, D2, D3, D4, D10	1N5406 (Motorola)
D5	MUR850 (Motorola)
D6, D8, D9, D11, D12, D13	1N4148
F1	5A 250V 3AG with clips
IC1	ML4812CP (Micro Linear)
L1	2mH, 4A I_{PEAK} (see below)
Q1	IRF840 or MTPN8N50

Reference	Description
Q2	LM7815CT
Q3	2N2222 or equivalent
R1A, R1B, R4A, R4B	180KΩ
R2A, R5A	10KΩ TRIMPOT BOURNS 3299 or equivalent
R2B, R5B	3.9KΩ
R3, R13	22KΩ
R6, R7, RPB	150KΩ
R10	39KΩ, 2W
R11	33KΩ
R12	1KΩ
RG	10Ω
RM	27KΩ
RPA, R15	360KΩ
RS	100Ω
RSC	33KΩ
RT	7.5KΩ
T1	SPANG F41206-TC N_S = 80, N_P = 1 (see attached)

Notes: All resistors 1/4W unless otherwise specified. Some reference designators are skipped (e.g. C2, C12, etc.) and do not appear on the schematic. These designators were used in previous revisions of the board and are not used on this revision. Additional information on key components is included in the attached appendix.

Magnetics Tips (Refer to Figure 11)

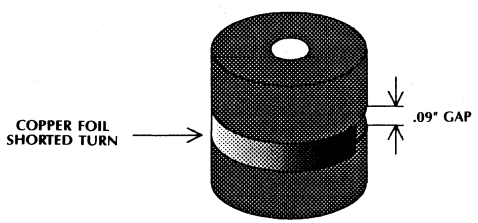
L1 — Main inductor:

One of several toroidal cores can be used for L1:

Material	Manufacturer	Part #	Turns (#24AWG)
Powdered Iron	Micrometals	T225-8/90	200
Powdered Iron	Micrometals	T184-40	120
Molypermalloy	SPANG (Mag. Inc.)	58076-A2 (high flux)	180

The T184-40 core above is the most economical, but has lower inductance at high current. This would yield higher ripple current and require more line EMI filtering. The value for RSC (slope compensation resistor on Pin 7) was calculated for the T225-8/90 and should be recalculated for other inductor characteristics. Selected pages of the Micrometals iron powder core data sheets are attached for your convenience. The core manufacturer also has additional applications literature available.

A gapped ferrite core can also be used in place of the powdered iron core. One such core is a Ferroxcube core #4229PL00-3C8. This is an un-gapped core. Using 145 turns of #24 AWG wire, a total air gap of .180" is required to give a total inductance of about 2mH. Since 1/2 of the gap will be on the outside of the core and 1/2 the gap on the inside, putting a .09" spacer in the center will yield a .180" total gap. To prevent leakage fields from generating RFI, a shorted turn of copper tape should be wrapped around the gap as shown below:



For production, a gapped center leg can be ordered from most core vendors, eliminating the need for the external shorted copper turn when using a pot core.

T1 — Sense Transformer

In addition to the core type mentioned in the parts list, the following Siemens cores should be suitable for substitution and may be more readily available in Europe.

Material	Size Code	Part #
N27	R16/6.3	B64290-K45-X27
N30	R16/6.3	B64290-K45-X830

The N27 material is for high frequency and will work better above 100kHz but both are adequate. In addition, Ferroxcube/Phillips Magnetics core 768T188-3C8 can be used.

U.S. Core Vendors:

Manufacturer	Phone Number
SPANG/Magnetics Inc.	(412) 282-8282
Micrometals	(800) 356-5977
Ferroxcube/Phillips Magnetics	(818) 998-7311

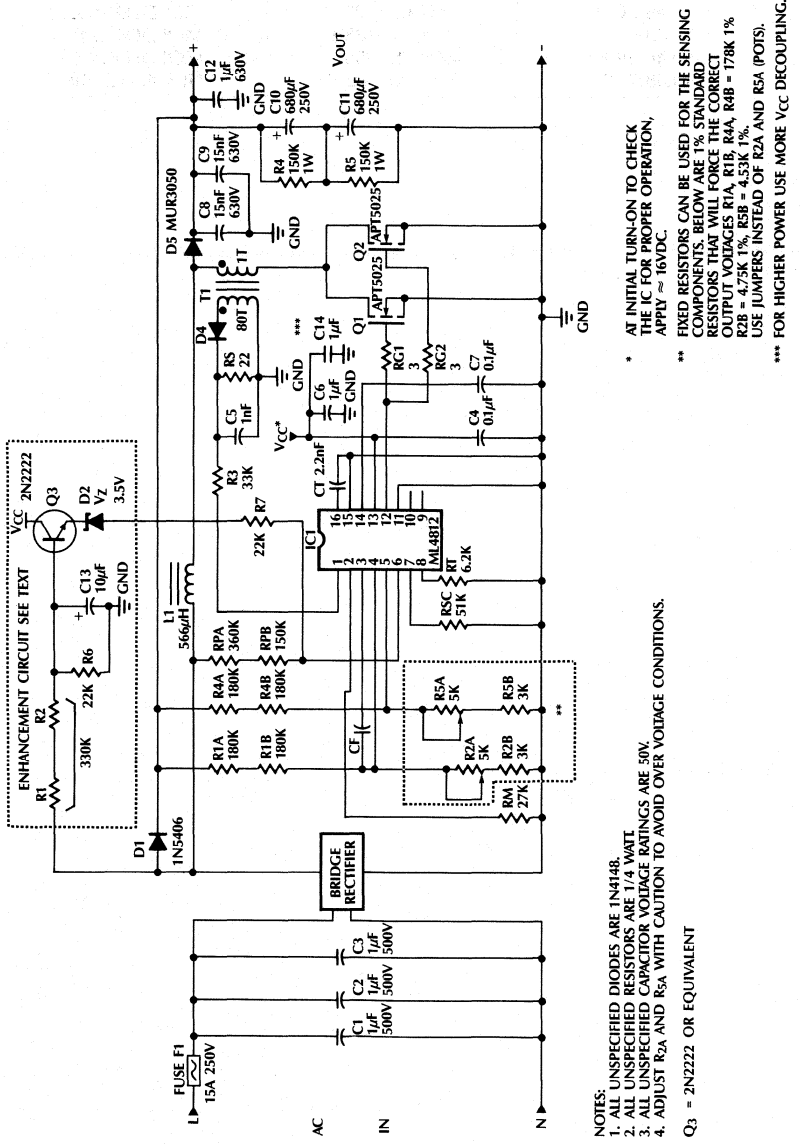


Figure 12. 1KW Input Power, Power Factor Correction Circuit

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ML4812CP	0°C to +70°C	MOLDED DIP
ML4812CQ	0°C to +70°C	MOLDED PCC
ML4812IP	–40°C to +85°C	MOLDED DIP
ML4812IQ	–40°C to +85°C	MOLDED PCC
ML4812MJ	–55°C to +125°C	HERMETIC DIP

Micro Linear

ML4812-EVAL

Power Factor Controller Evaluation Kit

GENERAL DESCRIPTION

The ML4812 EVAL kit provides a convenient vehicle to evaluate the ML4812 Power Factor Correction circuit. The board implements a 200W "boost" type power factor correction system. Special care has been taken in the layout of this PC board to provide adequate space for probes and a large area for ground plane to increase system noise immunity.

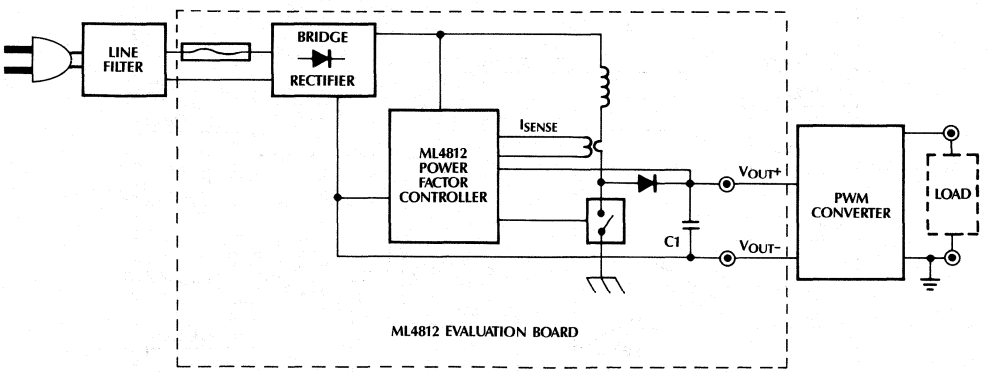
This kit includes a blank PC board, schematic of a complete power factor correction system and specifications for the key external components necessary to build a prototype Power Factor Correction front end. The unit is designed to operate over a 90VAC to 265VAC line range and can run from no load to a full 200W. Higher power levels can be achieved using this board by using larger external components.

This boost mode converter is set to run with a 380V output and achieves power factors of better than .99 over a wide range of input line and output load.

FEATURES

- Power factor > .99
- Harmonic currents well below proposed IEC555-2 limits
- 90 to 265VAC input, 380V output to 200W
- 380VDC output to 200W
- Over-Voltage Protection
- Peak Current sense circuit protects Power MOSFET
- PC board and ML4812CP controller included
- Line and Load regulation better than 2%
- Complete documentation and applications information

BLOCK DIAGRAM



6

Micro Linear

ML4813

Flyback Power Factor Controller

GENERAL DESCRIPTION

The ML4813 is designed to optimally facilitate a discontinuous "flyback" or "buck-boost" type power factor correction system for low power, low cost applications. Special care has been taken in the design of the ML4813 to reject system noise. The circuit includes a precision reference, oscillator, error amplifier, over-voltage comparator, over-current comparator, and an extra op-amp as well as a high current output. In addition, start-up is simplified by an under-voltage lockout circuit with 6V hysteresis.

In a typical application, the ML4813 functions as a voltage mode regulator. By maintaining a constant duty cycle, the current follows the input voltage, making the impedance of the entire circuit appear purely resistive. With the flyback circuit, power factors of .99 are easily achievable with a small output inductor and a minimum of external components.

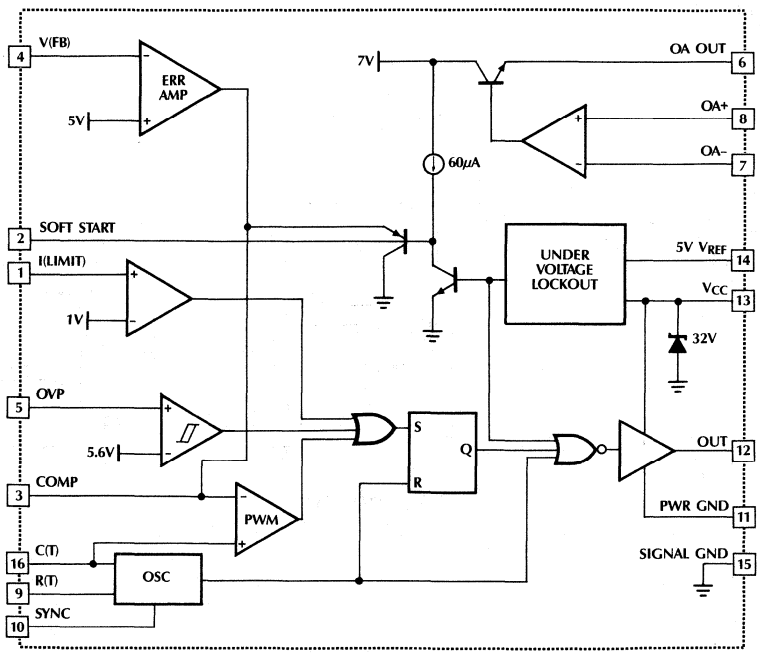
FEATURES

- Precision buffered 5V reference (±1%)
- Extra op-amp for output voltage instrumentation amplifier
- Over Current comparator for switch protection
- Soft Start and 6V hysteresis under-voltage lockout for easy low surge off-line starting
- 1 A Peak Current Totem-Pole Output Drive
- Over-Voltage comparator eliminates output "runaway" due to load removal
- Large oscillator amplitude for better noise immunity

APPLICATIONS

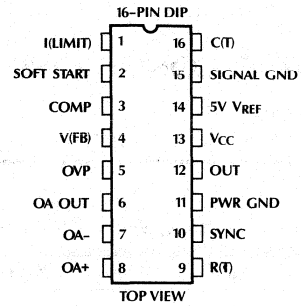
- PC power supplies
- Lamp Ballasts

BLOCK DIAGRAM (Pin out shown is for DIP)

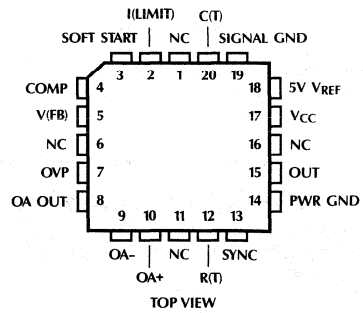


PIN CONFIGURATION

ML4813
16-Pin DIP



ML4813
20-Pin PCC



PIN DESCRIPTION (DIP)

PIN #	NAME	FUNCTION
1	I(LIMIT)	Current limit sense pin. Normally connected to sense resistor. When this pin exceeds 1V, the PWM cycle is terminated.
2	SOFT START	Normally connected to a Soft Start capacitor.
3	COMP	Output of error amplifier and input to PWM comparator.
4	V(FB)	Control loop feedback voltage.
5	OVP	Input to over voltage comparator.
6	OA OUT	Output of uncommitted op-amp.
7	OA–	Negative input of uncommitted op-amp.
8	OA+	Positive input of uncommitted op-amp.
9	R(T)	Oscillator timing resistor pin. A 5V source sets a current in the external resistor which is mirrored to charge C(T).
10	SYNC	Input used to synchronize the oscillator to an external source.
11	PWR GND	Return for the High Current Totem pole output.
12	OUT	High Current Totem pole output.
13	V_{CC}	Positive Supply for the IC.
14	5V V_{REF}	Buffered output for the 5V voltage reference.
15	SIGNAL GND	Analog signal ground.
16	C(T)	Timing Capacitor for the Oscillator.

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

Supply Current (I_{CC}) 40mA
Output Current, Source or Sink (Pin 12)
DC 1.0A
Output Energy (capacitive load per cycle) 5μJ
Error Amp Sink Current (pin 3) 10mA
Oscillator Charge Current 5mA
Analog Inputs (pins 1, 3–8) ..... –0.3V to 5.5V

Junction Temperature ..... 150°C
Storage Temperature Range ..... –65°C to +150°C
Lead Temperature (Soldering 10 sec.) ..... +260°C
Thermal Resistance (θ_{JA})
Plastic Chip Carrier (PCC) – Q ..... 60°C/W
Plastic DIP – P ..... 65°C/W

OPERATING CONDITIONS

Temperature Range
ML4813C ..... 0°C to 70°C

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, R_T = 14KΩ, C_T = 1000pF, T_A = Operating Temperature Range, V_{CC} = 15V (Note 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Oscillator					
Initial Accuracy	T_J = 25°C	90	97	104	KHz
Voltage Stability	12V < V_{CC} < 18V		0.3		%
Temperature Stability			2		%
Total Variation	line, temp.	88		108	KHz
Ramp Valley			1.0		V
Ramp Peak			4.3		V
R(T) Voltage		4.8	5.0	5.2	V
Discharge Current (pin 8 open)	T_J = 25°C, $V_{PIN\ 16}$ = 2V	7.5	8.4	9.3	mA
	$V_{PIN\ 16}$ = 2V	7.2	8.4	9.5	mA
Sync Pulse Threshold		.8	1.4	2.0	V
Sync Input Bias Current			350	800	μA
Reference Section					
Output Voltage	T_J = 25°C, I_O = 1mA	4.95	5.00	5.05	V
Line Regulation	12V < V_{CC} < 25V		6	20	mV
Load Regulation	1mA < I_O < 20mA		3	20	mV
Temperature Stability			.4		%
Total Variation	line, load, temp.	4.9		5.1	V
Output Noise Voltage	10Hz to 10KHz		50		μV
Long Term Stability	T_J = 125°C, 1000 Hrs, (note 1)		5	25	mV
Short Circuit Current	V_{REF} = 0V	–30	–85	–180	mA
Error Amplifier Section					
Input Offset Voltage		–15		15	mV
Input Bias Current			–0.1	–1.0	μA
Open Loop Gain	1 < $V_{PIN\ 3}$ < 5V	60	75		dB
PSRR	12V < V_{CC} < 25V	60	70		dB
Output Sink Current	$V_{PIN\ 3}$ = 1.1V, $V_{PIN\ 4}$ = 6.2V	2	12		mA
Output Source Current	$V_{PIN\ 3}$ = 5.0V, $V_{PIN\ 4}$ = 4.8V	–0.5	–1.0		mA
Output High Voltage	$I_{PIN\ 3}$ = –0.5mA, $V_{PIN\ 4}$ = 4.8V	6.0	6.4		V
Output Low Voltage	$I_{PIN\ 3}$ = 2mA, $V_{PIN\ 4}$ = 6.2V		0.5	1.0	V
Unity Gain Bandwidth			1.0		MHz

ELECTRICAL CHARACTERISTICS (Continued)

Unless otherwise specified, R_T = 14KΩ, C_T = 1000pF, T_A = Operating Temperature Range, V_{CC} = 15V (note 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Un-Committed Op Amp					
Input Offset Voltage		-10		10	mV
Input Bias Current			-0.1	-1.0	μA
Input Offset Current		-0.2		0.2	μA
Open Loop Gain			90		dB
PSRR		80	125		dB
Output High Voltage	$I_{PIN\ 6}$ = -20mA	7	8		V
Output Low Voltage	$R_{L(PIN\ 6)}$ = 10KΩ		.2	.5	V
I(LIMIT) Comparator					
Input Trip Point	Output Off	.8	1.0	1.2	V
Input Bias Current			-2	-15	μA
Propagation Delay			150		nS
OVP Comparator					
Input Trip Point	Output Off	5.5	5.6	5.7	V
Hysteresis	Output On		100		mV
Input Bias Current			-0.3	-3	μA
PWM Comparator					
Input Common Mode Range		-0.2		5.5	V
Input Bias Current			-2	-10	μA
Propagation Delay			150		nS
Soft Start Section					
Soft Start Current (pin 2)	$V_{PIN\ 2}$ = 1V	40	60	80	μA
Output Section					
Output Voltage Low	I_{OUT} = 20mA		0.1	0.4	V
	I_{OUT} = 200mA		1.2	2.2	V
Output Voltage High	I_{OUT} = -20mA	13	13.6		V
	I_{OUT} = -200mA	12	13.4		V
Output Voltage Low in UVLO	I_{OUT} = 5mA, V_{CC} = 8V		0.1	0.8	V
Output Rise/Fall Time	C_L = 1000pF		50		nS
Under-Voltage Lockout					
Start-up Threshold		15	16	17	V
Shut-Down Threshold		9	10	11	V
V_{REF} Good Threshold			4.4		V
Total Device					
Supply Current	Start-up, V_{CC} = 14V		.9	1.5	mA
	Operating		20	30	mA
Internal Shunt Zener Voltage	I_{CC} = 30mA	25	30	34	V

Note 1: This parameter not 100% tested in production but guaranteed by design.

Note 2: V_{CC} is raised above the Start-up Threshold first to activate the IC, then returned to 15V.

FUNCTIONAL DESCRIPTION

OSCILLATOR

The ML4813 oscillator charges the external capacitor (C_T) with a current (I_{SET}) equal to $5/R_{SET}$. When the capacitor voltage reaches the upper threshold, the comparator changes state and the capacitor discharges to the lower threshold through Q1. While the capacitor is discharging, Q2 provides a high pulse.

The Oscillator period can be described by the following relationship:

$$T_{OSC} = T_{RAMP} + T_{DEADTIME}$$

where:

$$T_{RAMP} = C \text{ (Ramp Valley to Peak)} \div I_{SET}$$

and:

$$T_{DEADTIME} = C \text{ (Ramp Valley to Peak)} \div (8.4mA - I_{SET})$$

A pulse of a duration shorter than $T_{DEADTIME}$ from an external frequency source set to a higher frequency than f_{OSC} can be applied to pin 10 to synchronize the oscillator. R(SYNC) and C(SYNC) shorten longer pulses.

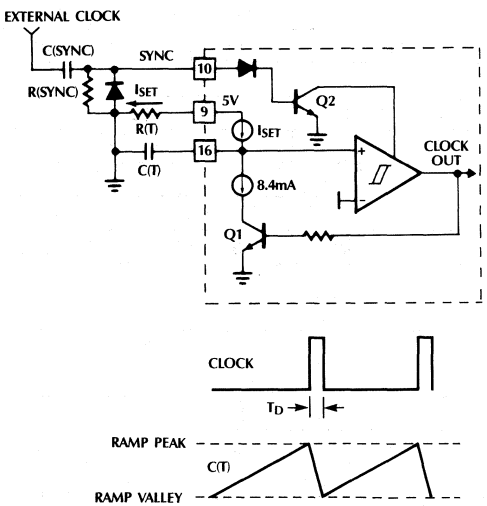


Figure 1. Oscillator Block Diagram

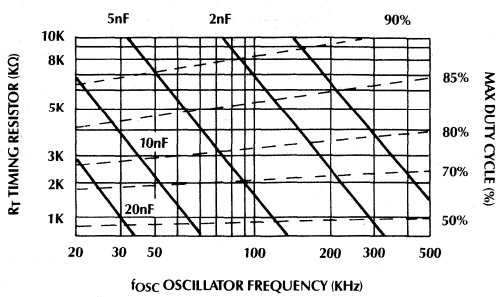


Figure 2. Oscillator Timing Resistance vs. Frequency

OUTPUT DRIVER STAGE

The ML4813 Output Driver is a 1A peak output high speed totem pole circuit designed to quickly drive capacitive loads, such as power MOSFET gates.

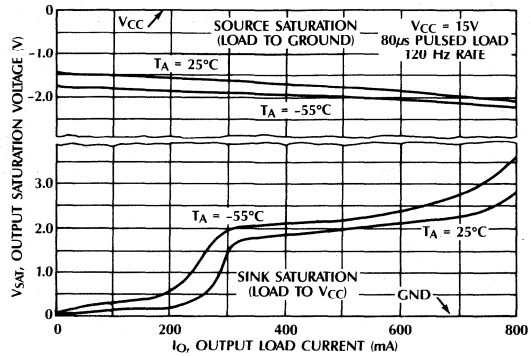


Figure 3. Output Saturation Voltage vs. Output Current

ERROR AMPLIFIER

The ML4813 error amplifier is a high open loop gain, wide bandwidth, amplifier.

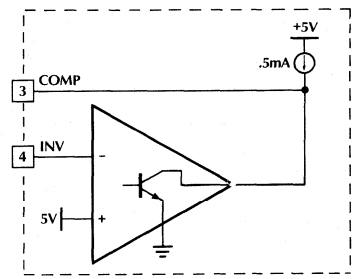


Figure 4. Error Amplifier Configuration

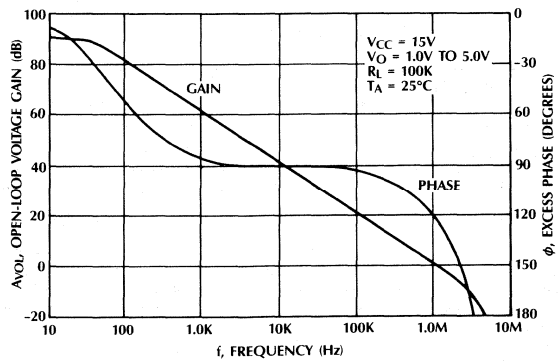


Figure 5. Error Amplifier Open-Loop Gain and Phase vs. Frequency

UN-COMMITTED OP-AMP

The ML4813 contains an un-committed op-amp which is normally configured as a differencing amplifier to sense the output voltage. The output voltage in the flyback configuration is not ground referenced. The op-amp in the ML4813 is a PNP input amplifier similar to the LM324 but with an open emitter output stage (class A).

UNDER VOLTAGE LOCKOUT

On power-up the ML4813 remains in the UVLO condition; output low and quiescent current low. The IC becomes operational when V_{CC} reaches 16V. When V_{CC} drops below 10V, the UVLO condition is imposed. During the UVLO condition, the 5V V_{REF} pin is "off", making it usable as a "flag" for starting up a down-stream PWM converter.

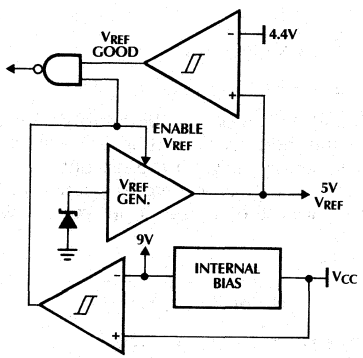


Figure 6. Under-Voltage Lockout Block Diagram

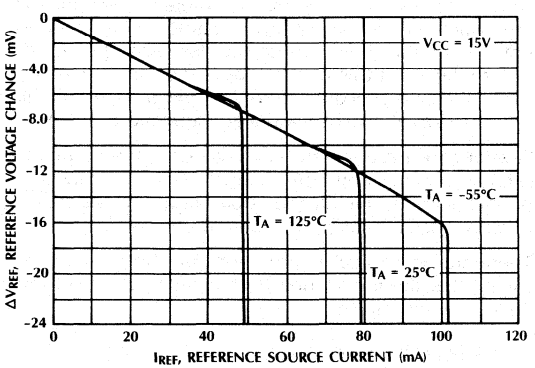


Figure 7. Reference Load Regulation

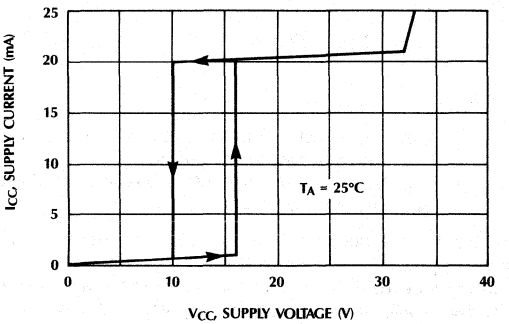


Figure 8. Total Supply Current vs. Supply Voltage

APPLICATIONS

The ML4813 is used to implement a discontinuous mode flyback (buck-boost) power factor regulator. This topology is particularly well suited for low power applications such as: fluorescent ballasts; and low power switching supplies. Also it is a useful topology when there is a requirement for the output voltage to be lower than the peak input voltage, or where an isolated output is required. This is not possible with the boost topology, where the output voltage must always be higher than the maximum peak of the input voltage range. The typical input range for the flyback power factor regulator is from 90 VAC to 260 VAC.

The regulator operates in the discontinuous inductor current conduction mode. The inductor energy stored during the "ON" time of the power switch Q is completely delivered to the output capacitance during the "OFF" time. At steady state conditions, the inductor current at the beginning of the "ON" time starts to ramp-up from 0 Amps to a value that is determined by the instantaneous value of the input full wave rectified voltage; the "ON" time as it is set by the error amplifier and the PWM comparator; and finally by the inductor itself (L).

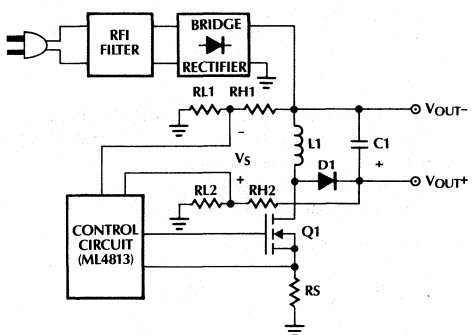


Figure 9. Block Diagram of the Regulator

The expression for the inductor peak current is given by:

$$I_L(\theta) = \frac{V_{IN}(\theta)t_{ON}}{L} \quad (1)$$

Where:

$I_L(\theta)$ = The instantaneous peak inductor current.
t_{ON} = Power switch "on" time.
$V_{IN}(\theta) = V_P \sin \theta$ = Instantaneous Input Voltage.
V_P = Input Peak Voltage.

Figure 10, is a diagram of the relationship between the low frequency envelope and the high frequency inductor current. Note that for clarity the scale between the two waveforms has not been preserved. Normally for 60Hz input line and 100KHz switching frequency, each half of the sine wave contains approximately 833 high frequency triangular waveforms.

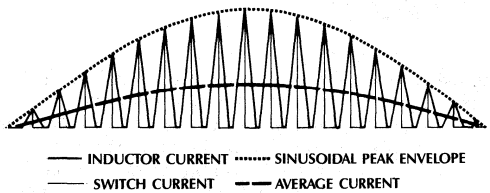


Figure 10. Switch and Line Currents in the Flyback PFC Circuit

The envelope of the peaks of the switch current, which in this case represent the current drawn from the input source, have a sinewave shape. This relationship is shown as:

$$I_L(\theta) = I_P \sin \theta \quad (2)$$

Combining (1) and (2) the following useful relationship is obtained:

$$t_{ON} = \frac{L\ I_P}{\sqrt{2}\ V_{RMS}} \quad (3)$$

Note that $V_{IN}(\theta) = V_P \sin \theta$, and also $V_P = \sqrt{2}\ V_{RMS}$. The average value of the input triangular current is:

$$I_{AVG}(\theta) = \frac{t_{ON}}{2T}\ I_P \sin \theta \quad (4)$$

Where:

I_{AVG} = Average value of the switch current. This is the value of the current at the input of the regulator after filtering.
t_{ON} = Switch "on" time.
T = Period of the switch cycle.

Substitution of (3) into (4) yields.

$$I_{AVG}(\theta) = \frac{L\ I_P^2}{2.828\ T\ V_{RMS}} \sin \theta \quad (5)$$

Equation (5) clearly shows that the average value of the switch current is sinusoidal and in phase with the input voltage. The peak value of the average current is:

$$I_{AVG(PEAK)} = \frac{L\ I_P^2}{2.828\ T\ V_{RMS}} \sin \theta \quad (6)$$

Also:

$$I_{AVG(PEAK)} = \frac{\sqrt{2}\ P_{IN}}{V_{RMS}} \quad (7)$$

Solving equations (7) and (6) for P_{IN}:

$$P_{IN} = \frac{1}{4}\ L\ I_P^2\ f \quad (8)$$

For optimum performance and the lowest inductor peak currents, the inductor current should be at the verge of continuity at the lowest operating voltage point and at full load. The above can be satisfied if:

$$I_P \leq \frac{V_{IN}\ V_{OUT}}{f\ L(V_{IN} + V_{OUT})} \quad (9)$$

Where: $V_{IN} = \sqrt{2} \times V_{IN\ MIN\ (RMS)}$

Finally (8) and (9) can be combined to derive an upper bound for the inductor value that will guarantee that the regulator always stays in the discontinuous mode of operation. If the regulator were to operate in the continuous mode the average input current would not be sinusoidal.

$$L \leq \left[\frac{V_{IN}\ V_{OUT}}{2\sqrt{f\ P_{IN}}\ (V_{IN} + V_{OUT})}\right]^2 \quad (10)$$

FLYBACK INDUCTOR CALCULATION

Equation (10) gives the upper bound for the inductor value for any set of specified operating conditions. Normally a few iterations may be required, for finalizing the value. The reason for this is that equation (10) does not contain parameters to correct for second or third order effects. All this means that a good initial value for the inductor is probably 10 to 20% lower than the value calculated by the right hand side expression in (10).

Several core materials are candidates for the inductor, such as: powder iron cores, gapped ferrites, moly permalloy cores, etc. In the application that will be described later, a gapped ferrite core is used.

There are no particular restrictions on the inductor except that the inductance is of correct value and the losses are acceptable.

INPUT BYPASS CAPACITANCE

The triangular high frequency current is bypassed by the input capacitor (C_I) labeled C_7 in Figure 12. This is a high quality film capacitor with low ESR value for minimum losses and heating. A polyester, polypropylene or x-type (for line side) is a good candidate. Typical values, depending on the power level, can range anywhere from 0.33μF to 1.5μF. The

next filtering stage of the RFI filter which has an inductor as input isolates C_7 from the other capacitors which may be present at the input circuit. Note that C_I (C_7) can be on either side of the bridge rectifier. The preferred location for low crossover distortion is at the input side. The voltage ripple across this capacitor is:

$$V_{C(P-P)} = \frac{D}{C_I f}\sqrt{\frac{P_{IN}}{Lf}} - \frac{\sqrt{2}\,P_{IN}}{C_I f\,V_{IN}} \qquad (11)$$

Where:

$V_{C(P-P)}$ = Peak to peak worst case high frequency capacitor voltage.
D = Switch Duty Cycle.

Therefore the RFI filter that follows has to be able to attenuate $V_{C(P-P)}$ to the levels set by the relevant regulatory specifications.

INPUT TRANSIENT OVERVOLTAGE PROTECTION

Careful examination of the power circuits reveals that there is no large capacitance at the input of the regulator. The only capacitances present are the RFI filter capacitors. These capacitors have a combined value in the range of a couple of microfarads. Thus their ability to absorb and minimize any line induced transients is almost non existent. Transients can occur also under sudden load removal. If the line impedance is inductive, hazardous drain source voltages may be generated leading to the destruction of the power switch. To keep this from happening a transient over-voltage protection device should be chosen such that enough safety margin is allowed for the power switch. A good rule of thumb is:

$$B_{VDSS} > V_{ZA} + V_{OUT(OVP)} \qquad (12)$$

Where:

B_{VDSS} = Drain-Source breakdown voltage for the FET.
V_{ZA} = Activation or clamping voltage of the over-voltage transient protector.
$V_{OUT(OVP)}$ = Maximum output voltage. This is set by the OVP function of the controller, and will be covered later.

THE OUTPUT CIRCUIT

The output circuit for this topology, although it is non-isolated, does not share the same ground with the power circuit. Therefore connecting the two grounds with the measuring leads of instruments should be avoided. This is a common mistake especially with the oscilloscope leads.

The output voltage "rides" on the input voltage when the (+) output is measured with respect to PGND (figure 11).

The extra OP-AMP provided in the ML4813 is used to sense the output voltage for regulation and over voltage conditions. This op-amp is connected as a difference amplifier with its output referenced to PGND. Resistors RH1, RH2, RL1, RL2 are used to scale down the voltage.

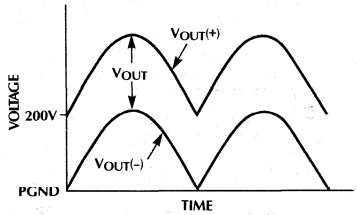


Figure 11. Output Voltage with Respect to PGND

Normally RH1 = RH2 = RH and RL1 = RL2 = RL. Then the voltage designated as V_S in Figure 9 is given by:

$$V_S = V_{OUT}\frac{RL}{RH + RL} \qquad (13)$$

OUTPUT CAPACITANCE

The output capacitance should be calculated such that it has the required output ripple at the worst case operating point. In addition the ESR should be sufficiently low to prevent dissipation due to RMS currents. The first criterion can be met by choosing the value of the output capacitor based on the following:

$$C \geq \frac{P_{IN}}{2\pi f_L\,\Delta V_R\,V_{OUT}} \qquad (14)$$

Where:

C = Total output capacitance.
P_{IN} = Total input power.
ΔV_R = Peak output capacitor ripple voltage.
V_{OUT} = Output Voltage.
f_L = Line Frequency times 2 (120 for 60Hz line).

The second criterion for the selection of the output capacitor can be satisfied by choosing a component with adequately low ESR value, that can safely bypass the RMS currents.

OUTPUT DIODE

The output diode can be a "fast" or ultrafast" type depending on the operating frequency. Reverse recovery losses are low since at steady state and under normal operating conditions the regulator operates in discontinuous current mode. The diode should be rated to handle the output current. The resulting power dissipation will be the forward drop of the diode times the output current.

POWER SWITCH

If a power FET is used, it should be sized for the required efficiency. Lower $R_{DS(ON)}$ devices will yield lower losses, but if they are operated at high frequencies (100KHz) higher charge dumping losses (1/2 $C_{DS}\,V_{DS}^2\,f$) will be experienced. The RMS current value through the power FET and the sensing resistor is:

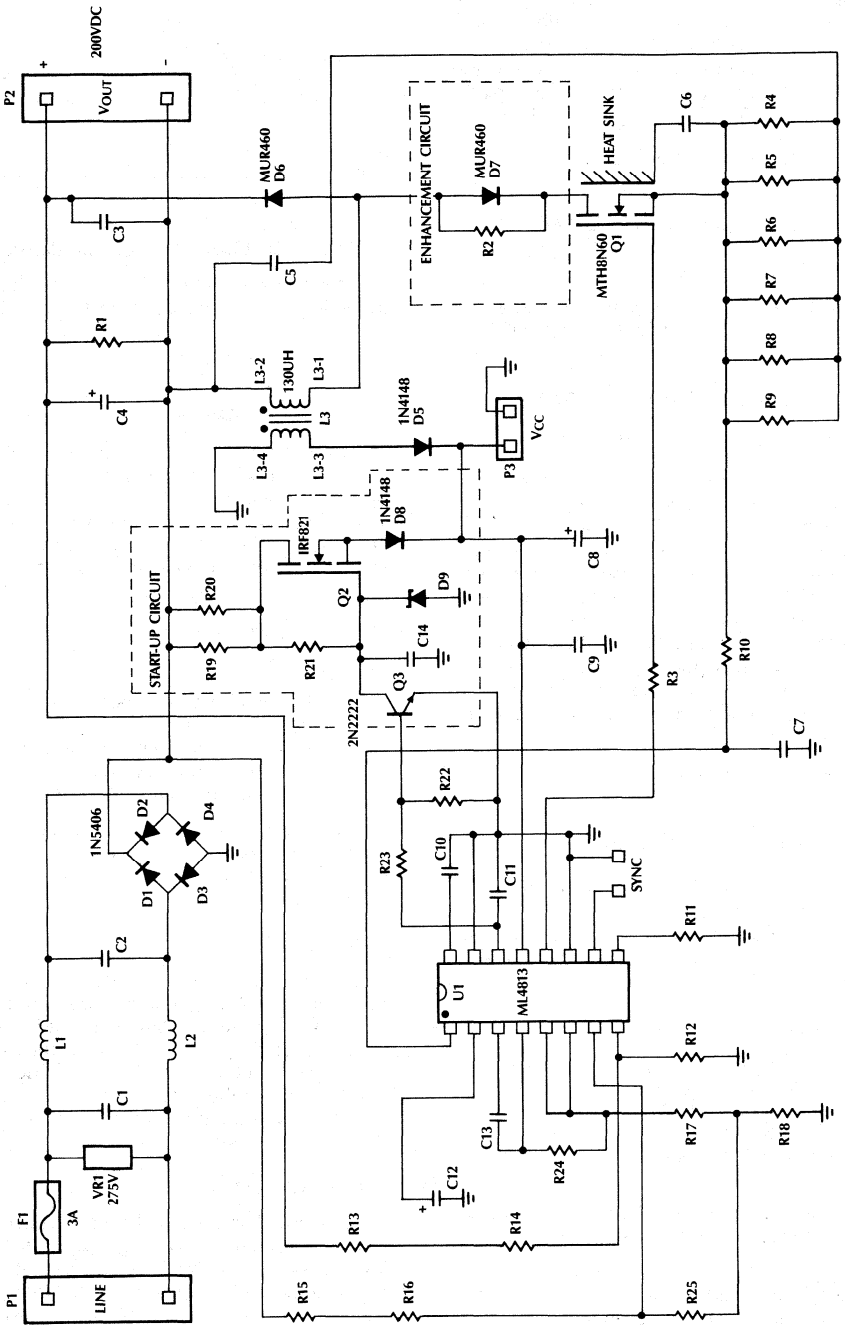


Figure 12. ML4813 Typical Application: 80W Flyback Power Factor Regulator

$$I_{RMS} = \sqrt{\frac{L\ I_P^3\ f_L}{3\sqrt{2}\ V_{RMS}}} \sqrt{\sum_{k=1}^{r} \sin^2 \frac{k\pi}{r}} \qquad (15)$$

Where:

I_{RMS} = Total RMS current through the power FET and sense resistor.
f_L = Line Frequency times 2 (120 for 60Hz line).
$r = f_{SWITCH}/f_L$.

Table 1 is provided to assist in calculating (15) above. When the power switch is a bipolar transistor (constant V_{CE} drop) then the power dissipation produced can be calculated by using (16):

$$P_D = \frac{0.9\ P_{IN}}{V_{RMS}} V_{CE} \qquad (16)$$

Where:

P_D = Power dissipation by the transistor (conduction losses).
V_{RMS} = RMS value of the minimum input voltage.
V_{CE} = Collector Emitter forward drop of the power transistor.

OFF-LINE START-UP AND BIAS SUPPLY GENERATION

A fast starting circuit is shown in figure 12. MOSFET Q2 quickly charges the IC's V_{CC} capacitor (C8) when the supply is initially turned on. This allows the supply to come on less than 1 second after AC power is applied. A simpler start-up circuit may be used which replaces the active circuit with a 39KΩ 2W resistor but starts more slowly (up to 15 seconds under low line conditions). Systems which do not require quick starting can reduce cost with the latter start-up method.

f_{SWITCH} (KHz)	r	$\sqrt{\sum_{k=1}^{r} \sin^2 \frac{k\pi}{r}}$
20	167	9.1
30	250	11.2
40	333	12.9
50	417	14.4
60	500	15.8
70	583	17.1
80	667	18.3
90	750	19.4
100	833	20.4
110	917	21.4
120	1000	22.4
130	1083	23.3
140	1167	24.2
150	1250	25.0
160	1333	25.7
170	1417	26.5
180	1500	27.3
190	1583	28.0
200	1667	28.9

Table 1. Figures for Calculating I_{RMS} (eq. 15)

POWER FACTOR ENHANCEMENT

Some combinations of line and load may exhibit distortion of the input current waveform. This distortion is usually caused by the inductor "ringing" with the C_{DS} of the power MOSFET, resulting in a non-zero inductor current at the beginning of the next cycle. This ringing can be dampened by using R2 and D7 in figure 12. Applications which can get by with slightly worse power factor can eliminate these components.

ADJUSTING THE OUTPUT VOLTAGE

The error amplifier creates an error voltage from the difference between the output voltage presented on pin 6 and the 5V internal reference. Since the output voltage is not ground referenced, the ML4813's internal op-amp is connected as an instrumentation amplifier (figure 13).

The output voltage is set by a combination of resistors which determine the relationship between (V_{OUT}+ – V_{OUT}–) and the output of the op-amp (pin 6). For the following discussion, R15' = R15 + R16 and R14' = R14 + R13. The differencing amplifier operation depends on the following relationships:

$$R15' = R14'$$
and
$$R12 = R25 + (R18 \parallel R17)$$

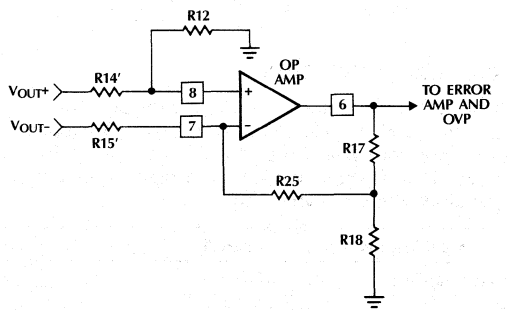


Figure 13. Ground Referencing the Output Voltage

Then:

$$V_{OUT} = \left(\frac{5V \times R18}{R17 + R18}\right)\left(\frac{R15'}{R15' + R25}\right)\left(\frac{R14'}{R12} + 1\right)$$

Since R25 is a low value compared to R15', the second term reduces to approximately 1. The third term is set at approximately 200. Therefore the above equation reduces to:

$$V_{OUT} \cong 1000 \times \left(\frac{R18}{R17 + R18}\right)$$

The over voltage comparator has a threshold that is set for 1.12 × V_{OUT} when pin 5 and pin 6 are connected directly. Figure 14 shows the connection for setting an OVP trip point higher than 1.12 × V_{OUT}, where:

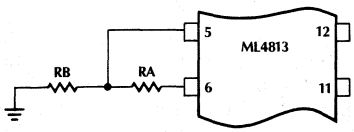


Figure 14. Setting OVP for a $V_{OVP} > 1.12 \times V_{OUT}$

$$V_{OVP} \cong 1.12 \times V_{OUT} \times \left(\frac{RA + RB}{RB} \right)$$

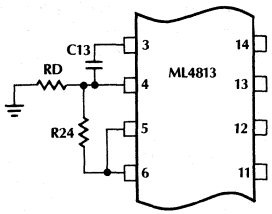


Figure 15. Setting OVP for a $V_{OVP} < 1.12 \times V_{OUT}$

Figure 15 shows OVP set for a voltage lower than 1.12 × V_{OUT} where:

$$V_{OVP} \cong 1.12 \times V_{OUT} \times \left(\frac{RD + R24}{RD} \right)$$

INDUCTOR INFORMATION

L3 is the flyback inductor and also provides the operating power for the control circuitry. A gapped ferrite pot core was chosen for this application for it's modest high frequency losses with high ripple current operation. Some possible choices are:

Manufacturer	Part #	Total Gap	N_P
Magnetics Inc.	F43019	.05"	32
Ferroxcube (Phillips)	3019 PL00-3F3	.05"	32
Ferroxcube (Phillips)	3019 PA125-3C8	.07"	38

The first 2 cores are sold ungapped and require the use of a .025" spacer to gap the center leg to yield a total gap length of .05". If an ungapped core is used, a "shorted turn" should be employed as shown below (figure 16) to prevent radiated EMI. The third core listed is sold with its center leg pre-gapped (.07" total), hence the outside of the core closes completely providing shielding without the shorted turn being required. N_S should be 3 turns. All windings #24AWG wire.

L1 and L2 inductors are constructed using a powdered iron. This is a suitable material for these inductors since the high frequency ripple currents (and resulting flux excursions) are much less severe than for L3. The core selected is:

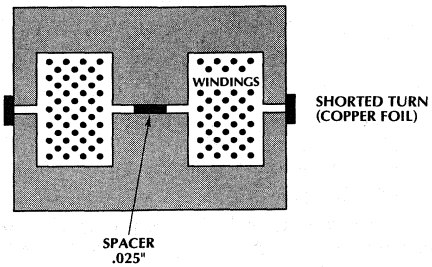


Figure 16. Construction of EMI Shield for Ungapped Cores

Manufacturer	Part #	Turns
MicroMetals	T68-26D	80T #24AWG

COMPONENT	DESCRIPTION
C1, C2	0.68μF, 630V
C3, C5, C6	.01μF, 1KV
C4	330μF, 250V
C7	1000pF, 50V
C8	1000μF, 16V
C9	1μF, 50V
C10	6800pF, 50V
C11, C14	0.1μF, 50V
C12	4.7μF, 50V
C13	0.22μF, 50V
D1 thru D4	1N5406
D5, D8	1N4148
D6, D7	MUR460
D9	22V Zener, 1/4 W
F1	3AG, 3A, 250V
Heat Sink	Thermalloy 6398-U-P3
L1, L2	500μH, 1.5A RMS
L3	160μH, 5A peak
Q1	MTH8N60
Q2	IRF821
Q3	2N2222
R1	220KΩ
R2, R19, R20	4.3KΩ
R3	10Ω
R4 thru R9	1Ω
R10	100Ω
R11	1.8KΩ
R12	4.02KΩ, 1%
R13 thru R16	402KΩ, 1%
R17	806Ω, 1%
R18	200Ω
R21	510KΩ
R22, R23	2KΩ
R24	100KΩ
R25	3.83KΩ, 1%
U1	ML4813CP
VR1	TNR12G431KM

Note: All resistor values 1/4 W ± 5% unless otherwise specified. All capacitor values ±10% unless otherwise specified.

Table 2. Component Values for Figure 8

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ML4813CP	0°C to +70°C	Molded DIP
ML4813CQ	0°C to +70°C	Molded PCC

Micro Linear

ML4815

Zero Voltage Switching Resonant Controller

GENERAL DESCRIPTION

The ML4815 is designed to facilitate zero-voltage switched (ZVS) resonant converters requiring constant off-time and variable on-time control. Since the power MOSFET is turned on at zero voltage in ZVS resonant converters, power dissipation due to charge-dumping of the MOSFET drain-source capacitance is eliminated, allowing high frequency operation and power density to be maximized. MOSFET parasitic drain-source capacitance can also be used as part of the resonant circuit, minimizing component count.

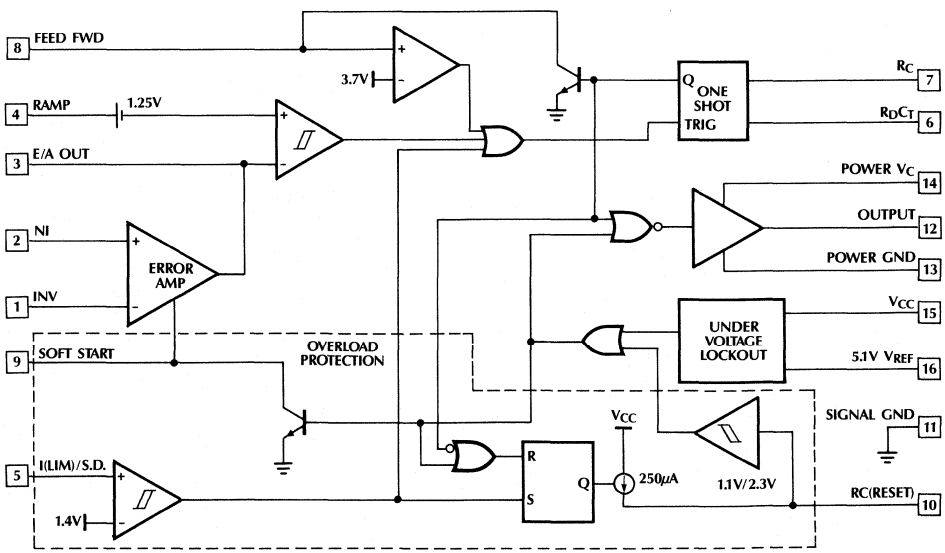
The ML4815 features a monostable multivibrator for precise off-time setting. The on-time is modulated through a ramp comparator in a manner similar to PWM converters. Either current-mode control with maximum on-time clamp or voltage-mode control with input feedforward can be selected.

ML4815 supports pulse-by-pulse (peak) current limiting as well as "hiccup" mode for fault protection. The controller is designed for operation up to 2MHz. ML4815 also includes a wide band error amplifier and a high peak current output driver which minimizes cross-conduction current.

FEATURES

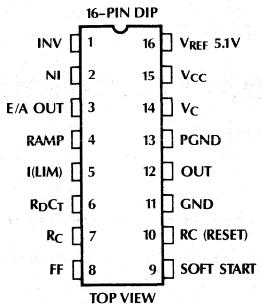
- Supports Single-Switch ZVS Resonant Topology with Minimal External Components
- Ideal for Simple, High Density DC to DC Converters
- Small Converter Frequency Variation from No-Load to Full-Load
- High Current (2A Peak) Totem-Pole Output Drive with Low Cross Conduction
- Precision Buffered 5.1V Reference (±2%)
- Wideband (5.5MHz), High Slew Rate (12V/μS) Error Amp.
- Under-Voltage Lockout with Low Current Start-Up
- Integrating Fault Detection/Soft-Start Reset

BLOCK DIAGRAM (Pin out shown is for 16-pin DIP)

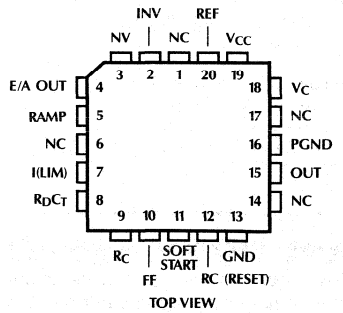


PIN CONNECTIONS

ML4815
16-Pin DIP



ML4815
20-Pin PCC



PIN DESCRIPTION

PIN #	NAME	FUNCTION
1	INV	Inverting input to error amp.
2	NI	Non-inverting input to error amp.
3	E/A OUT	Output of error amplifier and input to main comparator.
4	RAMP	Non-inverting input to main comparator. Connected to pin 8 for feedforward voltage-mode control or to pin 5 for current-mode control.
5	I(LIM)	Current limit sense pin. Normally connected to current sense resistor.
6	R_DC_T	Off-time setting capacitor and resistor.
7	R_C	Resistor to pin 6 to limit C_T charging rate.
8	FF	Capacitor to generate feedforward ramp.
9	SOFT START	Normally connected to Soft Start Capacitor and charging resistor.
10	RC (RESET)	Timing Capacitor for over-current integration and restart-delay.
11	GND	Analog Signal Ground.
12	OUT	High Current Totem pole output.
13	PGND	Return for the High Current Totem pole output.
14	V_C	Positive Supply for the High Current Totem pole output.
15	V_{CC}	Positive Supply for the IC.
16	5.1V REF	Buffered output for the 5.1V voltage reference.

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

Supply Voltage (Pins 14, 15) 30V
Output Current, Source or Sink (Pin 12)
DC 0.5A
Pulsed (0.5μs) 2A
Analog Inputs (Pins 1, 2, 4, 5, 8, 9, 10) ..... -0.3V to 6V
Error Amplifier Output Current (pin 3) ..... -5mA
Soft Start Sink Current (Pin 9) 100mA
Feedforward Sink Current (Pin 8) 80mA
C_T Charging Current (Pin 7) ..... -50mA

Junction Temperature
ML4815C ..... 125°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering 10 sec) ..... +260°C
Thermal Resistance (θ_{JA})
Plastic DIP ..... 65°C/W
Plastic Chip Carrier (PCC) ..... 60°C/W

OPERATING CONDITIONS

Temperature Range
ML4815C ..... 0°C to 70°C

ELECTRICAL CHARACTERISTICS

Unless otherwise noted, these specifications apply for C_T = 330pF, R_C = 100Ω, R_D = 2KΩ, V_{CC} = 15V, T_A = Operating Temperature Range. Pin numbers refer to 16-pin DIP.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Reference Section					
Output Voltage	T_J = 25°C, I_O = 1mA	5.00	5.10	5.20	V
Line Regulation	10V < V_{CC} < 30V		2	20	mV
Load Regulation	1mA < I_O < 10mA		5	20	mV
Temperature Stability	-55°C < T_J < 125°C, (note 1)		.2	.4	%
Total Variation	line, load, temp (note 1)	4.95		5.25	V
Output Noise Voltage	10Hz to 10KHz		50		μV
Long Term Stability	T_J = 125°C, 1000 hrs, (note 1)		5	25	mV
Short Circuit Current	V_{REF} = 0V	-15	-50	-100	mA
Error Amplifier Section					
Input Offset Voltage				15	mV
Input Bias Current			.6	3	μA
Input Offset Current			.1	1	μA
Open Loop Gain	1 < V_O < 4V	60	96		dB
CMRR	1.5 < V_{CM} < 5.5V	75	95		dB
PSRR	12 < V_{CC} < 25V	75	110		dB
Output Sink Current	$V_{PIN\ 3}$ = 1V	1	2.5		mA
Output Source Current	$V_{PIN\ 3}$ = 4V	-.5	-1.3		mA
Output High Voltage	$I_{PIN\ 3}$ = -0.5mA	4.0	4.7	5.0	V
Output Low Voltage	$I_{PIN\ 3}$ = 1mA	0	0.5	1.0	V
Unity Gain Bandwidth	(note 1)	3	5.5		MHz
Slew Rate	(note 1)	6	12		V/μs
RAMP Comparator Section					
Pin 4 Bias Current	$V_{PIN\ 7}$ = 0		-0.7		μA
Pin 3 Zero DC Threshold	$V_{PIN\ 2}$ = 2V, $V_{PIN\ 1}$ = $V_{PIN\ 3}$ $V_{PIN\ 5}$ = 0, $V_{PIN\ 6}$ = 1.5V $V_{PIN\ 8}$ = 2V		1.18		V
Delay to Output	C_L = 0, (note 1)		55		ns

ELECTRICAL CHARACTERISTICS (Continued)

Unless otherwise noted, these specifications apply for C_T = 330pF, R_C = 100Ω, R_D = 2KΩ, V_{CC} = 15V, T_A = Operating Temperature Range. Pin numbers refer to 16-pin DIP.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Current Limit Comparator					
Pin 5 Input Bias Current	$0 < V_{PIN\ 5} < 4V$		2		μA
Current Limit Threshold			1.41		V
Hysteresis			30		mV
Delay to Output	$V_{PIN\ 10}$ = 0, C_L = 0 (note 1)		50		ns
One-Shot Section					
Off-Time Initial Accuracy	C_L = 0, T_A = 25°C		0.45		μs
Off-Time Voltage Stability	C_L = 0, $12V < V_{CC} < 25V$		5		%
Off-Time Temperature Stability	C_L = 0 (note 1)		5		%
Off-Time Total Variation	C_L = 0, line, temp (note 1)		6		%
Feedforward/Maximum On-Time Clamp Section					
Discharge Current	$V_{PIN\ 8}$ = 2.5V		30		mA
On-Time Initial Accuracy	C_{FF} = 330pF, R_{FF} = 2.7KΩ to V_{REF}, C_L = 0		1.0		μs
Shutdown/Restart Section					
Pin 10 Charging Current			-250		μA
Overload Shutdown Threshold			2.3		V
Restart Threshold			1.1		V
Soft-Start Section					
Input Bias Current	$V_{PIN\ 9}$ = 4V		1		μA
Discharge Current	$V_{PIN\ 9}$ = 1V		25		mA
Under-Voltage Lockout Section					
Start Threshold			13.4		V
UVLO Hysteresis			3.6		V
Output Section					
Output Low Level	I_{OUT} = 20mA		0.25	0.40	V
	I_{OUT} = 200mA		1.2	2.2	V
Output High Level	I_{OUT} = -20mA		13.0		V
	I_{OUT} = -200mA		12.7		V
Rise/Fall Time	C_L = 1nF (note 1)		30		ns
Supply Current					
Start Up Current			1.3		mA
Operating I_{CC}	f = 1MHz, C_L = 0, T_A = 25°C		28		mA

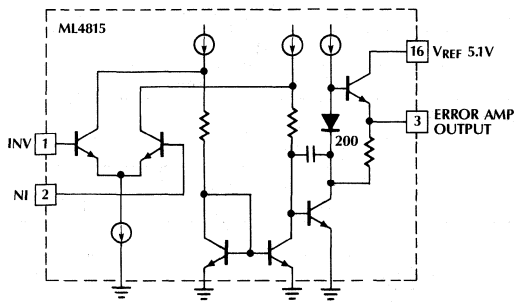
FUNCTIONAL DESCRIPTION

ML4815 PRINTED CIRCUIT BOARD LAYOUT CONSIDERATIONS

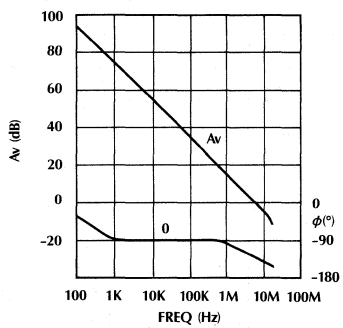
High speed circuits demand careful attention to layout and component placement. To assure proper performance of the ML4815, follow these rules: 1) Use a ground plane. 2) Damp or clamp parasitic inductive kick energy from the gate of driven MOSFET. Don't allow the output pins to ring below ground. A series gate resistor or a shunt 1 Amp Schottky diode at the output pin will serve this purpose. 3) Bypass V_{CC}, V_C, and V_{REF}. Use 1μF monolithic ceramic capacitors for V_{CC} and V_C with low equivalent series inductance. Allow less than 1 cm of total lead length for each capacitor between the bypassed pin and the ground plane. 4) Treat the off-time setting capacitor, C_T, like a bypass capacitor.

ERROR AMPLIFIER CIRCUIT

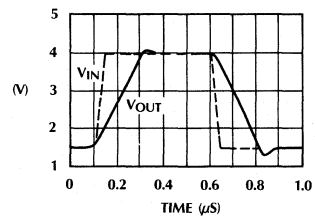
Simplified Schematic



Open-Loop Frequency Response



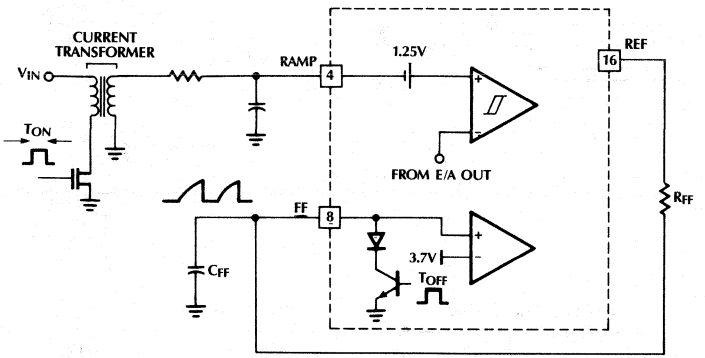
Unity Gain Slew Rate



CONTROL METHODS

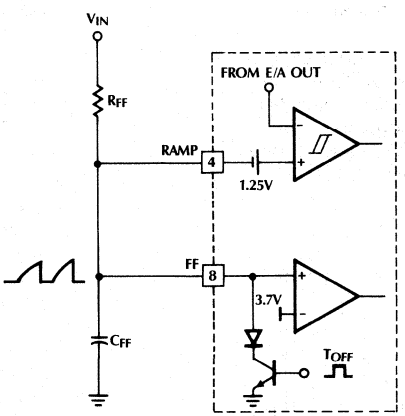
In current-mode control, the current transformer output is fed into the RAMP comparator input. The current-sense waveform is used as the on-time modulating ramp. The on-time can be clamped to a maximum by using R_{FF} and C_{FF} as shown.

Current-Mode Control with Maximum On-Time Clamp



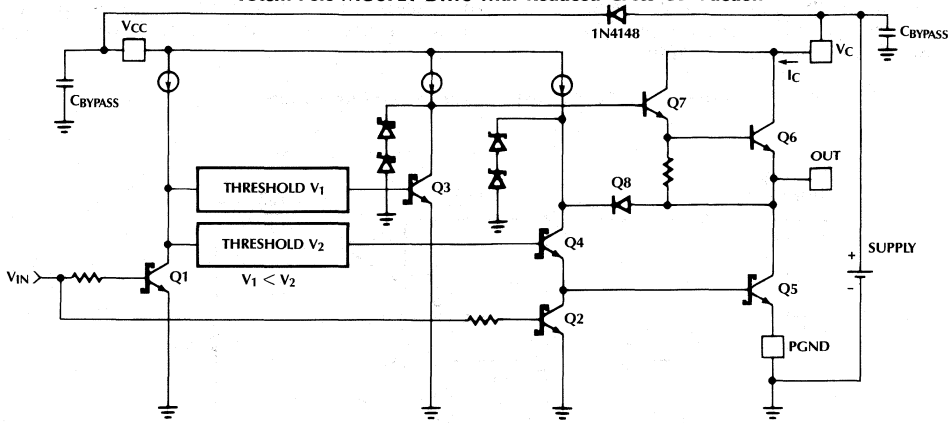
In feedforward voltage-mode control, the on-time modulating ramp is generated with an external capacitor C_{FF} from pin 8 to the ground. C_{FF} is charged through an external resistor R_{FF}. The maximum on-time is the time taken to charge C_{FF} to 3.7V. Since the charging current depends on V_{IN}, the resulting maximum on-time varies with V_{IN}.

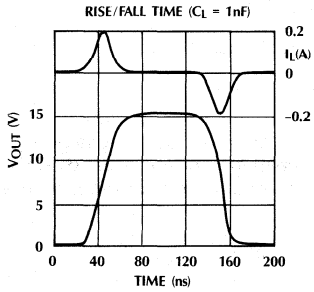
Feedforward Control

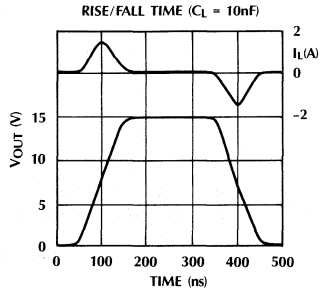


OUTPUT SECTION

Totem-Pole MOSFET Drive with Reduced Cross-Conduction

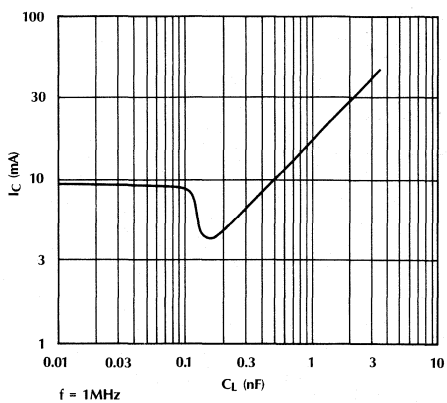






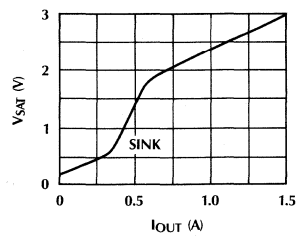
- When driving power MOSFET's with high equivalent gate capacitance ($C_G > 3nF$), it is advisable to use an external 1N4148 diode between V_{CC} and V_C pins (figure above) to reduce extra power dissipation caused by slow turn-off of Q_7. In this case both V_{CC} and V_C pins should have bypass capacitors (C = 1μF) as close as possible to the IC pins.

I_C vs C_L

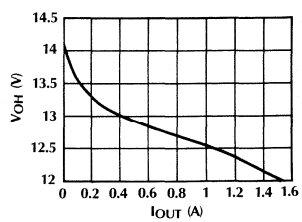


f = 1MHz
T_J = 150°C
I_C = TOTEM-POLE DRIVER CURRENT

V_{OL} Curve



V_{OH} Curve

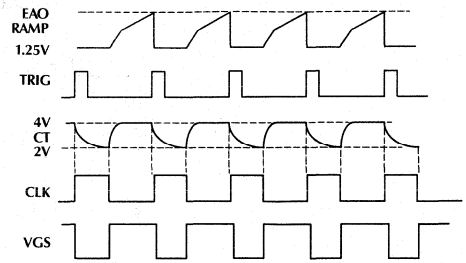


ONE-SHOT

The figure below shows the detailed block diagram of the one-shot. The one-shot is programmed with external resistors R_C, R_D and capacitor C_T. Assuming that CLK is low and Q_2 conducts initially, the timing capacitor C_T is charged to 4V through R_C and Q_3. This corresponds to the switch conduction cycle (on-time). When either the feedforward ramp or the sensed current signal exceeds the error amplifier output voltage, a trigger pulse is sent to the one-shot, setting the R-S latch X_2 and disabling Q_3. C_T is immediately discharged through R_D until C_T voltage reaches the lower threshold (2V) of the Schmitt-trigger X_1. At this point, X_1 output goes high, resetting X_2. Q_1 turns off, allowing Q_3 to recharge C_T to 4V. This time interval corresponds to the switch off-time. Since the off-time is simply the discharge time of C_T, one can express

$$T_{OFF} = 0.69\ R_D C_T$$

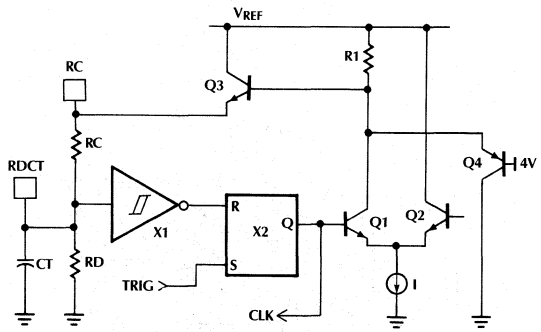
Timing Diagram of the One-Shot



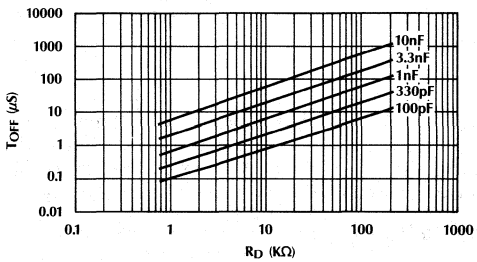
The purpose of R_C is to slow the charging transient of C_T in order to widen the internal reset pulse. R_C is usually chosen such that the following inequality is satisfied.

$$\frac{R_C}{R_C + R_D} < 0.05$$

Block Diagram of the One-Shot



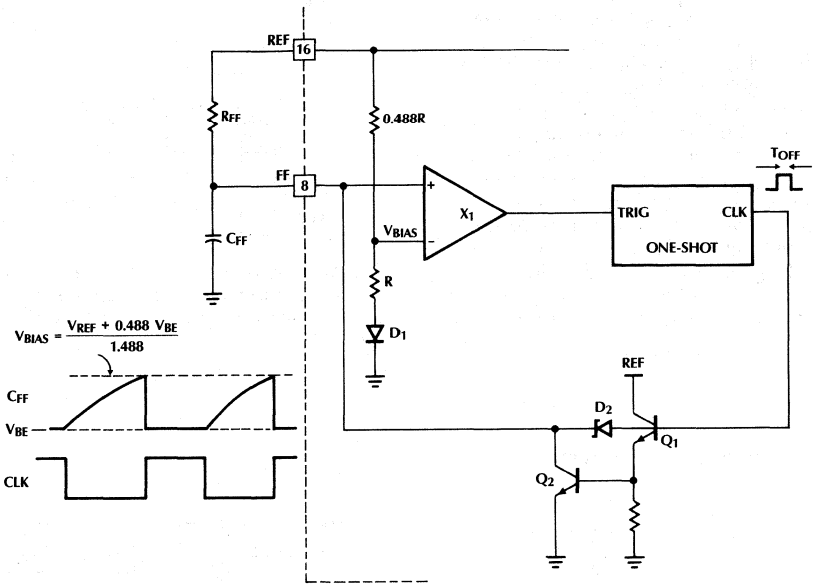
T_{OFF} vs R_D



6

CONSTANT ON-TIME CLAMP (In Current-Mode Only)

Constant On-Time Clamp

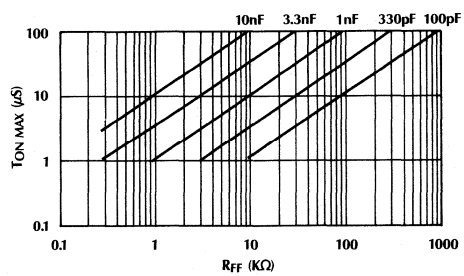


In current-mode control, the maximum on-time can be clamped by using the comparator X_1 (figure above). The internal transistors Q_1, Q_2 and diode D_2 discharges C_{FF} to approximately V_{BE}. The time taken to charge C_{FF} from V_{BE} to V_{BIAS} $\left(= \frac{V_{REF} + 0.488\ V_{BE}}{1.488} \right)$ sets the maximum on-time. The diode D_1 compensates the V_{BE} dependent C_{FF} valley voltage. It can be shown that

$$T_{ON(MAX)} \approx 1.115\ R_{FF}\ C_{FF}$$

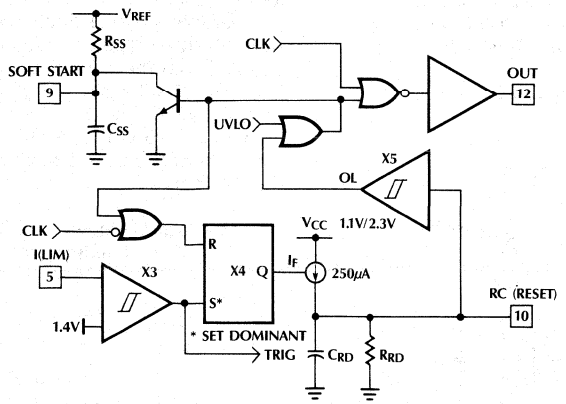
and $T_{ON(MAX)}$ is relatively independent of temperature.

T_{ON} vs R_{FF}



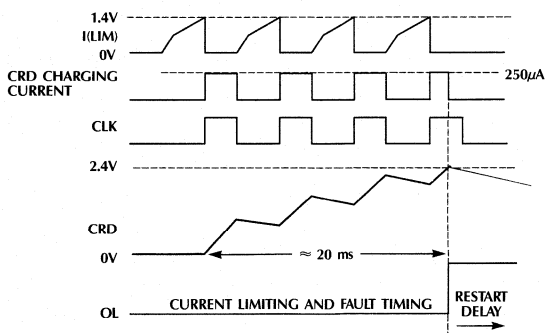
CURRENT-LIMITING, OVERLOAD SHUTDOWN AND FAULT MANAGEMENT

Overload Protection and Fault Management



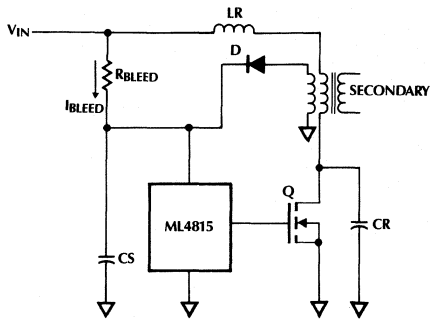
ML4815 features a unique overload protection scheme. The power transistor current is compared with the current-limit threshold (1.4V) of X_3. When the sensed current exceeds this threshold, the one-shot is triggered and the R-S latch X_4 is set. The one-shot blanks the gate drive and X_4 turns on the current source I_F. The external capacitor C_{RD}, which is normally fully discharged, is charged towards an overload threshold of 2.3V. The packet of charge delivered to C_{RD} in each over-current cycle is $I_F \times T_{OFF}$ (figure below). X_4 is reset after the off-time elapses. If output short is removed before C_{RD} reaches the overload threshold, C_{RD} will be discharged through R_{RD} and normal operation will resume. Under persistent output short circuit, C_{RD} is charged until it reaches 2.3V. The gate drive is immediately terminated and the soft-start capacitor is discharged. C_{RD} then discharges through R_{RD} towards the restart threshold (1.1V). Gate drive remains off until C_{RD} is discharged below 1.1V. The time taken for C_{RD} to discharge to the restart threshold is the restart-delay time. This delay reduces the average power delivered to the load during overload, thus protecting both the load and the controller. If overload persists, the controller will continue to hiccup until the cause of overload is removed. The controller undergoes soft-start at each restart. The overload shutdown and restart sequence for a converter with non-bootstrapped power supply V_{CC} is illustrated in figure.

Current Limiting Overload Shutdown and Restart Sequence (Non-Bootstrapped Operation)



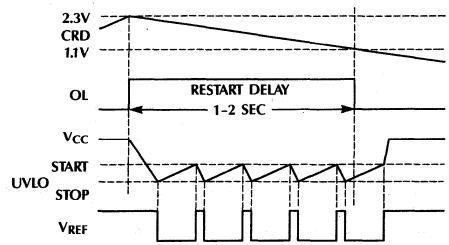
For a bootstrapped converter (where controller V_{CC} is obtained from an auxiliary winding of the main transformer), overload shutdown causes both the converter output and the controller V_{CC} to collapse. Undervoltage lockout (UVLO) is activated and the on-chip bandgap reference is disabled. ML4815 dissipates only 2mA of supply current during shutdown. Since

Simplified V_{CC} Bootstrapping Scheme

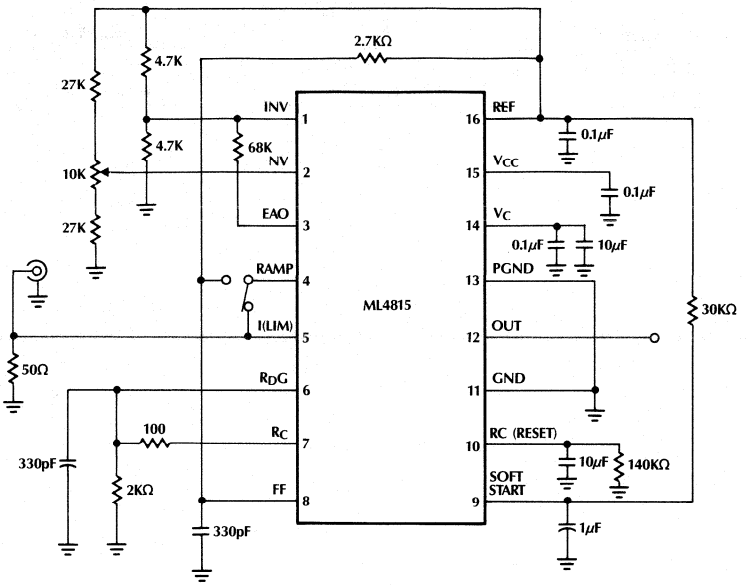


I_{BLEED} is higher than the start-up current, C_S will be charged towards the UVLO start threshold. When this happens, the entire controller becomes operational except that the gate drive remains off. I_{CC} jumps to its full operational value. Since V_{CC} bootstrapping is not yet available, I_{CC} will discharge C_S below the UVLO stop threshold. The on-chip reference will again be disabled with the controller supply current reduced to 2mA. I_{BLEED} will again charge C_S towards the UVLO start threshold. The process repeats until C_{RD} is discharged below the restart threshold. The shutdown and restart sequence is illustrated with the timing diagram below.

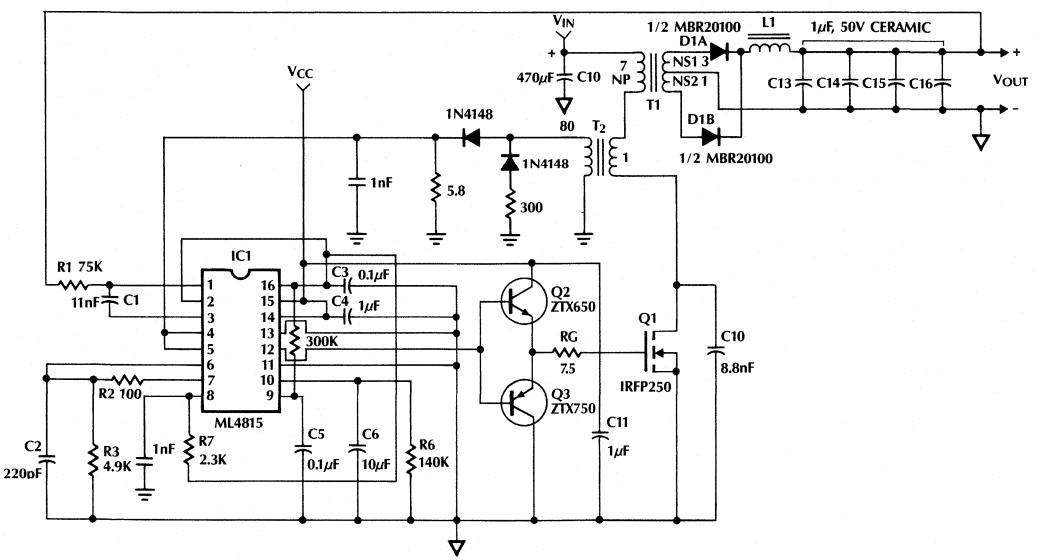
Overload Shutdown UVLO and Restart Sequence (Bootstrapped Operation)



OPEN LOOP LABORATORY TEST FIXTURE



SCHEMATIC OF THE 50W ZVS DC/DC CONVERTER



ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ML4815CP	0°C to +70°C	Molded DIP
ML4815CQ	0°C to +70°C	Molded PCC

Micro Linear

ML4816

High Frequency Multi-Mode Resonant Controller

GENERAL DESCRIPTION

The ML4816 controller IC is suitable for a wide range of resonant converter topologies. This controller can be used with Zero Current Switched (ZCS) Quasi Resonant Converters (QRC) requiring constant on-time and modulated off-time, as well as frequency modulated converters such as Series Resonant Converters operating above resonance.

The ML4816's oscillator features independent control of charging and discharging currents (on-time and off-time). Output frequency can be obtained either proportional or inversely proportional to the controlling voltage. In addition, both upper and lower frequency limits (f_{MIN} and f_{MAX}) can be independently set.

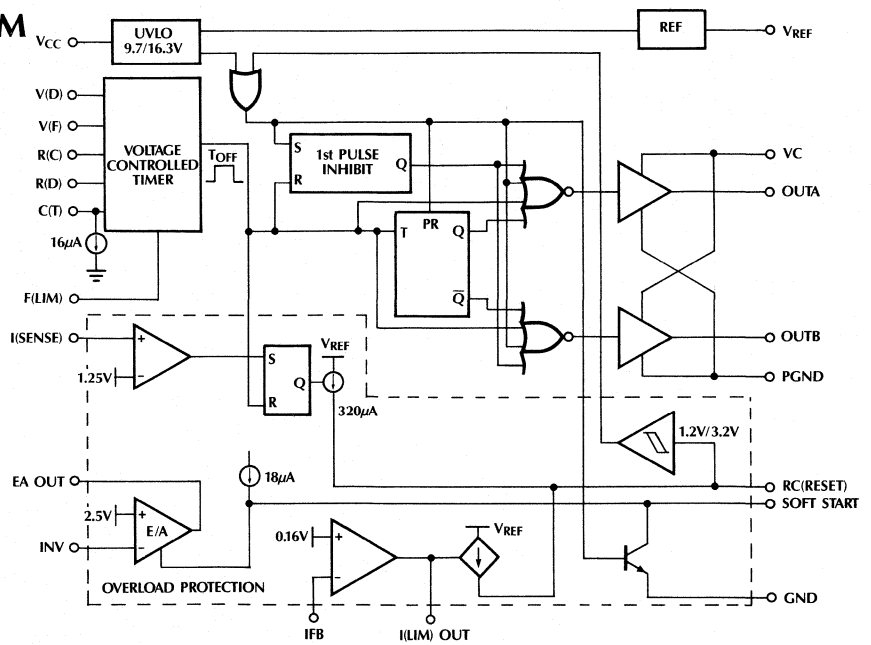
Both pulse-by-pulse and DC current limiting are provided for. Overload protection (shutdown) is triggered after a programmable delay time. Restart after overload shutdown can be delayed by a programmable time. Internal logic disables the restart delay on initial turn-on.

The ML4816 includes under-voltage lockout with 6V hysteresis and high current high speed totem pole output drivers for high speed drive of external MOSFETs.

FEATURES

- Supports Zero Current Switched (ZCS) Quasi-Resonant Converters
- Supports Series Resonant (ZVS) converters operating above resonance
- Wide oscillator frequency range
- Programmable f_{MIN} and f_{MAX} limits
- Practical Operation to 2.5 MHz (f_{OSC})
- Low Start-up Current and Under-Voltage Lockout Circuits support Off-Line Operation
- Pulse by Pulse or DC Current Limiting
- Integrating Soft Start Reset (Fault Integration) with Programmable Restart Delay
- High current (2A peak) totem-pole output drive
- Precision buffered 5V Reference (±1%)

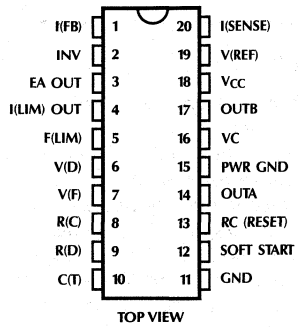
BLOCK DIAGRAM



6

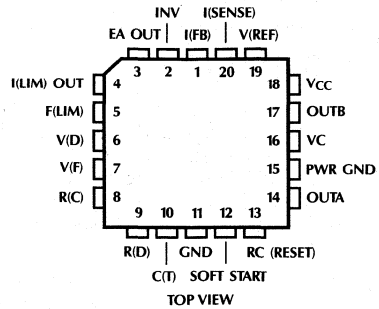
PIN CONFIGURATION

ML4816
20-Pin DIP



TOP VIEW

ML4816
20-Pin PCC



TOP VIEW

Micro Linear

ML4817

High Frequency Single-Ended PWM Controller

GENERAL DESCRIPTION

The ML4817 High Frequency PWM Controller is optimized for use in single-ended Switch Mode Power Supply designs running at frequencies up to 1MHz. Propagation delays are minimal through the comparators and logic for reliable high frequency operation while slew rate and bandwidth are maximized in the error amplifier. This controller is designed to work in either voltage or current mode.

A unique overload protection circuit helps to limit stress on the output devices. This integrating method of fault detection also provides for reset delay before restart. A 1.4V threshold current limit comparator provides cycle-by-cycle current limit.

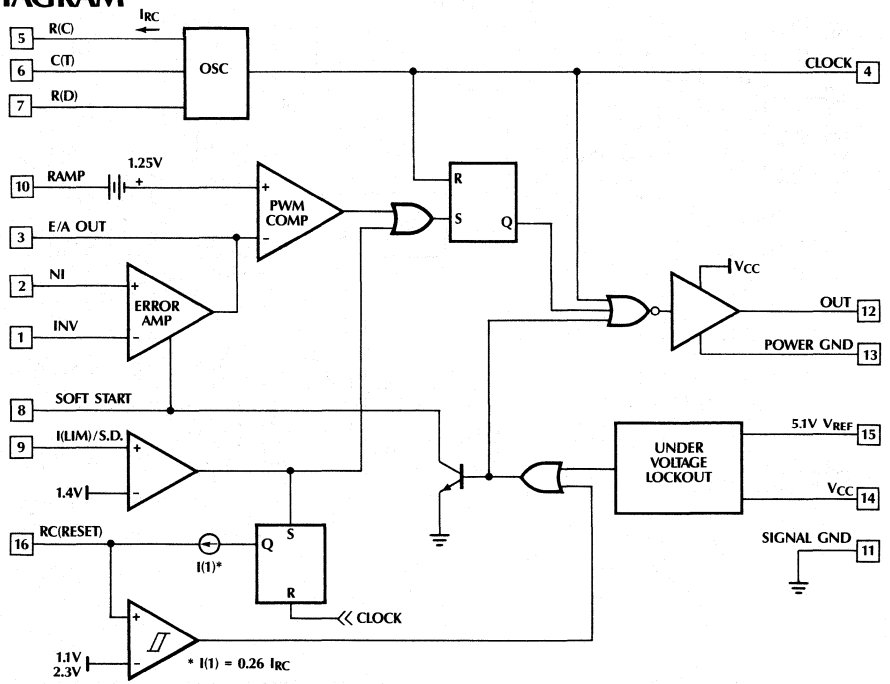
The ML4817 oscillator features accurately programmable dead time control to precisely limit the maximum duty cycle.

The ML4817 is fabricated on a 40V bipolar process from the FB3480 Power Supply Controller Array. Customized versions of this controller are therefore easily implemented. Please refer to the FB3480 datasheet for more information.

FEATURES

- Practical Operation at Switching Frequencies to 1MHz
- High Current (2A peak) Totem Pole Output
- Temperature Stable precise oscillator frequency and dead time
- Precision maximum duty cycle limit
- Integrating fault detection with reset delay
- Fast Shut Down Path from Current Limit to Output
- Output pulls low for Under-Voltage Lockout
- Under-Voltage Lockout circuit with 3.6V hysteresis

BLOCK DIAGRAM



6

Micro Linear

ML4818

Phase Modulation/Soft Switching Controller

GENERAL DESCRIPTION

The ML4818 is a complete phase modulation control IC suitable for full bridge soft switching converters. Unlike conventional PWM circuits, the phase modulation technique allows for zero voltage switching transitions and square wave drive across the transformer. The IC modulates the phases of the two sides of the bridge to control output power.

The ML4818 can be operated in either current or voltage mode. The delay times for the outputs are externally programmable to allow the zero voltage switching transitions to take place.

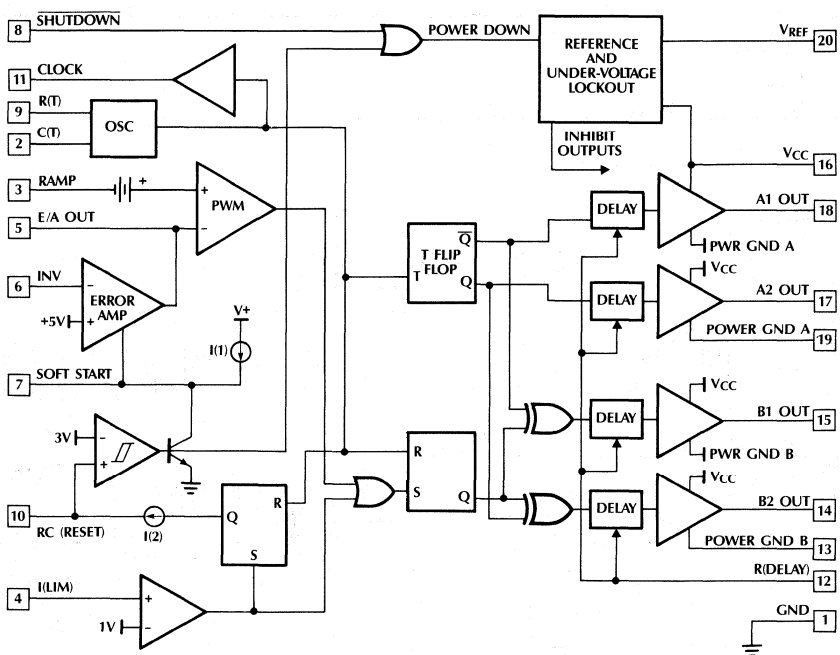
Both pulse-by-pulse current limit and integrating fault detection and soft start reset are provided. The under-voltage lockout circuit features a 6V hysteresis with a low starting current to allow off-line start up with a bleed resistor. A shutdown function powers down the IC, putting it into a low quiescent state.

The circuit can be operated at frequencies above 1MHz. The ML4818 contains four high current totem pole outputs which feature high slew rate with low cross conduction.

FEATURES

- Controls Full Bridge Phase Modulation Zero Voltage Switching Circuit
- Four 2A Peak Current Totem Pole Output Drivers
- Operation to 1.5MHz
- Voltage Mode or Current Mode Operation
- Cycle-by-Cycle Current Limiting with Integrating Fault Detection
- Precision Buffered 5V Reference (±1%)
- Under-Voltage Lockout Circuit with 6V Hysteresis
- Programmable Clock Width and Output Blanking Delay

BLOCK DIAGRAM



Micro Linear

ML4819

Power Factor and PWM Controller "Combo"

GENERAL DESCRIPTION

The ML4819 is a complete boost mode Power Factor Control (PFC) which also contains a PWM controller. The PFC circuit is similar to the ML4812 while the PWM controller can be used for current or voltage mode control for a second stage converter. Since the PWM and PFC circuits share the same oscillator, synchronization of the two stages is inherent. The outputs of the controller IC provide high current (>1A peak) and high slew rate to quickly charge and discharge MOSFET gates. Special care has been taken in the design of the ML4819 to increase system noise immunity.

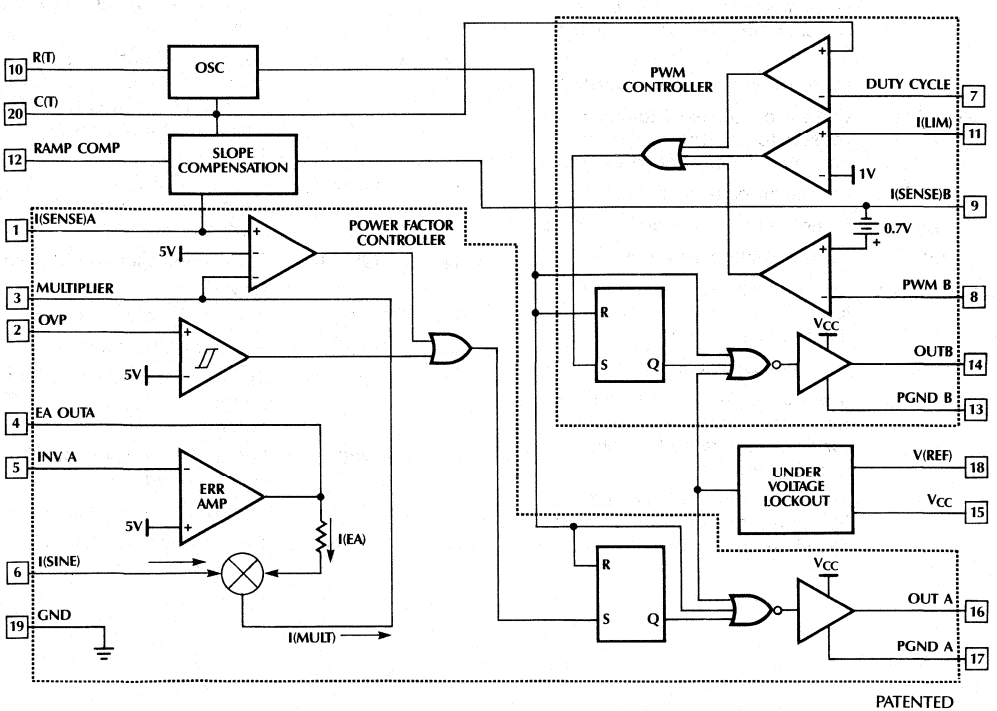
The PFC section is a peak current sensing control which uses a current sense transformer or SENSE FET to non-dissipatively sense switch current, giving the system improved overall efficiency over the average current sensing control method.

The PWM section includes cycle by cycle current limiting, precise duty cycle limiting for single ended converters, and slope compensation.

FEATURES

- Two 1A Peak Current Totem-Pole Output Drivers
- Precision buffered 5V Reference (±1%)
- Large oscillator amplitude for better noise immunity
- Precision duty cycle limit for PWM section
- Current input multiplier reduces external components and improves noise immunity
- Programmable Ramp Compensation circuit
- Over-Voltage comparator eliminates output "runaway" due to load removal
- Wide common mode range in current sense comparators for better noise immunity
- Under-Voltage Lockout circuit with 6V hysteresis

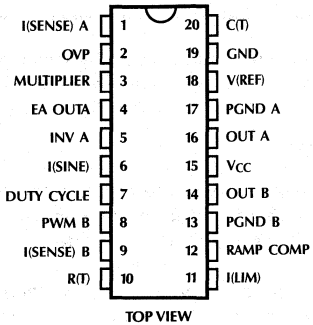
BLOCK DIAGRAM (Pin out shown is for DIP)



PATENTED

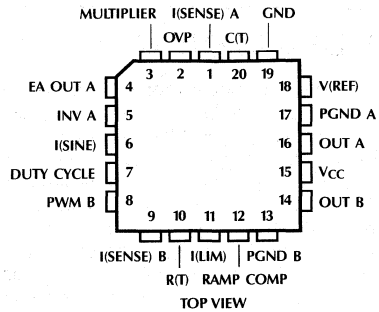
PIN CONFIGURATIONS

ML4819
20-Pin DIP



TOP VIEW

ML4819
20-Pin PCC



TOP VIEW

PIN DESCRIPTION

PIN #	NAME	FUNCTION
1	I(SENSE) A	Input from the PFC Current Sense Transformer to the PWM comparator (+). Current Limit occurs when this point reaches 5V.
2	OVP	Input to over voltage comparator.
3	MULTIPLIER	Output of Current Multiplier. A resistor to ground on this pin converts the current to a voltage.
4	EA OUT A	Output of error amplifier.
5	INV A	Inverting input to error amplifier.
6	I(SINE)	Current Multiplier input.
7	DUTY CYCLE	PWM controller duty cycle is limited by setting this pin to a fixed voltage.
8	PWM B	Error voltage feedback input.
9	I(SENSE) B	Input for Current Sense resistor for current mode operation or for Oscillator ramp for voltage mode operation.
10	R(T)	Oscillator timing resistor pin. A 5V source across this resistor sets the charging current for C(T).
11	I(LIM)	Cycle by cycle PWM current limit. Exceeding 1V threshold on this pin terminates the PWM cycle.
12	RAMP COMP	Buffered output from the Oscillator Ramp (C(T)). A resistor to ground sets a current 1/2 of which is sourced on pins 9 and 11.
13	GND B	Return for the high current totem pole output of the PWM controller.
14	OUT B	PWM controller totem pole output.
15	V_{CC}	Positive Supply for the IC.
16	OUT A	PFC controller totem pole output.
17	GND A	Return for the high current totem pole output of the PFC controller.
18	V(REF)	Buffered output for the 5V voltage reference.
19	GND	Analog signal ground.
20	C(T)	Timing Capacitor for the Oscillator.

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

Supply Voltage (V_{CC}) 35V
Output Current, Source or Sink (Pin 12)
DC 1.0A
Output Energy (capacitive load per cycle) 5μJ
Multiplier I(SINE) Input (Pin 6) 1.2mA
Error Amp Sink Current (Pin 3) 10mA
Oscillator Charge Current 2mA
Analog Inputs (Pins 1, 4, 5) ..... –0.3V to 5.5V
Junction Temperature ..... 150°C
Storage Temperature Range ..... –65°C to +150°C
Lead Temperature (Soldering 10 sec) ..... +260°C
Thermal Resistance (θ_{JA})
Plastic Chip Carrier (PCC)-Q ..... 60°C/W
Plastic DIP-P ..... 65°C/W

OPERATING CONDITIONS

Temperature Range
ML4819C ..... 0°C to +70°C

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, R_T = 14KΩ, C_T = 1000pF, T_A = Operating Temperature Range, V_{CC} = 15V (note 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Oscillator					
Initial Accuracy	T_J = 25°C	90	97	104	KHz
Voltage Stability	12V < V_{CC} < 25V		0.2		%
Temperature Stability			2		%
Total Variation	line, temp	88		106	KHz
Ramp Valley			0.9		V
Ramp Peak			4.3		V
R(T) Voltage		4.8	5.0	5.2	V
Discharge Current (pin 8 open)	T_J = 25°C, $V_{PIN\ 16}$ = 2V	7.5	8.4	9.3	mA
	$V_{PIN\ 16}$ = 2V	7.2	8.4	9.5	mA
Duty Cycle Limit Comparator					
Input Offset Voltage		–15		15	mV
Input Bias Current			–2	–10	μA
Duty Cycle	$V_{PIN\ 7}$ = $V_{REF/2}$	43	45	47	%
Reference Section					
Output Voltage	T_J = 25°C, I_O = 1mA	4.95	5.00	5.05	V
Line Regulation	12V < V_{CC} < 25V		2	20	mV
Load Regulation	1mA < I_O < 20mA		8	25	mV
Temperature Stability			.4		%
Total Variation	line, load, temp	4.9		5.1	V
Output Noise Voltage	10Hz to 10KHz		50		μV
Long Term Stability	T_J = 125°C, 1000 hrs, (note 1)		5	25	mV
Short Circuit Current	V_{REF} = 0V	–30	–85	–180	mA
Error Amplifier Section					
Input Offset Voltage		–15		15	mV
Input Bias Current			–0.1	–1.0	μA
Open Loop Gain	1 < $V_{PIN\ 4}$ < 5V	60	75		dB
PSRR	12V < V_{CC} < 25V	60	90		dB
Output Sink Current	$V_{PIN\ 4}$ = 1.1V, $V_{PIN\ 5}$ = 5.2V	2	12		mA

ELECTRICAL CHARACTERISTICS (Continued)

Unless otherwise specified, R_T = 14KΩ, C_T = 1000pF, T_A = Operating Temperature Range, V_{CC} = 15V (note 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Error Amplifier Section (Continued)					
Output Source Current	$V_{PIN\ 4}$ = 5.0V, $V_{PIN\ 5}$ = 4.8V	-0.5	-1.0		mA
Output High Voltage	$I_{PIN\ 4}$ = -0.5mA, $V_{PIN\ 5}$ = 4.8V	6.5	7.0		V
Output Low Voltage	$I_{PIN\ 4}$ = 2mA, $V_{PIN\ 5}$ = 5.2V		0.7	1.0	V
Unity Gain Bandwidth			1.0		MHz
Multiplier					
I(SINE) Input Voltage	I(SINE) = 500μA	.4	.7	.9	V
Output Current (pin 2)	I(SINE) = 500μA, Pin 5 = V_{REF} - 20mV	480	495	505	μA
	I(SINE) = 500μA, Pin 5 = V_{REF} + 20mV		0	1	μA
	I(SINE) = 1mA, Pin 5 = V_{REF} - 20mV	960	990	1005	μA
Bandwidth			200		KHz
PSRR	12V < V_{CC} < 25V		70		dB
Slope Compensation Circuit					
RAMP COMP Voltage (pin 12)			$V_{PIN\ 20}$ - 1		V
I_{OUT} (pin 1 or pin 9)	$I_{PIN\ 12}$ = 100μA (note 3)	45	48	51	μA
OVP Comparator					
Input Offset Voltage	Output Off	-15		15	mV
Hysteresis	Output On	100	120	140	mV
Input Bias Current			-0.3	-3	μA
Propagation Delay			150		ns
I(SENSE) Comparators A and B					
Input Common Mode Range		-0.2		5.5	V
Input Offset Voltage	I(SENSE) A	-15		15	mV
	I(SENSE) B	+0.4	0.7	+0.9	V
Input Bias Current			-3	-10	μA
Input Offset Current		-1		1	μA
Propagation Delay			150		ns
I_{LIMIT} (A) Trip Point	$V_{PIN\ 3}$ = 5.5V	4.8	5	5.2	V
I(LIM) Comparator					
I_{LIMIT} Trip Point		.95	1.0	1.05	V
Input Bias Current			-2	-10	μA
Propagation Delay			150		ns
Output Section (A and B)					
Output Voltage Low	I_{OUT} = -20mA		0.1	0.4	V
	I_{OUT} = -200mA		1.6	2.2	V
Output Voltage High	I_{OUT} = 20mA	13	13.5		V
	I_{OUT} = 200mA	12	13.4		V
Output Voltage Low in UVLO	I_{OUT} = -1mA, V_{CC} = 8V		0.1	0.8	V
Output Rise/Fall Time	C_L = 1000pF		50		ns

ELECTRICAL CHARACTERISTICS (Continued)

Unless otherwise specified, R_T = 14KΩ, C_T = 1000pF, T_A = Operating Temperature Range, V_{CC} = 15V (note 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Under Voltage Lockout					
Start-Up Threshold		15	16	17	V
Shut-Down Threshold		9	10	11	V
V_{REF} Good Threshold			4.4		V
Total Device					
Supply Current	Start-Up, V_{CC} = 14V		.6	1.2	mA
	Operating, T_J = 25°C		25	35	mA

Note 1: This parameter not 100% tested in production but guaranteed by design.
Note 2: V_{CC} is raised above the Start-up Threshold first to activate the IC, then returned to 15V.
Note 3: PWM comparator bias currents are subtracted from this reading.

FUNCTIONAL DESCRIPTION

OSCILLATOR

The ML4819 oscillator charges the external capacitor (C_T) with a current (I_{SET}) equal to $5/R_{SET}$. When the capacitor voltage reaches the upper threshold, the comparator changes state and the capacitor discharges to the lower threshold through Q1. While the capacitor is discharging, Q2 provides a high pulse.

The Oscillator period can be described by the following relationship:

$$T_{OSC} = T_{RAMP} + T_{DEADTIME}$$

where:

$$T_{RAMP} = \frac{C\ (\text{Ramp Valley to Peak})}{I_{SET}}$$

and:

$$T_{DEADTIME} = \frac{C\ (\text{Ramp Valley to Peak})}{(8.4\text{mA} - I_{SET})}$$

The maximum duty cycle of the PWM section can be limited by setting a threshold on pin 7. When the C(T) ramp is above the threshold at pin 7, the PWM output is held off and the PWM flip-flop is set:

$$D_{LIMIT} \cong \frac{D_{OSC} \times (V_{PIN\ 7} - 0.9)}{3.4}$$

Where:

D_{LIMIT} = Desired duty cycle limit
D_{OSC} = Oscillator duty cycle

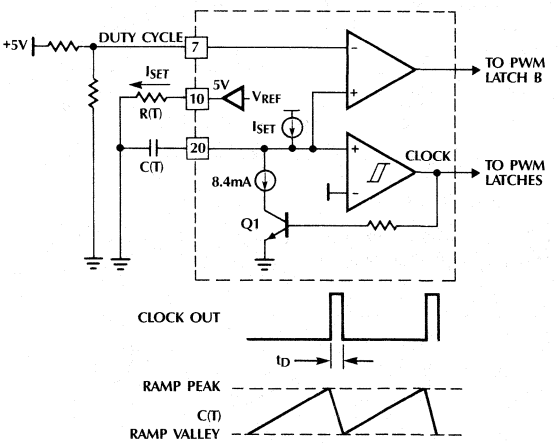


Figure 1. Oscillator Block Diagram

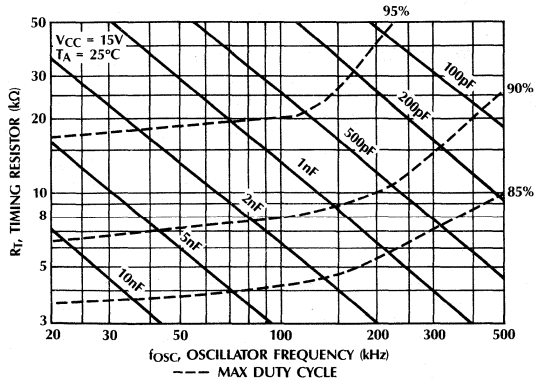


Figure 2. Oscillator Timing Resistance vs. Frequency

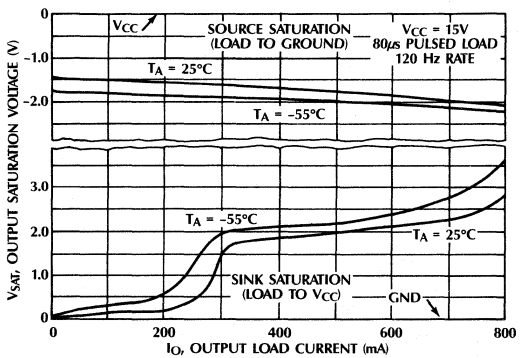


Figure 3. Output Saturation Voltage vs. Output Current

ERROR AMPLIFIER

The ML4819 error amplifier is a high open loop gain, wide bandwidth, amplifier.

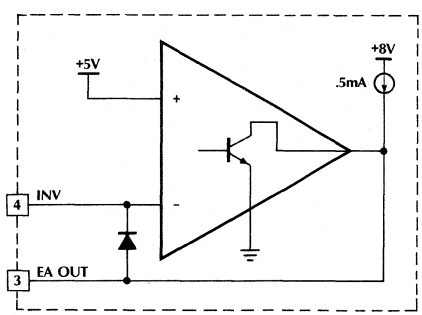


Figure 4. Error Amplifier Configuration

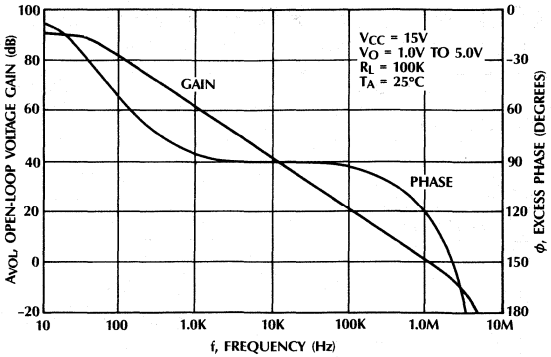


Figure 5. Error Amplifier Open-Loop Gain and Phase vs. Frequency

MULTIPLIER

The ML4819 multiplier is a linear current input multiplier to provide high immunity to the disturbances caused by high power switching. The rectified line input sine wave is converted to a current via a dropping resistor. In this way, small amounts of ground noise produce an insignificant effect on the reference to the PWM comparator.

The output of the multiplier is a current proportional to:

$$I_{OUT} \propto I(SINE) \times I(EA)$$

where I(SINE) is the current in the dropping resistor, and I(EA) is a factor which varies from 0 to 1 proportional to the output of the error amplifier. When the error amplifier is saturated high, the output of the multiplier is approximately equal to the I(SINE) input current.

The multiplier output current is converted into the reference voltage for the PWM comparator through a resistor to ground on the multiplier output (pin 3).

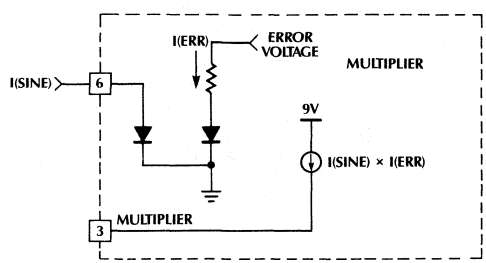


Figure 6. Multiplier Block Diagram

SLOPE COMPENSATION

Slope compensation is accomplished by adding 1/2 of the current flowing out of pin 12 to pin 1 (for the PFC section) and pin 9 (for the PWM section). The amount of slope compensation is equal to $(I_{PIN\ 12}/2) \times R_L$ where R_L is the impedance to GND on pin 1 or pin 9. Since most of the PWM applications will be limited to 50% duty cycle, slope compensation should not be needed for the PWM section. This can be defeated by using a low impedance load to the current sense on pin 9.

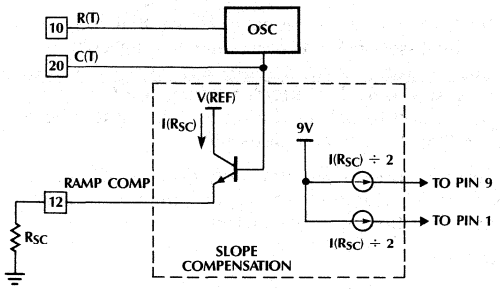


Figure 7. Slope Compensation Circuit

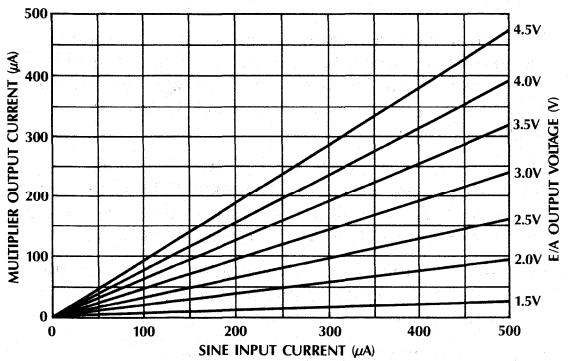


Figure 8. Multiplier Linearity

UNDER VOLTAGE LOCKOUT

On power-up the ML4819 remains in the UVLO condition; output low and quiescent current low. The IC becomes operational when V_{CC} reaches 16V. When V_{CC} drops below 10V, the UVLO condition is imposed. During the UVLO condition, the 5V V_{REF} pin is "off", making it usable as a "flag".

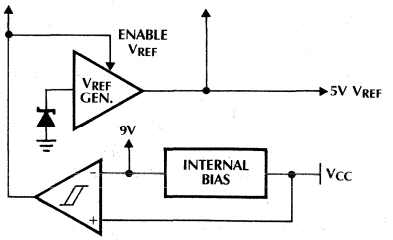


Figure 9. Under-Voltage Lockout Block Diagram

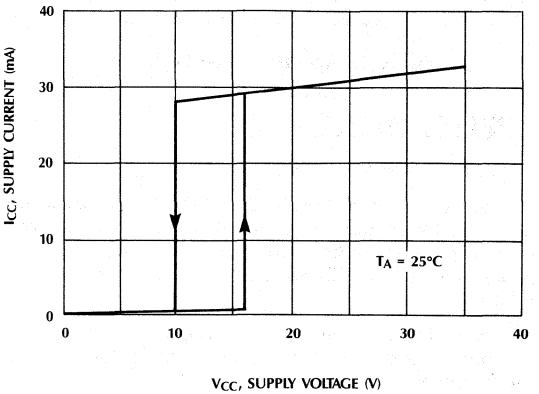


Figure 10a. Total Supply Current vs. Supply Voltage

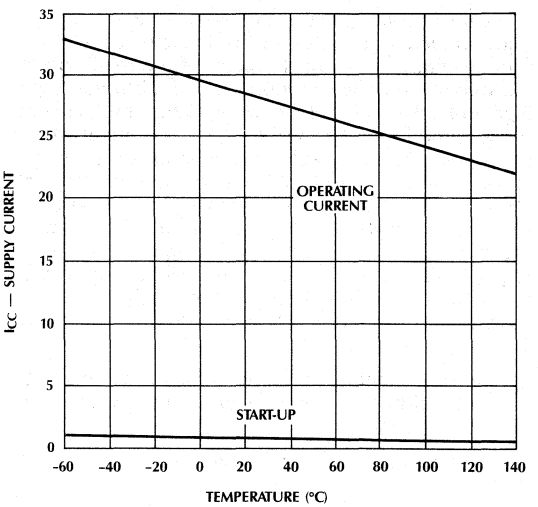


Figure 10b. Total Supply Current (I_{CC}) vs. Temperature

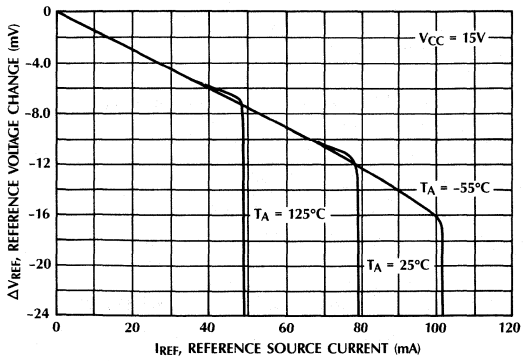


Figure 11. Reference Load Regulation

APPLICATIONS

POWER FACTOR SECTION

The power factor section in the ML4819 is similar to the power factor section in the ML4812 with the exception of the operation of the slope compensation circuit. Please refer to the ML4812 data sheet for more information.

The following calculations refer to figure 12. The component designators in the equations below refer to the following components in figure 12:

R_T = R16, C_T = C6.

INPUT INDUCTOR (L1) SELECTION

The central component in the regulator is the input boost inductor. The value of this inductor controls various critical operational aspects of the regulator. If the value is too low, the input current distortion will be high and will result in low power factor and increased noise at the input. This will require more input filtering. In addition, when the value of the inductor is low the inductor dries out (runs out of current) at low currents. Thus the power factor will decrease at lower power levels and/or higher line voltages. If the inductor value is too high, then for a given operating current the required size of the inductor core will be large and/or the required number of turns will be high. So a balance must be reached between distortion and core size.

One more condition where the inductor can dry out is analyzed below where it is shown to be maximum duty cycle dependent.

For the boost converter at steady state:

$$V_{OUT} = \frac{V_{IN}}{1 - D_{ON}} \quad (1)$$

Where D_{ON} is the duty cycle $[T_{ON}/(T_{ON} + T_{OFF})]$. The input boost inductor will dry out when the following condition is satisfied:

$$V_{IN}(t) < V_{OUT} \times (1 - D_{ON}) \quad (2)$$

or

$$V_{INDRY} = [1 - D_{ON}\ (max)] \times V_{OUT} \quad (3)$$

V_{INDRY}: Voltage where the inductor dries out.
V_{OUT}: Output dc voltage.

Effectively, the above relationship shows that the resetting volt-seconds are more than setting volt-seconds. In energy transfer terms this means that less energy is stored in the inductor during the ON time than it is asked to deliver during the OFF time. The net result is that the inductor dries out.

The recommended maximum duty cycle is 95% at 100KHz to allow time for the input inductor to dump its energy to the output capacitors.

For example:

if: V_{OUT} = 380V and
D_{ON} (max) = 0.95

then substituting in (3) yields V_{INDRY} = 20V. The effect of drying out is an increase in distortion at low voltages.

For a given output power, the instantaneous value of the input current is a function of the input sinusoidal voltage waveform, i.e. as the input voltage sweeps from zero volts to a maximum value equal to its peak so does the current.

The load of the power factor regulator is usually a switching power supply which is essentially a constant power load. As a result, an increase in the input voltage will be offset by a decrease in the input current.

By combining the ideas set forth above, some ground rules can be obtained for the selection and design of the input inductor:

Step 1: Find minimum operating current.

$$I_{IN}(min)_{PEAK} = \frac{1.414 \times P_{IN}(min)}{V_{IN}(max)} \quad (4)$$

V_{IN}(max) = 260V
P_{IN}(min) = 50W
then: $I_{IN}(min)_{PEAK}$ = 0.272A

Step 2: Choose a minimum current at which point the inductor current will be on the verge of drying out. For this example 40% of the peak current found in step 1 was chosen.

then: I_{LDRY} = 100mA

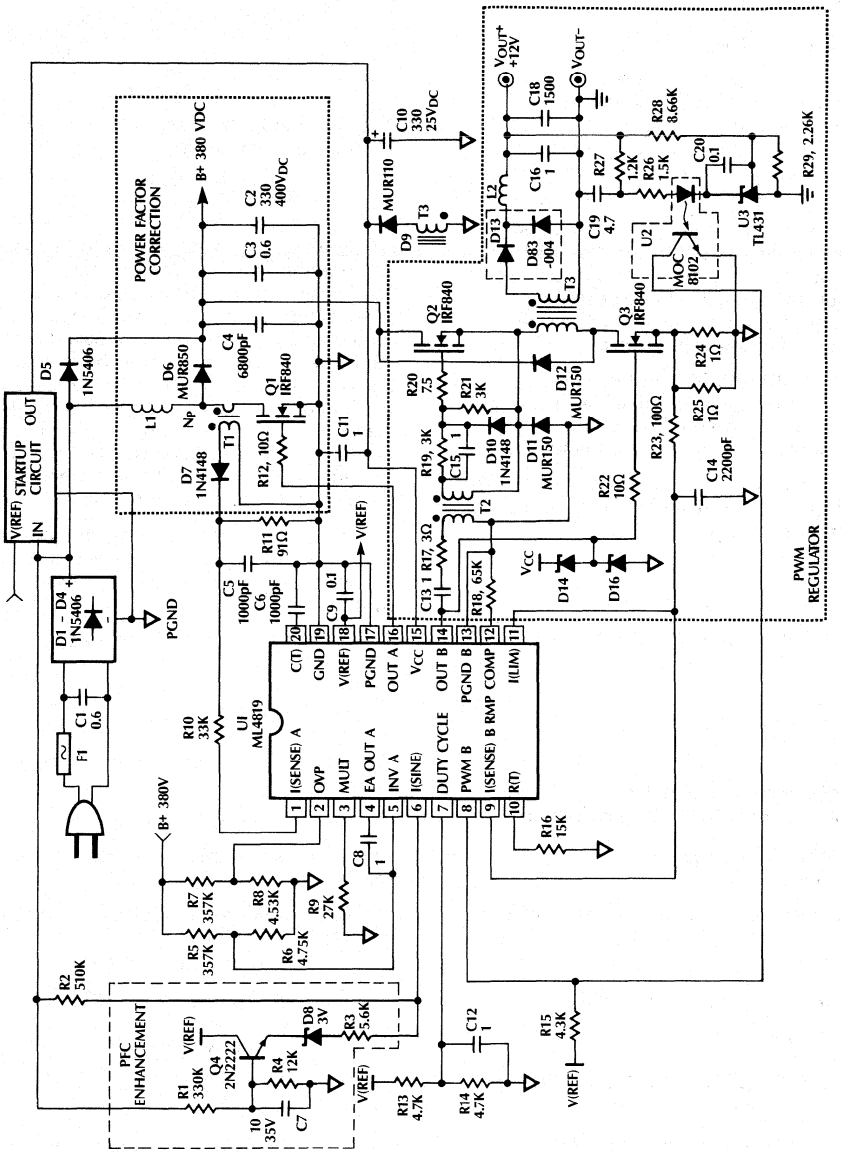


Figure 12. Typical Application, 180W Power Factor Corrected 12V Output Power Supply

Step 3: The value of the inductance can now be found using previously calculated data.

$$L1 = \frac{V_{INDRY} \times D_{ON(max)}}{I_{LDRY} \times f_{OSC}} \quad (5)$$

$$= \frac{20V \times 0.95}{100mA \times 100KHz} = 2mH$$

The inductor can be allowed to decrease in value when the current sweeps from minimum to maximum value. This allows the use of smaller core sizes. The only requirement is that the ramp compensation must be adequate for the lower inductance value of the core so that there is adequate compensation at high current.

Step 4: The presence of the ramp compensation will change the dry out point, but the value found above can be considered a good starting point. Based on the amount of power factor correction the above value of L1 can be optimized after a few iterations.

Gapped Ferrites, Molypermalloy, and Powdered Iron cores are typical choices for core material. The core material selected should have a high saturation point and acceptable losses at the operating frequency.

One ferrite core that is suitable at around 200W is the #4229PL00-3C8 made by Ferroxcube. This ungapped core will require a total gap of 0.180" for this application.

OSCILLATOR COMPONENT SELECTION

The oscillator timing components can be calculated by using the following expression:

$$f_{OSC} = \frac{1.36}{R_T \times C_T} \quad (6)$$

For example:

Step 1: At 100KHz with 95% duty cycle T_{OFF} = 500ns calculate C_T using the following formula:

$$C_T = \frac{T_{OFF} \times I_{DIS}}{V_{OSC}} = 1000pF \quad (7)$$

Step 2: Calculate the required value of the timing resistor.

$$R_T = \frac{1.36}{f_{OSC} \times C_T} = \frac{1.36}{100KHz \times 1000pF} \quad (8)$$

$$= 13.6K\Omega \text{ choose } R_T = 14K\Omega.$$

CURRENT SENSE AND SLOPE (RAMP) COMPENSATION COMPONENT SELECTION

Slope compensation in the ML4819 is provided internally. A current equal to $V_{C(T)}/2(R18)$ is added to I(SENSE) A (pin 1). This is converted to a voltage by R10, adding slope to the sensed current through T1. The amount of slope compensation should be at least 50% of the downslope of the inductor current during the off time as reflected on pin 1. Note that slope compensation is a requirement only if the inductor current is continuous and the duty cycle is more than 50%. The highest inductor downslope is found at the point of inductor discontinuity:

$$\frac{di_L}{dt} = \frac{V_B - V_{IN\ DRY}}{L} = \frac{380V - 20V}{2mH} \quad (9)$$

$$= 0.18\ A/\mu s$$

The downslope as reflected to the input of the PWM comparator is given by:

$$S_{PWM} = \frac{V_B - V_{IN\ DRY}}{L1} \times \frac{R_{11}}{N_C} \quad (10)$$

Where N_C is the turns ratio of the current transformer (T1) used. In general, current transformers simplify the sensing of switch currents especially at high power levels where the use of sense resistors is complicated by the amount of power they have to dissipate. Normally the primary side of the transformer consists of a single turn and the secondary consists of several turns of either enameled magnet wire or insulated wire. The diameter of the ferrite core used in this example is 0.5" (SPANG/Magnetics F41206-TC). The rectifying diode at the output of the current transformer can be a 1N4148 for secondary currents up to 75mA average.

Sense FETs or resistive sensing can also be used to sense the switch current, the sensed signal has to be amplified to the proper level before it is applied to the ML4819.

The value of the ramp compensation (SC_{PWM}) as seen at pin 1 is:

$$SC_{PWM} = \frac{2.5 \times R_9}{R_{16} \times C_6 \times R_{18}} \quad (11)$$

The required value for R_{18} can therefore be found by equating:

$$SC_{PWM} = A_{SC} \times S_{PWM}$$

where A_{SC} is the amount of slope compensation and solving for R_{18}.

The value of R_9 (pin 2) depends on the selection of R_2 (pin 6)

$$R_2 = \frac{V_{IN(max)PEAK}}{I_{SINE}(peak)} = \frac{260 \times 1.414}{0.72mA} = 510K \quad (12)$$

$$R_9 > \frac{V_{CLAMP} \times R_2}{V_{IN(min)PEAK}} = \frac{4.8 \times 510K}{80 \times 1.414} \cong 22K \quad (13)$$

Choose R9 = 27K

The peak of the inductor current can be found approximately by:

$$I_{LPEAK} = \frac{1.414 \times P_{OUT}}{V_{IN(min)RMS}} = \frac{1.414 \times 200}{90} = 3.14A \quad (14)$$

Selection of N_C which depends on the maximum switch current, assume 4A for this example is 80 turns.

$$R_{11} = \frac{V_{CLAMP} \times N_C}{I_{LPEAK}} = \frac{4.8 \times 80}{4} \cong 100\Omega \quad (15)$$

Where R_{11} is the sense resistor, and V_{CLAMP} is the current clamp at the inverting input of the PWM comparator. This clamp is internally set to 5V. In actual application it is a good idea to assume a value less than 5V to avoid unwanted current limiting action due to component tolerances. In this application V_{CLAMP} was chosen as 4.8V.

Having calculated R_{11} the value S_{PWM} and of R_{18} can now be calculated:

$$S_{PWM} = \frac{380V - 20}{2mH} \times \frac{100}{80} = 0.225V/\mu s$$

$$R_{18} = \frac{2.5 \times R_9}{A_{SC} \times S_{PWM} \times R_T \times C_T} \quad (16)$$

$$R_{18} = \frac{2.5 \times 27K}{0.7 \times (.225 \times 10^6) \times 14K \times 1nF} \cong 30K$$

Choose R18 = 33K

The following values were used in the calculation:

$R_9 = 27K$ $\quad A_{SC} = 0.7$
$R_T = 14K$ $\quad C_T = 1nF$

VOLTAGE REGULATION COMPONENTS

The values of the voltage regulation loop components are calculated based on the operating output voltage. Note that voltage safety regulations require the use of sense resistors that have adequate voltage rating. As a rule of thumb if 1/4W resistors are available, two of them should be used in series. The input bias current of the error amplifier is approximately 0.5μA, therefore the current available from the voltage sense resistors should be significantly higher than this value. Since two 1/4W resistors have to be used the total power rating is 1/2W. The operating power is set to be 0.4W then with 380V output voltage the value can be calculated as follows:

$$R_5 = (380V)^2/0.4W = 360K \quad (17)$$

Choose two 178K, 1% connected in series.

Then R_6 can be calculated using the formula below:

$$R_6 = \frac{V_{REF} \times R_5}{V_B - V_{REF}} = \frac{5V \times 356K}{380V - 5V} = 4.747K \quad (18)$$

Choose 4.75K, 1%. One more critical component in the voltage regulation loop is the feedback capacitor for the error amplifier. The voltage loop bandwidth should be set such that it rejects the 120Hz ripple which is present at the output. If this ripple is not adequately attenuated it will cause distortion on the input current waveform. Typical bandwidths range anywhere from a few Hertz to 15Hz. The main compromise is between transient response and distortion. The feedback capacitor can be calculated using the following formula:

$$C_8 = \frac{1}{3.142 \times R_5 \times BW} \quad (19)$$

$$C_8 = \frac{1}{3.142 \times 356K \times 2Hz} = 0.44\mu F$$

OVERVOLTAGE PROTECTION (OVP) COMPONENTS

The OVP loop should be set so that there is no interaction with the voltage control loop. Typically it should be set to a level where the power components are safe to operate. Ten to fifteen volts above V_{OUT} seems to be adequate. This sets the maximum transient output voltage to about 395V.

By choosing the high voltage side resistor of the OVP circuit the same way as above i.e. R_7 = 356K then R_8 can be calculated as:

$$R_8 = \frac{V_{REF} \times R_7}{V_{OVP} - V_{REF}} = \frac{5V \times 356K}{395V - 5V} = 4.564K \quad (20)$$

Choose 4.53K, 1%.

Note that R_5, R_6, R_7 and R_8 should be tight tolerance resistors such as 1% or better.

OFF-LINE START-UP AND BIAS SUPPLY GENERATION

The Start-Up Circuit in figure 12 can be either a "bleed resistor" (39KΩ, 2W) or the circuit shown in figure 13. The bleed resistor method offers the advantage of simplicity and lowest cost, but may yield excessive turn-on delay at low line.

When the voltage on pin 15 (V_{CC}) exceeds 16V, the IC starts up. The energy stored on the C10 supplies the IC with running power until the supplemental winding on T3 can provide the power to sustain operation.

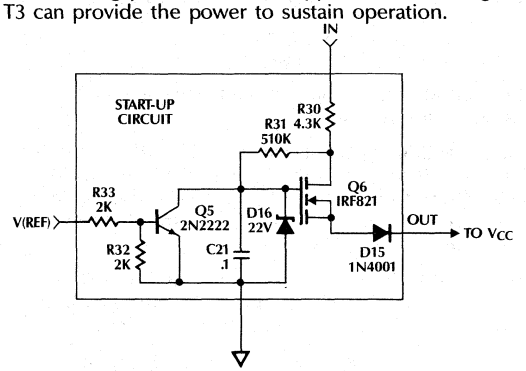


Figure 13. Start-Up Circuit

ENHANCEMENT CIRCUIT

The theory of operation of the power factor enhancement circuit (inside the dotted lines) in Figure 11 is described in APPLICATION NOTE 11 in detail. It improves the power factor and lowers the input current harmonics. Note that the circuit meets the proposed IEC 555 specifications (with the enhancement) on the harmonics with a large margin while correcting the input power factor to better than 0.99 under most steady state operating conditions.

PWM SECTION

The PWM section in figure 12 is a two switch forward converter, shown in figure 14 below for clarity. This fully clamped circuit eliminates the need for very high voltage MOSFETs. Flyback topology is also possible with the ML4819.

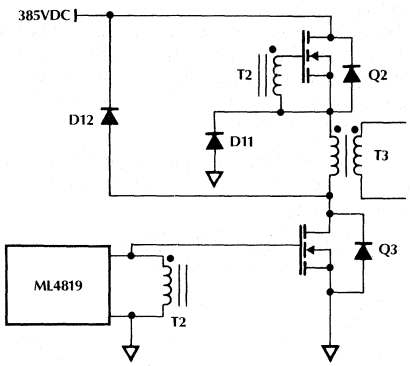


Figure 14. Two-Switch Forward Converter

This regulator (figure 12) uses current mode control. Current is sensed through R24 and filtered for high frequency noise and leading edge transient through R23 and C14. The main regulation loop is through PWM B. The TL431 (U3) in the secondary serves as both the voltage reference and error amplifier, with isolation provided by an opto coupler (U2) providing a current command signal on pin 8. Loop compensation is provided by R29 and C20. The output voltage is set by:

$$V_{OUT} = 2.5 \left(1 + \frac{R_{29}}{R_{28}} \right) \quad (21)$$

The control loop is compensated using standard compensation techniques.

Current is limited to a threshold of 2A (1V on R24). The duty cycle is limited in this circuit to below 50% to prevent transformer (T3) core saturation. The maximum duty cycle limit of 45% is set using a threshold of $V_{REF}/2$ on pin 7.

The circuit in figure 12 can be modified for voltage mode operation by utilizing the slope current which appears on pin 9 as shown in figure 15 below.

The ramp amplitude appearing on pin 9 will be

$$V_R = \frac{I_{R18}}{2} \times R(V) \quad (22)$$

where R_{18} is the slope compensation resistor. Since this circuit operates with a constant input voltage (as supplied by the PFC section) voltage feed-forward is unnecessary.

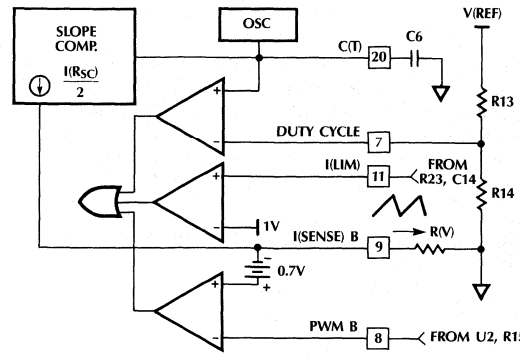


Figure 15. Voltage Mode Configuration

CONSTRUCTION AND LAYOUT TIPS

High frequency power circuits require special care during breadboard construction and layout. Double sided printed circuit boards with ground plane on one side are highly recommended. All critical switching leads (power FET, output diode, IC output and ground leads, bypass capacitors) should be kept as small as possible. This is to minimize both the transmission and pick-up of switching noise.

There are two kinds of noise coupling; inductive and capacitive. As the name implies inductive coupling is due to fast changing (high di/dt) circulating switching currents. The main source is the loop formed by Q1, D6, and C3–C4. Therefore this loop should be as small as possible, and the above capacitors should be good high frequency types.

The second form of noise coupling is due to fast changing voltages (high dv/dt). The main source in this case is the drain of the power FET. The radiated noise in this case can be minimized by insulating the drain of the FET from the heatsink and then tying the heatsink to the source of the FET with a high frequency capacitor.

The IC has two ground pins named PWR GND and Signal GND. These two pins should be connected together with a very short lead at the printed circuit board exit point. In general grounding is very important and ground loops should be avoided. Star grounding schemes are preferred.

Component Values/Bill of Materials for Figure 12

Component	Description
C1, C3	0.6μF, 630V Film (250 VAC)
C2	330μF, 400V Electrolytic
C4	6800pF, 1KV Ceramic
C5, C6	1000pF
C7	10μF, 35V
C8, C11, C13, C15, C16	1μF, Ceramic
C9, C20, C21	0.1μF, Ceramic
C10	1500μF, 25V Electrolytic
C12, C17	1μF, Ceramic
C14	2200pF
C18	1500μF, 16V Electrolytic
C19	4.7μF
D1–D5	1N5406
D6	MUR850
D7, D10	1N4148
D8	3V Zener diode or 4 × 1N4148 in series
D9	MUR110
D11, D12	MUR150
D13	D83-004K
D15	1N4001
D16, D14	1N5818 or 1N5819
F1	5A, 250V, 3AG
L1	2mH, 4A I_{PEAK} Core: Ferroxcube 4229-3C8 150 Turns #24 AWG 0.150" gap
L2	10μH Core: Spang OF 43019 UG00 8 Turns #15AWG gap 0.05"
Q1–Q3	IRF840
Q4, Q5	2N2222
Q6	IRF821
R1	330K
R2, R31	510K
R3	5.6K

Component	Description
R4	12K
R5, R7	357K, 1%
R6	4.75K, 1%
R8	4.53K, 1%
R9	27K
R10, R18	33K
R11	91Ω
R12, R22	10Ω
R13, R14	4.7K
R15	4.3K
R16	15K
R17	3Ω
R20	7.5Ω
R21, R19	3K
R23	100Ω
R24, R25	1Ω
R26	1.5K
R27	1.2K
R28	8.66K, 1%
R29	2.26K, 1%
R30	2K, 1W
R32, R33	2K
T1	Spang F41206-TC or Siemens B64290-K45-X27 or X830 or Ferroxcube 768T188-3C8 N_S = 80, N_P = 1
T2	Same core as T1 $N_S = N_P$ = 15 bifilar
T3	Core: Ferroxcube 4229-3C8 Pri. 44 Turns #18 Litz wire Sec. 4 Turns of copper strip Aux. 2 Turns #24 AWG
U2	MOC8102
U3	TL431

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ML4819CP	0°C to +70°C	Molded DIP
ML4819CQ	0°C to +70°C	Molded PCC

Micro Linear

ML4823

High Frequency Power Supply Controller

GENERAL DESCRIPTION

The ML4823 High Frequency PWM Controller is an IC controller optimized for use in Switch Mode Power Supply designs running at frequencies to 1MHz. Propagation delays are minimal through the comparators and logic for reliable high frequency operation while slew rate and bandwidth are maximized on the error amplifier. This controller is designed for single-ended applications using voltage or current mode and provides for input voltage feed forward.

A 1V threshold current limit comparator provides cycle-by-cycle current limit and exceeding a 1.4V threshold initiates a soft-start cycle. The soft start pin doubles as a maximum duty cycle clamp. All logic is fully latched to provide jitter-free operation and prevent multiple pulsing. An under-voltage lockout circuit with 800mV of hysteresis assures low startup current and drives the outputs low during fault conditions.

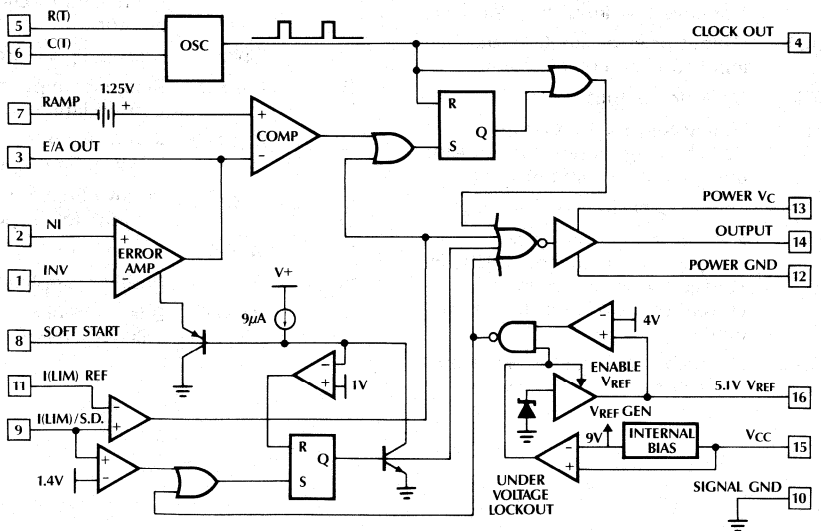
The ML4823 is fabricated on a 40V bipolar process FB3480 Power Supply Controller Array. Customized versions of this controller are therefore easily implemented. Please refer to the FB3480 datasheet for more information.

This controller is similar in architecture and performance to the UC1823 controller, however the ML4823 includes features not found on the 1823. These features are set in *Italics.*

FEATURES

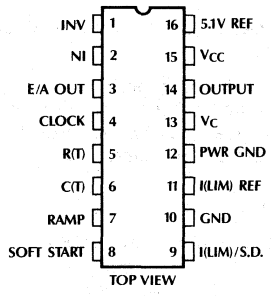
- Practical Operation at Switching Frequencies to 1.0MHz
- High Current (2A peak) Totem Pole Output
- Wide Bandwidth Error Amplifier
- Fully Latched Logic
- Pulse-by-Pulse Current Limiting
- Soft Start and Max. Duty Cycle Control
- Under Voltage Lockout with Hysteresis
- 5.1V, ±1% Trimmed Bandgap Reference
- Pin Compatible Improved Replacement for UC1823
- *Fast Shut Down Path from Current Limit to Outputs*
- *Soft Start Latch Ensures Full Soft Start Cycle*
- *Outputs Pull Low for Undervoltage Lockout*

BLOCK DIAGRAM



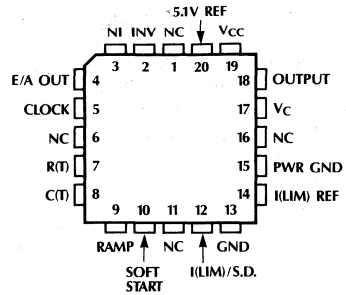
PIN CONNECTIONS

ML4823
16-Pin DIP



TOP VIEW

ML4823
20-Pin PCC



TOP VIEW

PIN DESCRIPTION

PIN #	NAME	FUNCTION
1	INV	Inverting input to error amp.
2	NI	Non-inverting input to error amp.
3	E/A OUT	Output of error amplifier and input to main comparator.
4	CLOCK	Oscillator output.
5	R(T)	Timing Resistor for Oscillator — sets charging current for oscillator timing capacitor (pin 6).
6	C(T)	Timing Capacitor for Oscillator.
7	RAMP	Non-Inverting input to main comparator. Connected to C(T) for Voltage Mode operation or to current sense resistor for current mode.
8	SOFT START	Normally connected to Soft Start Capacitor.
9	I(LIM)/S.D.	Current limit sense pin. Normally connected to current sense resistor.
10	GND	Analog Signal Ground.
11	I(LIM) REF	Reference input for cycle-by-cycle current limit comparator.
12	PWR GND	Return for the High Current Totem pole outputs.
13	V_C	Positive Supply for the High Current Totem pole outputs.
14	OUT B	High Current Totem pole output.
15	V_{CC}	Positive Supply for the IC.
16	5.1V REF	Buffered output for the 5.1V voltage reference.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (Pins 15, 13) 30V
Output Current, Source or Sink (Pins 11, 14)
DC 0.5A
Pulse (0.5μs) 2.0A
Analog Inputs
(Pins 1, 2, 7, 8, 9) ..... -0.3V to 6V
Clock Output Current (Pin 4) ..... -5mA
Error Amplifier Output Current (Pin 3) 5mA
Soft Start Sink Current (Pin 8) 20mA
Oscillator Charging Current (Pin 5) ..... -5mA
Junction Temperature
ML4823M ..... 150°C
ML4823I, ML4823C ..... 125°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering 10 sec.) ..... +260°C

Thermal Resistance (θ_{JA})
Plastic DIP ..... 65°C/W
Ceramic DIP ..... 65°C/W
Plastic Chip Carrier (PCC) ..... 60°C/W

OPERATING CONDITIONS

Temperature Range
ML4823M ..... -55°C to +125°C
ML4823I ..... -40°C to +85°C
ML4823C ..... 0°C to +70°C

Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, R_T = 3.65KΩ, C_T = 1000pF, T_A = Operating Temperature Range, V_{CC} = 15V.

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
Oscillator						
Initial Accuracy		T_J = 25°C, (note 1)	360	400	440	KHz
Voltage Stability		10V < V_{CC} < 30V, (note 1)		0.2	2	%
Temperature Stability		(note 1)			5	%
Total Variation		line, temp, (note 1)	340		460	KHz
Clock Out High			3.9	4.5		V
Clock Out Low				2.3	2.9	V
Ramp Peak		(note 1)	2.6	2.8	3.0	V
Ramp Valley		(note 1)	0.7	1.0	1.25	V
Ramp Valley to Peak		(note 1)	1.6	1.8	2.0	V
Reference Section						
Output Voltage	ML4823C	T_J = 25°C, I_O = 1mA	5.00	5.10	5.20	V
	ML4823M, ML4823I		5.05	5.10	5.15	V
Line Regulation		10V < V_{CC} < 30V		2	20	mV
Load Regulation		1mA < I_O < 10mA		5	20	mV
Temperature Stability		-55°C < T_J < 150°C, (note 1)		.2	.4	%
Total Variation	ML4823C	line, load, temp, (note 1)	4.95		5.25	V
	ML4823M, ML4823I		5.0		5.20	V
Output Noise Voltage		10Hz to 10KHz		50		μV
Long Term Stability		T_J = 125°C, 1000 hrs, (note 1)		5	25	mV
Short Circuit Current		V_{REF} = 0V	-15	-50	-100	mA
Error Amplifier Section						
Input Offset Voltage	ML4823C				15	mV
	ML4823M, ML4823I				10	mV
Input Bias Current				.6	3	μA
Input Offset Current				.1	1	μA
Open Loop Gain		1 < V_O < 4V	60	95		dB

ELECTRICAL CHARACTERISTICS (Continued)

Unless otherwise specified, R_T = 3.65KΩ, C_T = 1000pF, T_A = Operating Temperature Range, V_{CC} = 15V.

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
Error Amplifier Section (Continued)						
CMRR		$1.5 < V_{CM} < 5.5V$	75	95		dB
PSRR		$10 < V_{CC} < 30V$	85	110		dB
Output Sink Current		$V_{PIN\ 3}$ = 1V	1	2.5		mA
Output Source Current		$V_{PIN\ 3}$ = 4V	-.5	-1.3		mA
Output High Voltage		$I_{PIN\ 3}$ = -0.5mA	4.0	4.7	5.0	V
Output Low Voltage		$I_{PIN\ 3}$ = 1mA	0	0.5	1.0	V
Unity Gain Bandwidth		(note 1)	3	5.5		MHz
Slew Rate		(note 1)	6	12		V/μs
PWM Comparator Section						
Pin 7 Bias Current		$V_{PIN\ 7}$ = 0V		-1	-5	μA
Duty Cycle Range	ML4823C		0		85	%
	ML4823M, ML4823I		0		80	%
Pin 3 Zero DC Threshold		$V_{PIN\ 7}$ = 0V	1.1	1.25		V
Delay to Output		(note 1)		50	80	ns
Soft-Start Section						
Charge Current		$V_{PIN\ 8}$ = 0.5V	3	9	20	μA
Discharge Current		$V_{PIN\ 8}$ = 1V	1			mA
Current Limit/Shutdown Section						
Pin 9 Bias Current		$0V < V_{PIN\ 9} < 4V$			+10	μA
Current Limit Offset		$V_{PIN\ 11}$ = 1.1V	0		30	mV
Pin 11 Common Mode Range			1.0		1.25	V
Shutdown Threshold			1.25	1.4	1.55	V
Delay to Output		(note 1)		40	70	ns
Output Section						
Output Low Level		I_{OUT} = 20mA		.25	.4	V
		I_{OUT} = 200mA		1.2	2.2	V
Output High Level		I_{OUT} = -20mA	13.0	13.5		V
		I_{OUT} = -200mA	12.0	13.0		V
Collector Leakage		V_C = 30V		100	500	μA
Rise/Fall Time		C_L = 1000pF, (note 1)		30	60	ns
Under-Voltage Lockout Section						
Start Threshold			8.8	9.2	9.6	V
UVLO Hysteresis			.4	.8	1.2	V
Supply Current						
Start Up Current		V_{CC} = 8V		1.1	2.5	mA
I_{CC}		$V_{PIN\ 1,\ 7,\ 9}$ = 0V, $V_{PIN\ 2}$ = 1V		25	33	mA

Note 1: This parameter not 100% tested in production but guaranteed by design.

FUNCTIONAL DESCRIPTION

OSCILLATOR

The ML4823 oscillator charges the external capacitor (C_T) with a current (I_{SET}) equal to $3/R_{SET}$. When the capacitor voltage reaches the upper threshold (Ramp Peak), the comparator changes state and the capacitor discharges to the lower threshold (Ramp Valley) through Q1. While the capacitor is discharging, Q2 provides a high pulse.

The Oscillator period can be described by the following relationship:

$$T_{OSC} = T_{RAMP} + T_{DEADTIME}$$

where: $T_{RAMP} = C$ (Ramp Valley to Peak)$/I_{SET}$

and: $T_{DEADTIME} = C$ (Ramp Valley to Peak)$/I_{Q1}$

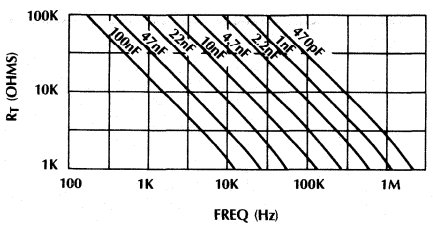


Figure 2. Oscillator Timing Resistance vs Frequency

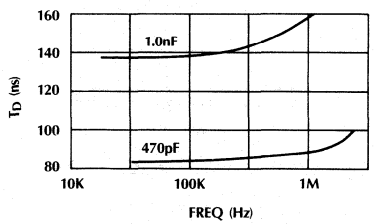


Figure 3. Oscillator Deadtime vs Frequency

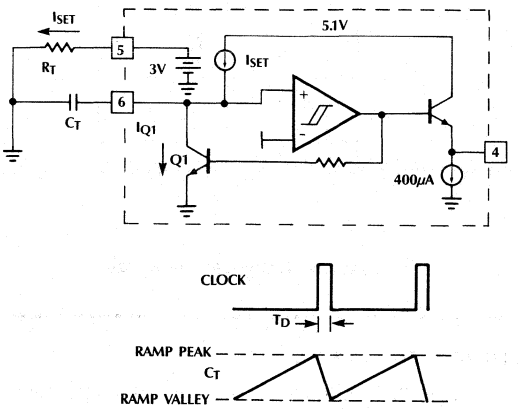


Figure 1. Oscillator Block Diagram

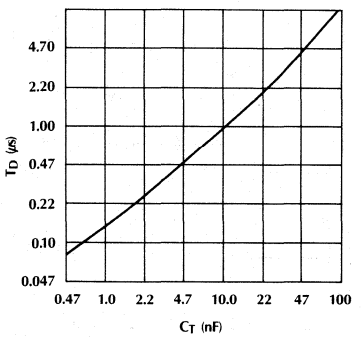


Figure 4. Oscillator Deadtime vs C(T) (3KΩ ≤ R(T) ≤ 100KΩ)

6

ERROR AMPLIFIER

The ML4823 error amplifier is a 5.5MHz bandwidth 12V/μs slew rate op-amp with provision for limiting the positive output voltage swing (Output Inhibit line) for ease in implementing the soft start function.

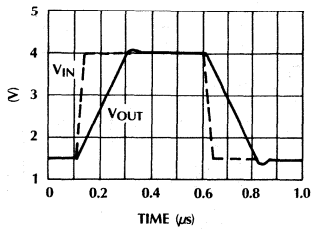


Figure 5. Unity Gain Slew Rate

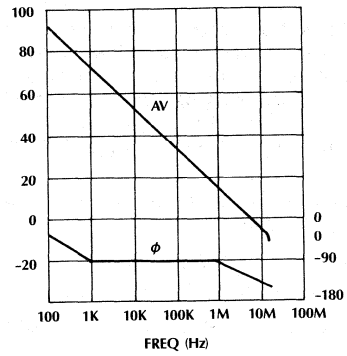


Figure 6. Open Loop Frequency Response

OUTPUT DRIVER STAGE

The ML4823 Output Driver is a 2A peak output high speed totem pole circuit designed to quickly switch the gates of capacitive loads, such as power MOSFET transistors.

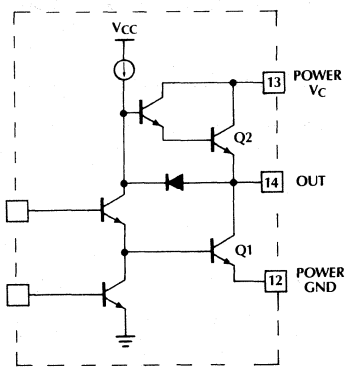


Figure 7. Simplified Schematic

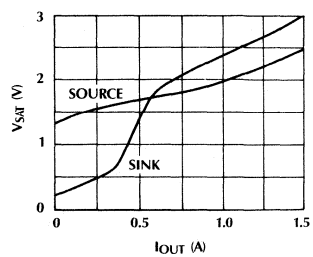


Figure 8. Saturation Curves

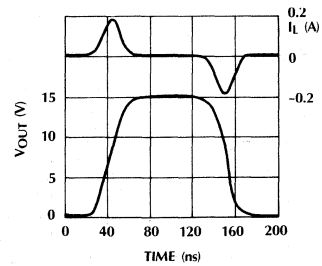


Figure 9. Rise/Fall Time (C_L = 1000pF)

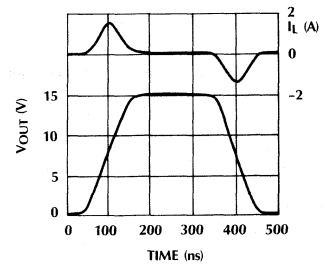


Figure 10. Rise/Fall Time (C_L = 10,000pF)

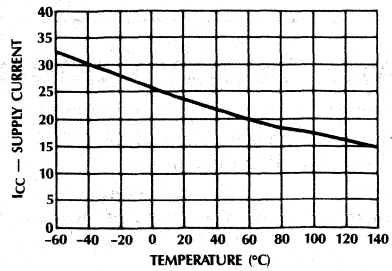


Figure 11. Supply Current vs Temperature

SOFT START AND CURRENT LIMIT

The ML4823 employs two current limits. When the voltage at pin 9 exceeds the I(LIM) REF threshold on pin 11, the outputs are immediately shut off and the cycle is terminated for the remainder of the oscillator period by resetting the RS flip flop.

If the output current is rising quickly (usually due to transformer saturation) such that the voltage on pin 9 reaches 1.4V before the outputs have turned off, a soft start cycle is initiated. The soft start capacitor (pin 8) is discharged and outputs are held "off" until the voltage at pin 8 reaches 1V, ensuring a complete soft start cycle. The duty cycle on start up is limited by limiting the output voltage of the error amplifier voltage to the voltage at pin 8.

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ML4823CP	0°C to +70°C	Molded DIP
ML4823CQ	0°C to +70°C	Molded PCC
ML4823IP	-40°C to +85°C	Molded DIP
ML4823IQ	-40°C to +85°C	Molded PCC
ML4823MJ	-55°C to +125°C	Hermetic DIP
ML4823CS	0°C to +70°C	Molded SOIC

Micro Linear

ML4825

High Frequency Power Supply Controller

GENERAL DESCRIPTION

The ML4825 High Frequency PWM Controller is an IC controller optimized for use in Switch Mode Power Supply designs running at frequencies to 1MHz. Propagation delays are minimal through the comparators and logic for reliable high frequency operation while slew rate and bandwidth are maximized on the error amplifier. This controller is designed to work in either voltage or current mode and provides for input voltage feed forward.

A 1V threshold current limit comparator provides cycle-by-cycle current limit while exceeding a 1.4V threshold initiates a soft-start cycle. The soft start pin doubles as a maximum duty cycle clamp. All logic is fully latched to provide jitter-free operation and prohibit multiple pulsing. An under-voltage lockout circuit with 800mV of hysteresis assures low startup current and drives the outputs low.

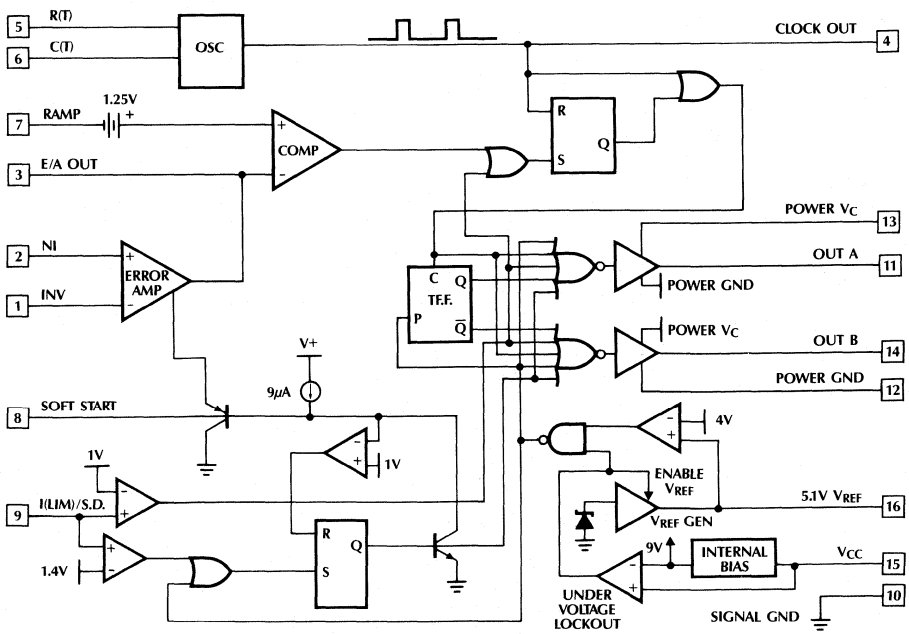
The ML4825 is fabricated on a 40V bipolar process from the FB3480 Power Supply Controller Array. Customized versions of this controller are therefore easily implemented. Please refer to the FB3480 datasheet for more information.

This controller is similar in architecture and performance to the UC1825 controller, however the ML4825 includes many features not found on the 1825. These features are set in *Italics*.

FEATURES

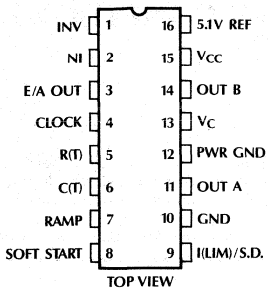
- Practical Operation at Switching Frequencies to 1.0MHz
- High Current (2A peak) Dual Totem Pole Outputs
- Wide Bandwidth Error Amplifier
- Fully Latched Logic with Double Pulse Suppression
- Pulse-by-Pulse Current Limiting
- Soft Start and Max. Duty Cycle Control
- Under Voltage Lockout with Hysteresis
- 5.1V, ±1% Trimmed Bandgap Reference
- Pin Compatible Improved Replacement for UC1825
- *Fast Shut Down Path from Current Limit to Outputs*
- *Outputs Preset to Known Condition After Under Voltage Lockout*
- *Soft Start Latch Ensures Full Soft Start Cycle*
- *Outputs Pull Low for Undervoltage Lockout*

BLOCK DIAGRAM

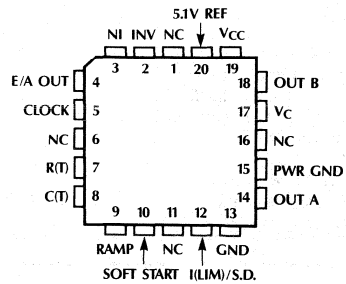


PIN CONNECTIONS

ML4825
16-Pin DIP



ML4825
20-Pin PCC



PIN DESCRIPTION

PIN #	NAME	FUNCTION
1	INV	Inverting input to error amp.
2	NI	Non-inverting input to error amp.
3	E/A OUT	Output of error amplifier and input to main comparator.
4	CLOCK	Oscillator output.
5	R(T)	Timing Resistor for Oscillator — sets charging current for oscillator timing capacitor (pin 6).
6	C(T)	Timing Capacitor for Oscillator.
7	RAMP	Non-Inverting input to main comparator. Connected to C(T) for Voltage Mode operation or to current sense resistor for current mode.
8	SOFT START	Normally connected to Soft Start Capacitor.
9	I(LIM)/S.D.	Current limit sense pin. Normally connected to current sense resistor.
10	GND	Analog Signal Ground.
11	OUT A	High Current Totem pole output. This output is the first one energized after Power On Reset.
12	PWR GND	Return for the High Current Totem pole outputs.
13	V_C	Positive Supply for the High Current Totem pole outputs.
14	OUT B	High Current Totem pole output.
15	V_{CC}	Positive Supply for the IC.
16	5.1V REF	Buffered output for the 5.1V voltage reference.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (Pins 15, 13) 30V
Output Current, Source or Sink (Pins 11, 14)
DC 0.5A
Pulse (0.5μs) 2.0A
Analog Inputs
(Pins 1, 2, 7) ..... –0.3V to 7V
(Pins 9, 8) ..... –0.3V to 6V
Clock Output Current (Pin 4) ..... –5mA
Error Amplifier Output Current (Pin 3) 5mA
Soft Start Sink Current (Pin 8) 20mA
Oscillator Charging Current (Pin 5) ..... –5mA
Junction Temperature
ML4825M ..... 150°C
ML4825I, ML4825C ..... 125°C
Storage Temperature Range ..... –65°C to +150°C
Lead Temperature (Soldering 10 sec.) ..... +260°C

Thermal Resistance (θ_{JA})
Plastic DIP ..... 65°C/W
Ceramic DIP ..... 65°C/W
Plastic Chip Carrier (PCC) ..... 60°C/W

OPERATING CONDITIONS

Temperature Range
ML4825M ..... –55°C to +125°C
ML4825I ..... –40°C to +85°C
ML4825C ..... 0°C to +70°C

Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, R_T = 3.65KΩ, C_T = 1000pF, T_A = Operating Temperature Range, V_{CC} = 15V.

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
Oscillator						
Initial Accuracy		T_J = 25°C, (note 1)	360	400	440	KHz
Voltage Stability		10V < V_{CC} < 30V, (note 1)		0.2	2	%
Temperature Stability		(note 1)			5	%
Total Variation		line, temp, (note 1)	340		460	KHz
Clock Out High			3.9	4.5		V
Clock Out Low				2.3	2.9	V
Ramp Peak		(note 1)	2.6	2.8	3.0	V
Ramp Valley		(note 1)	0.7	1.0	1.25	V
Ramp Valley to Peak		(note 1)	1.6	1.8	2.0	V
Reference Section						
Output Voltage	ML4825C	T_J = 25°C, I_O = 1mA	5.00	5.10	5.20	V
	ML4825M, ML4825I		5.05	5.10	5.15	V
Line Regulation		10V < V_{CC} < 30V		2	20	mV
Load Regulation		1mA < I_O < 10mA		5	20	mV
Temperature Stability		–55°C < T_J < 150°C, (note 1)		.2	.4	%
Total Variation	ML4825C	line, load, temp (note 1)	4.95		5.25	V
	ML4825M, ML4825I	line, load, temp (note 1)	5.0		5.20	V
Output Noise Voltage		10Hz to 10KHz		50		μV
Long Term Stability		T_J = 125°C, 1000 hrs, (note 1)		5	25	mV
Short Circuit Current		V_{REF} = 0V	–15	–50	–100	mA
Error Amplifier Section						
Input Offset Voltage	ML4825C				15	mV
	ML4825M, ML4825I				10	mV
Input Bias Current				.6	3	μA
Input Offset Current				.1	1	μA
Open Loop Gain		1 < V_O < 4V	60	96		dB

ELECTRICAL CHARACTERISTICS (Continued)

Unless otherwise specified, R_T = 3.65KΩ, C_T = 1000pF, T_A = Operating Temperature Range, V_{CC} = 15V.

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
Error Amplifier Section (Continued)						
CMRR		$1.5 < V_{CM} < 5.5V$	75	95		dB
PSRR		$10 < V_{CC} < 30V$	85	110		dB
Output Sink Current		$V_{PIN\ 3}$ = 1V	1	2.5		mA
Output Source Current		$V_{PIN\ 3}$ = 4V	–.5	–1.3		mA
Output High Voltage		$I_{PIN\ 3}$ = –0.5mA	4.0	4.7	5.0	V
Output Low Voltage		$I_{PIN\ 3}$ = 1mA	0	0.5	1.0	V
Unity Gain Bandwidth		(note 1)	3	5.5		MHz
Slew Rate		(note 1)	6	12		V/μs
PWM Comparator Section						
Pin 7 Bias Current		$V_{PIN\ 7}$ = 0V		–1	–5	μA
Duty Cycle Range	ML4825C		0		85	%
	ML4825M, ML4825I		0		80	%
Pin 3 Zero DC Threshold		$V_{PIN\ 7}$ = 0V	1.1	1.25		V
Delay to Output		(note 1)		50	80	ns
Soft-Start Section						
Charge Current		$V_{PIN\ 8}$ = 0.5V	3	9	20	μA
Discharge Current		$V_{PIN\ 8}$ = 1V	1			mA
Current Limit/Shutdown Section						
Pin 9 Bias Current	ML4825C	$0V < V_{PIN\ 9} < 4V$			+15	μA
	ML4825M, ML4825I	$0V < V_{PIN\ 9} < 4V$			+10	μA
Current Limit Threshold			.9	1	1.1	V
Shutdown Threshold			1.25	1.4	1.55	V
Delay to Output		(note 1)		40	70	ns
Output Section						
Output Low Level		I_{OUT} = 20mA		.25	.4	V
		I_{OUT} = 200mA		1.2	2.2	V
Output High Level		I_{OUT} = –20mA	13.0	13.5		V
		I_{OUT} = –200mA	12.0	13.0		V
Collector Leakage		V_C = 30V		100	500	μA
Rise/Fall Time		C_L = 1000pF, (note 1)		30	60	ns
Under-Voltage Lockout Section						
Start Threshold			8.8	9.2	9.6	V
UVLO Hysteresis			.4	.8	1.2	V
Supply Current						
Start Up Current		V_{CC} = 8V		1.1	2.5	mA
I_{CC}		$V_{PIN\ 1,\ 7,\ 9}$ = 0V, $V_{PIN\ 2}$ = 1V, T_A = 25°C		26	33	mA

Note 1: This parameter not 100% tested in production but guaranteed by design.

FUNCTIONAL DESCRIPTION

OSCILLATOR

The ML4825 oscillator charges the external capacitor (C_T) with a current (I_{SET}) equal to $3/R_{SET}$. When the capacitor voltage reaches the upper threshold (Ramp Peak), the comparator changes state and the capacitor discharges to the lower threshold (Ramp Valley) through Q1. While the capacitor is discharging, Q2 provides a high pulse.

The Oscillator period can be described by the following relationship:

$$T_{OSC} = T_{RAMP} + T_{DEADTIME}$$

where: $T_{RAMP} = C$ (Ramp Valley to Peak)$/I_{SET}$

and: $T_{DEADTIME} = C$ (Ramp Valley to Peak)$/I_{Q1}$

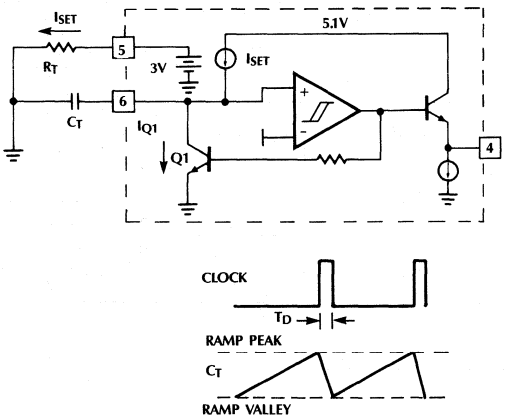
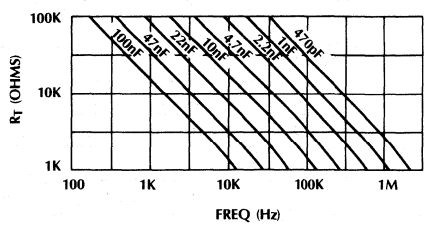


Figure 1. Oscillator Block Diagram



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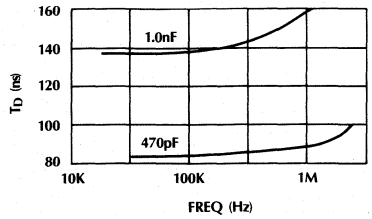

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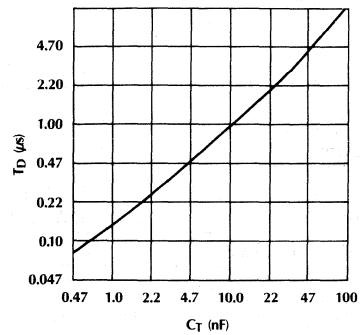

Figure 4. Oscillator Deadtime vs C(T) (3KΩ ≤ R(T) ≤ 100KΩ)

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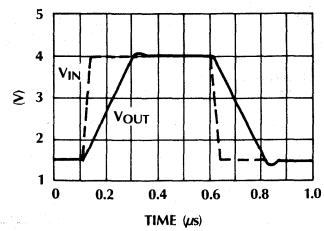

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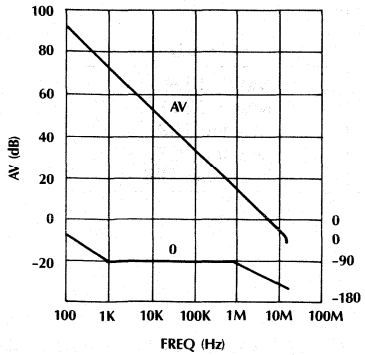

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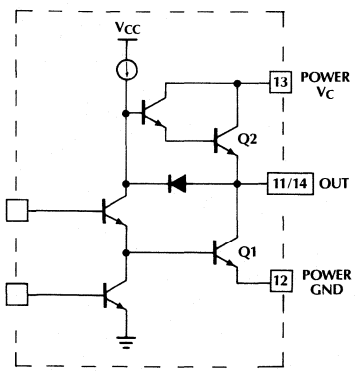

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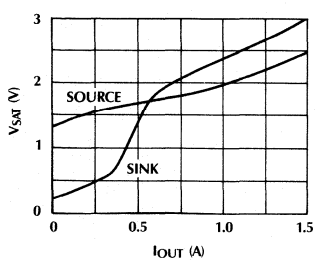


Figure 8. Saturation Curves

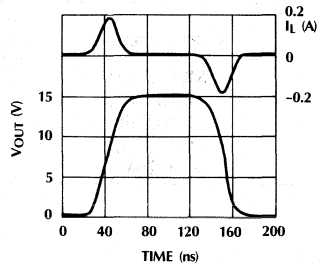


Figure 9. Rise/Fall Time (C_L = 1000pF)

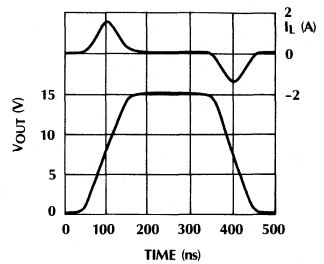


Figure 10. Rise/Fall Time (C_L = 10,000pF)

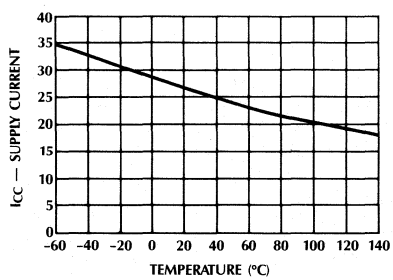


Figure 11. Supply Current vs Temperature

SOFT START AND CURRENT LIMIT

The ML4825 employs two current limits. When the voltage at pin 9 exceeds 1V, the outputs are immediately shut off and the cycle is terminated for the remainder of the oscillator period by resetting the RS flip flop.

If the output current is rising quickly such that the voltage on pin 9 reaches 1.4V before the outputs have turned off, a soft start cycle is initiated. The soft start capacitor (pin 8) is discharged and outputs are held "off" until the voltage at pin 8 reaches 1V, ensuring a complete soft start cycle. The duty cycle on start up is limited by limiting the output voltage of the error amplifier voltage to the voltage at pin 8.

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ML4825CP	0°C to +70°C	Molded DIP
ML4825CQ	0°C to +70°C	Molded PCC
ML4825IP	–40°C to +85°C	Molded DIP
ML4825IQ	–40°C to +85°C	Molded PCC
ML4825MJ	–55°C to +125°C	Hermetic DIP

Micro Linear

FB3480

Power Supply Controller Array

GENERAL DESCRIPTION

The FB3480 Power Supply Controller Array is a new concept in Switch Mode Power Supply Controller (SMPS) technology. This Array is the first configurable bipolar array specifically designed for SMPS applications. The FB3480 is optimized for high performance and low design cost and time, since most of the commonly used SMPS functions have been pre-designed and characterized.

With the FB3480 a power supply designer can select his own unique controller topology and features without the need for external components. This flexibility allows compact PC board layout, minimizing interference from induced RFI/EMI, and enhancing high frequency performance.

The FB3480 contains all of the elements found in most SMPS controllers in addition to areas of uncommitted circuitry on the Array which can be configured for unique applications. The core of the array is similar in performance to the UC1825 controller and consists of an oscillator, precision voltage reference, error amplifier and two totem pole high current output stages, which are specifically optimized for high performance at high frequency. These cells can be connected with other available circuitry on the chip to form a complete SMPS controller. The "uncommitted" sections of the array can be configured into comparators, logic, and other functions, to implement a complete control. In addition, closely matched resistors are available to precisely control thresholds and gain settings on the chip.

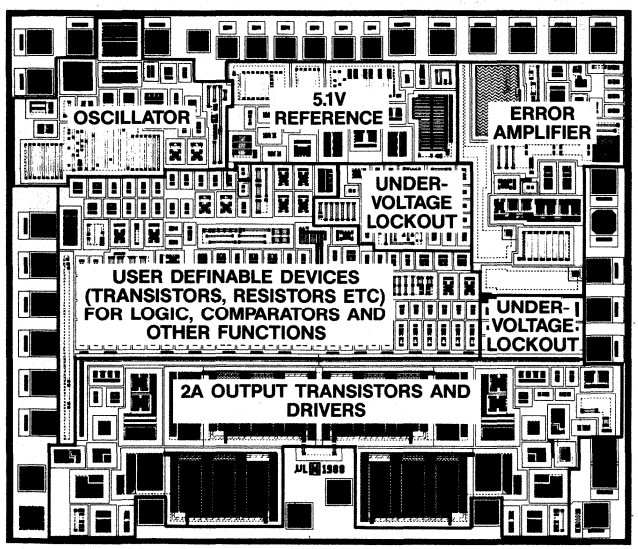
The FB3480 array is used to make several state of the art standard products, including the ML4825 and ML4809. Cells from these and future Micro Linear FB3480 based standard products can be made available for customer designs.

FEATURES

- Practical operation to Switching Speeds above 1 MHz
- Precision Bandgap Reference ..... ±1%
- 2 A peak push-pull output stages for high speed drive of power MOSFETs
- Fast comparator to output response time .. <50ns
- Available in DIP or PLCC
- Mil-Temp available
- Additional user-definable logic, comparators and other circuitry available on chip

6

BLOCK DIAGRAM



CIRCUIT CAPACITY

The FB3480 consists of pre-configured optimized functional cells which are commonly found in SMPS controllers. In addition the FB3480 has additional transistors and resistors available for user configuration. The Array topology is optimized to implement a full featured high performance SMPS controller utilizing both the "Dedicated Resources" (oscillator, error amp, reference and power output) and additional fully configurable resistors and transistors.

The FB3480 can be configured to fully implement the ML4825 improved pin compatible replacement for the popular UC1825 controller and still have resources on chip for additional functions.

The table below lists uncommitted resources which are still available after implementing the following controller designs completely.

The FB3480's unused elements can be configured into:

Component	ML4825		ML4823		FB3480
	Used	Unused	Used	Unused	Total
NPN Current Sink	20	9	15	14	29
NPN Transistors	27	29	21	35	56
Dual Emitter NPN	6	8	3	11	14
NPN Follower (1 Emitter)	0	8	0	8	8
NPN Follower (2 Emitter)	10	7	7	10	17
Low Voltage 4 Collector PNP	3	8	3	8	11
High Voltage 4 Collector PNP	2	2	2	2	4
PNP Current Source	3	3	2	4	6
Zeners (NPN Diodes)	2	4	0	6	6
2 A NPN Transistors	4	0	2	2	4
Implanted Resistors	37	18	29	26	55
Base Resistor	3	5	3	5	8
Bondable Pads	16	12	16	12	28

DEDICATED RESOURCES

The table below lists the dedicated functions which are available on the FB3480. Each of these blocks is described in more detail beginning on page 4.

REF #	Description	Count
OSC1	1.5 MHz. F_{MAX} R-C Oscillator	1
REF1	5.1 V Precision Reference	1
PWR1	2 A Peak Push-Pull Totem Pole Output Buffer	2
EA1	5.5 MHz Bandwidth, 12V/μS Slew Rate Error Amp	1
UV1	Under-Voltage Lockout Circuit	1

UNCOMMITTED RESOURCES

The FB3480 includes a large number of transistors and resistors which are used to make up the circuit functions or "cells" which are available for design and listed beginning on page 8. The table below lists how many of these components are available and their typical performance characteristics.

TYPICAL PERFORMANCE CHARACTERISTICS OF UNCOMMITTED RESOURCES

Transistors

Ref #	Description	β @ 100 μA	β @ 1 mA	$I_{(\beta/2)}$ (Note 1)	V_{CEO}	V_{CBO}	F_T (MHz)	Count
TN1	NPN Low Voltage		100	20	12	25	450	55
TN3	NPN Power (100 mA)		100	60	45	55	450	1
TN4	Dual Emitter NPN		100	20	45	55	450	10
TN5	NPN Emitter Follower		100	20	12	25	450	8
TN6	NPN Dual Emitter Follower		100	20	12	25	450	17
TN7	NPN Current Sinks		100	20	12	25	450	29
TP1	Lateral Low V PNP	30		1	15	25	4	8
TP2	Lateral High V PNP	30		1	45	45	4	3
TP3	Substrate PNP	60		1	45	45	20	1

Diodes

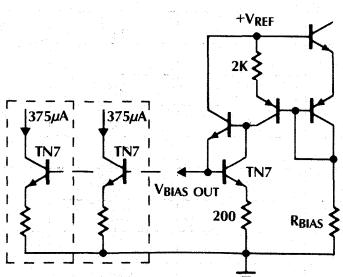
Ref #	Description	$V_{REVERSE}$	$I_{FORWARD}$ (mA)	Count
DN1	NPN Diode	6.8	2	6

Resistors

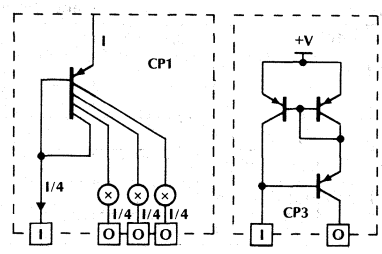
Ref #	Type	Value	Tolerance	Ratio Matching	Count
RB1	Base	2KΩ	20%	0.5%	6
RI1	Implant	2KΩ	20%	1.0%	29
RI2	Implant	8KΩ	20%	1.0%	8
R13	Implant	30KΩ	20%	3.0%	5

Note 1: This column indicates the useful current handling capability of the transistor and is defined as the current at which the β is down to 1/2 of its nominal (100μA for PNP and 1mA for NPN) value.

Transistors TP1, TP2, and TP3, are constructed with four separate collectors and can be used as current sources as shown below. TN7 is a special NPN transistor which includes a 200Ω resistor cell and is intended to be used as a current sink in conjunction with the on chip bias reference generator.



Current Sources CP1 and CP3 are examples of current sources which can be constructed with the PNP transistors. CP1 is a basic biasing current source, where the 3 output currents are equal to the input current. CP3 has an additional circuit to cancel the base current error and is more accurate and linear.



ABSOLUTE MAXIMUM RATINGS

Supply Voltage 36V
Output Current, Source or Sink (Power Outputs)
DC 0.5A
Pulse (0.5 μS) 2.0A
Input Voltage (logic, comparators etc.) ..... –0.3V to 6V
Error Amplifier Output Current 5mA
Oscillator Charging Current ..... –5mA
Junction Temperature ..... 150°C
Storage Temperature Range ..... –65°C to +150°C
Lead Temperature (Soldering 10 sec.) ..... +260°C

OPERATING TEMPERATURE RANGE

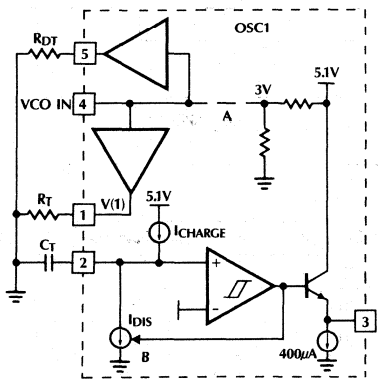
Plastic Packages (PCC or DIP) ..... –40°C to +85°C
Ceramic Packages ..... –55°C to +125°C

Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

FB3480 CORE CELL DESCRIPTIONS

Oscillator

The FB3480 oscillator charges the external capacitor (C_T) with a current (I_{SET}) equal to V(1)/R_T. When the capacitor voltage reaches the upper threshold, the comparator changes state and the capacitor discharges to the lower threshold. While the capacitor is discharging, a high pulse is provided on (3).



Several configurations are available for the FB3480 oscillator:

1. Basic ML4825 oscillator: A fixed discharge time is provided by saturating a transistor for I_{DIS}. This discharge current is approximately 10 mA. Charge time is fixed since pin 4 is set to 3V by the internal resistor divider at node A.
2. Controlled Discharge: I_{DIS} is equal to:
$$\frac{16 \times V(\text{pin } 5)}{R_{DT}}$$
3. Voltage Controlled Oscillator. The connection at node A is open and pin 4 is brought out. The control range is from 1V to 5.5V. The voltage at pin 4 sets the charge and discharge currents (if option 2 above is implemented) thereby controlling the frequency of the oscillator.

ELECTRICAL CHARACTERISTICS (unless otherwise noted, these specifications apply for R_T = 3.65KΩ, C_T = 1000pF, –55°C < T_J < 150°C, V_{CC} = 15V) fixed deadtime, A connected.

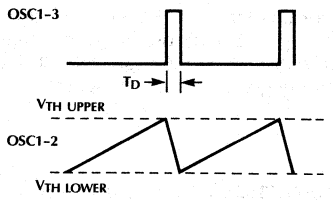
Parameter	Conditions	DESIGN LIMITS			Units
		Min	Typ	Max	
OSC1 and OSC2 Oscillator					
Initial Accuracy	T_J = 25°C	360	400	440	KHz
Voltage Stability	10V < V_{CC} < 30V		0.2	2	%
Temperature Stability	–55°C < T_J < 150°C			5	%
Total Variation	line, temp.	340		460	KHz
Clock out High		3.9	4.5		V
Clock out Low			2.3	2.9	V
Ramp Peak		2.6	2.8	3.0	V
Ramp Valley		0.7	1.0	1.25	V
Ramp Valley to Peak		1.6	1.8	2.0	V
Capacitor Discharge Current		10			mA
Current Consumption			3.2		mA
Typical VCO Control Range	1.5 < OSC2-4 < 5V	75%		175%	f_{NOM}

Oscillator (Continued)

The Oscillator period can be described by the following relationship:

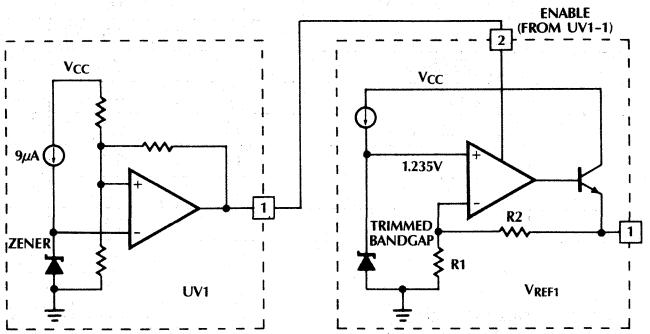
$T_{OSC} = T_{ramp} + T_{deadtime}$

where: $T_{ramp} = C (V_{upper} - V_{lower})/I_{charge}$
and: $T_{deadtime} = C (V_{upper} - V_{lower})/I_{dis}$



Voltage Reference and Undervoltage Lockout

The FB3480 voltage reference is a buffered trimmed bandgap design with excellent thermal characteristics. The undervoltage lockout circuit (UV1) monitors V_{CC} and compares it to a zener voltage with hysteresis in the comparator. When the supply is sufficiently high to allow operation of the controller, pin 1 of UV1 goes true, enabling V_{REF1}, which runs the bias circuitry for all the logic. In this way, when the V_{CC} is under voltage, the array goes into a low current consumption mode. The thresholds for UV1 can be selected.

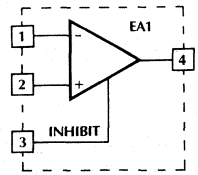


ELECTRICAL CHARACTERISTICS (unless otherwise noted, V_{CC} = 15V, -55°C < T_J < 150°C)

Parameter	Conditions	DESIGN LIMITS			Units
		Min	Typ	Max	
VR1					
Output Voltage	T_J = 25°C, I_O = 1mA	5.05	5.10	5.15	V
Line Regulation	10V < V_{CC} < 30V		2	20	mV
Load Regulation	1mA < I_O < 10mA		5	20	mV
Temperature Stability	-55°C < T_J < 150°C		.2	.4	mV/°C
Total Output Variation	line, temp.	5.0		5.20	V
Output Noise Voltage	10Hz to 10KHz		50		μV
Long Term Stability	T_J = 125°C, 1000 Hrs		5	25	mV
Short Circuit Current	V_{REF} = 0V	-15	-50	-100	mA
Current Consumption			.7		mA
UV1					
Start Threshold		8.8	9.2	9.6	V
UVOL Hysteresis		.4	.8	1.2	V

Error Amplifier

The FB3480 error amplifier is a 5.5 MHz bandwidth, 12V/μS slew rate op-amp with provision for limiting the positive output voltage swing (Output Inhibit line) for ease in implementing the soft start function.

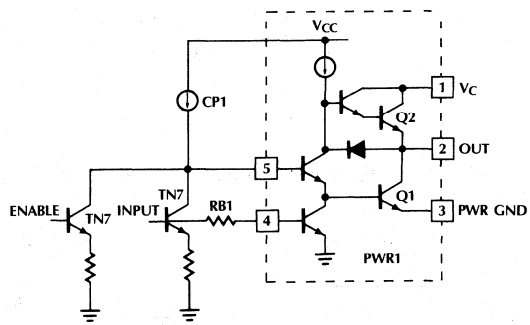


ELECTRICAL CHARACTERISTICS (unless otherwise noted, V_{CC} = 15V, -55°C < T_J < 150°C)

Parameter	Conditions	DESIGN LIMITS Min	Typ	Max	Units
EA1					
Input Offset Voltage				10	mV
Input Bias Current			.6	3	μA
Input Offset Current			.1	1	μA
Open Loop Gain	1 < V_O < 4V	60	96		dB
CMRR	1.5 < V_{CM} < 5.5V	75	95		dB
PSRR	10 < V_{CC} < 30V	85	110		dB
Output Sink Current	V_{FA1-1} = 1V	1	2.5		mA
Output Source Current	V_{EA1-1} = 4V	-.5	-1.3		mA
Output High Voltage	I_{EA1-1} = -0.5mA	4.0	4.7	5.0	V
Output Low Voltage	I_{EA1-1} = 1mA	0	0.5	1.0	V
Unity Gain Bandwidth		3	5.5		MHz
Slew Rate		6	12		V/μS
Current Consumption	I_{EA1-1} = 0		1.5		mA

Output Driver Stage

The FB3480 Output Driver is a 2A peak output high speed totem pole circuit designed to quickly switch the gates of capacitive loads, such as power MOSFET transistors. The external translator to the left of the PWR1 cell is shown as an example of how to interface from logic signals to the output stage and is made up of uncommitted resources available on the IC.



ELECTRICAL CHARACTERISTICS (unless otherwise noted, V_{CC} = 15V, -55°C < T_J < 150°C)

Parameter	Conditions	DESIGN LIMITS Min	Typ	Max	Units
PWR1					
Output Low Level (V_{OL})	I_{OUT} = 20mA I_{OUT} = 200mA		0.25 1.2	0.40 2.2	V V
Output High Level (V_{OH})	I_{OUT} = -20mA I_{OUT} = -200mA	13.0 12.0	13.5 13.0		V V
Collector Leakage	V_C = 30V		100	500	μA
Rise/Fall Time	C_L = 1000pF		30	60	nS
Current Consumption	I_{OUT} = 0		7.3		mA

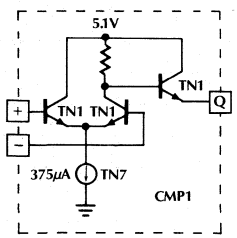
UNCOMMITTED RESOURCE CELLS

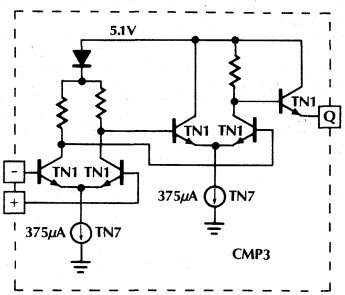
The functions listed below are pre-simulated "cells" which are available for use. These "cells' are made up from the uncommitted resources described on page 3.

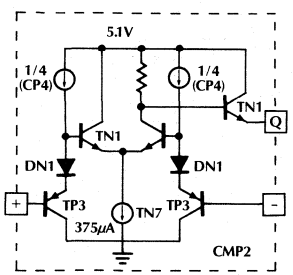
Comparators

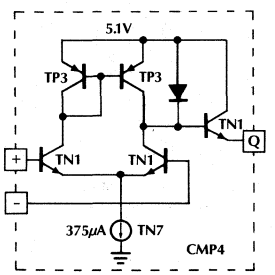
ELECTRICAL CHARACTERISTICS (unless otherwise noted, V_{CC} = 15V, -55°C < T_J < 150°C)

Parameter	Conditions	DESIGN LIMITS			Units
		Min	Typ	Max	
CMP1 — Simple NPN Comparator					
Output Low Level	I_{OUT} = 1mA		3.6	4.1	V
Output High Level	I_{OUT} = -1mA		4.35	4.7	V
Input Offset Voltage			10		mV
Input Common Mode Range		1		4.1	V
T_{PHL}			20		nS
T_{PLH}			20		nS
Voltage Gain			28		V/V
Quiescent Current Consumption			1		mA
CMP2 — Simple Ground Sensing PNP Input Comparator					
Output Low Level	I_{OUT} = 1mA		3.6	4.1	V
Output High Level	I_{OUT} = -1mA		4.35	4.7	V
Input Offset Voltage			20		mV
Input Common Mode Range		GND		3.1	V
T_{PHL}			25		nS
T_{PLH}			25		nS
Voltage Gain			28		V/V
Quiescent Current Consumption			1		mA





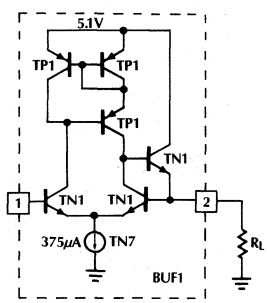


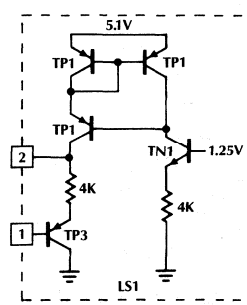


Comparators (Continued)

ELECTRICAL CHARACTERISTICS (unless otherwise noted, V_{CC} = 15V, –55°C < T_J < 150°C)

Parameter	Conditions	DESIGN LIMITS			Units
		Min	Typ	Max	
CMP3 — High Gain NPN Comparator					
Output Low Level	I_{OUT} = 1mA		3.6	4.1	V
Output High Level	I_{OUT} = –1mA		4.35	4.7	V
Input Offset Voltage			20		mV
Input Common Mode Range		1		4.1	V
T_{PHL}			35		nS
T_{PLH}			35		nS
Voltage Gain			700		V/V
Quiescent Current Consumption			1		mA
CMP4 — Very High Gain NPN Comparator					
Output Low Level	I_{OUT} = 1mA		3.6	4.1	V
Output High Level	I_{OUT} = –1mA		4.35	4.7	V
Input Offset Voltage			10		mV
Input Common Mode Range		1		4.1	V
T_{PHL}			500		nS
T_{PLH}			500		nS
Voltage Gain			15,000		V/V
Quiescent Current Consumption			1		mA
BUF1 — Voltage Follower (Buffer)					
Input Bias Current				4	µA
Output Voltage Range	I_{OUT} < 1mA	0		4.1	V
Offset Voltage				10	mV
Input Common Mode Range		1		4.1	V
Open Loop Voltage Gain			1000		V/V
Slew Rate	C_L < 1pF	2			V/µS
Quiescent Current Consumption			.375		mA
LS1 — 1.25V Level Shift					
Input Bias Current				12	µA
V_{OUT} – V_{IN}		1.1		1.4	V



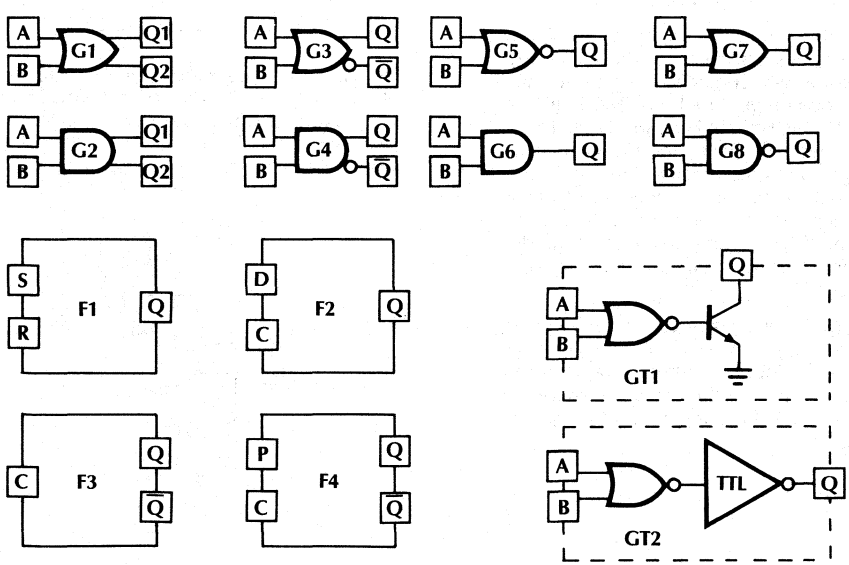


Internal Logic Macro Functions

The FB3480 logic section is a pre-characterized library made up of high speed, high noise immunity Emitter Function Logic (EFL) and Emitter Coupled Logic (ECL) functions. This logic family uses uncommitted low voltage transistors and resistors which are available to be metallized (described on page 3) to make up the logic functions below.

This family features the ability to "wire or" the outputs as well as having a very flexible structure and fast propogation delay times. For more information on designing with EFL logic, please refer to the Application Hints on page 12.

Ref #	Description	Component Utilization							Design Limits	
		TN1	TN4	TN5	TN6	TN7	DN1	RB1	t_{PD} (nS)	I_{CC} (mA)
G1	2-Input 2-Output OR	3			1	1		1	7	.375
G2	2-Input 2-Output AND		1		1	2	1	1	5	.7
G3	2-Input Complementary Output OR/NOR	2		2		1		2	7	.375
G4	2-Input Complementary Output AND/NAND	4		2		2	2	2	7	.7
G5	2-Input NOR	3		1		1		1	7	.375
G6	2-Input AND		1	1		2	1	1	5	.7
G7	2-Input OR	3		1		1		1	7	.375
G8	2-Input NAND	4		1		2	1	1	7	.7
GT1	EFL to TTL 2-Input OR Open Collector	4				1	2	2	10	.7
GT2	EFL to TTL 2-Input OR Totem Pole	5				2	3	5	13	1.125
F1	R-S Flip Flop	2	1		1	1		1	8	.375
F2	Positive Edge Triggered D Flip Flop	4	2		2	3		1	10	1.125
F3	Positive Edge Triggered T Flip Flop	6	5			5		3	12	1.875
F4	T Flip Flop with Preset	8	1			6		4	12	2.26



APPLICATIONS INFORMATION

DESIGNING AND SPECIFYING A CONTROLLER

The FB3480's core cell architecture is designed to simplify the task of designing a PWM controller for unique needs or specific tasks. Micro Linear will design the IC for a nominal initial lot charge providing that the design uses the cells described in this datasheet. A specification for a customized FB3480 controller requires the following elements:

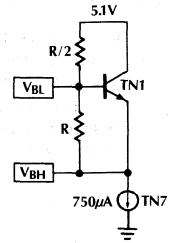
1. A block diagram describing the interconnection of the cells. This could also take the form of a modified block diagram from any of Micro Linear's standard products (such as the ML4809 or ML4825). The block diagram should be drawn in terms of the cells described in this datasheet.
2. Packaging requirements. The FB3480 has 28 bondable pads. Industrial temperature range units can be packaged in 28 pin Plastic Leaded Chip Carrier (PLCC) Plastic DIP packages from 14 to 28 pins. Military temperature range units can be packaged in Ceramic DIP packages from 14 to 28 pins.
3. Test specifications.
4. Operating Temperature Range requirements.

An accurate indication of circuit performance can be obtained by prototyping with one of Micro Linear's standard products built from the FB3480 (such as the ML4825 or ML4809) and using "off the shell" comparators and logic of similar performance to that specified in the FB3480 datasheet.

DESIGNING WITH EFL LOGIC

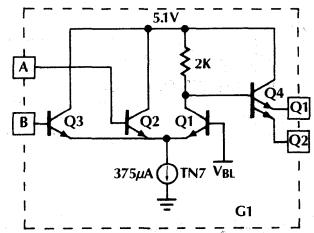
The FB3480's logic section is a collection of high frequency NPN transistors, current sink transistors, resistors and diodes which can be configured into a variety of high speed logic functions. The logic family used in the FB3480 is Emitter Function Logic (or EFL) which features speed, flexibility and simplicity. Since most of the logic is interconnected "on chip", buffering to drive PC board layout capacitances is not needed, further minimizing the number of transistors which are used to accommplish the necessary logic. In addition, the output structure lends itself to accomplishing "wired-or" functions.

The family's output voltage swings are between (V_{REF} – V_{BE}), logic 1, and (V_{REF} – $2V_{BE}$), logic 0, where V_{REF} is set to 5.1V internally. Input thresholds are called V_{BH} and V_{BL} and are set by the threshold generator shown below to (V_{REF} – $V_{BE}/2$) for a logic 1 and (V_{REF} – 3 * $V_{BE}/2$) for a logic 0.

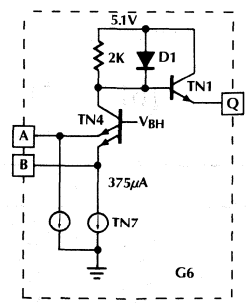


LOGIC BIAS THRESHOLD GENERATOR

In the example below, G1 is a full OR gate. When either input A or input B exceeds V_{BL} (1.5 * V_{BE} down from the supply), Q1 is cut off, putting the base of Q4 at V_{REF}, which puts V_{REF} – V_{BE} on the output at the emitters of Q4. When both A and B are below V_{BL}, Q1 conducts forcing the voltage on its collector to drop to (V_{REF} – V_{BE}). This occurs since TN7 is set so that its current (375 μA) will cause a V_{BE} drop to occur in a 2KΩ resistor. The output emitters of Q4 will be at V_{BASE} – V_{BE}, or (V_{REF} – $2V_{BE}$).



G6 is an AND gate using a dual emitter input. When either emitter is allowed to go below V_{BL} (V_{BH} – V_{BE}), TN1 conducts, which causes the output to go low. If both inputs are above V_{BL}, TN4's base sits at V_{REF}, which makes TN4's output (V_{REF} – V_{BE}).



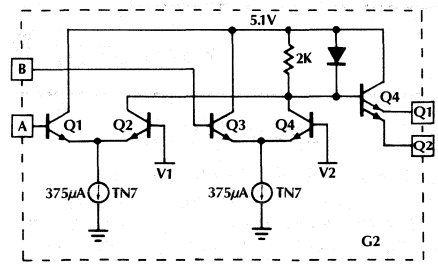
APPLICATIONS INFORMATION (Continued)

When multiple outputs are tied together, they function like an OR gate. Only one of the output emitters need to go "high" for the line to become true. This assumes that the node is loaded with one current sink.

Comparator functions with combinational logic can also be easily constructed using this family. Note that G1 has a full differential input stage. By applying a voltage (V1) on the base of Q1, the output will be true when A or B exceed V1. A similar example using an AND function is shown below.

With the FB3480, a power supply designer can select his own unique controller topology and features without the need for external components. This flexibility allows compact PC board layout, minimizing interference from induced RFI/EMI, and enhancing high frequency performance.

Inverting or complementary outputs can be obtained easily from most simple logic functions simply by moving the load resistor and output transistor base connection to the opposite collector.



6

General Purpose PWM Controller Array

GENERAL DESCRIPTION

The FB3490 Power Supply Controller Array is optimized for use in Switch Mode Power Supply designs at frequencies up to 750 KHz. These "core cells" (Oscillator, Reference, Output Drivers) are optimized for high performance while retaining maximum flexibility. In addition, this array contains cells (or tiles) which can be used for logic, amplifiers, comparators and other special functions.

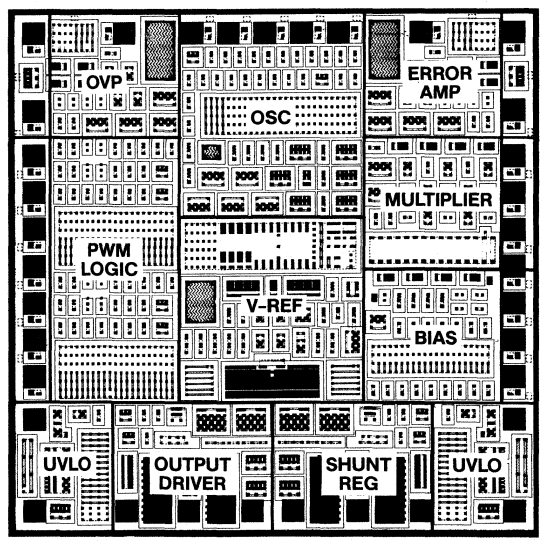
With the FB3490, a power supply designer can select a unique controller topology and feature set without the need for external components. Design and layout of a unique controller is simplified through the use of many pre-defined and pre-simulated "soft macros" which can be made available for customer designs.

This array is similar in performance to the UC1846 and was used to implement the ML4812 Power Factor Controller. Cells from these and future Micro Linear FB3490 based standard products can be made available for customer designs.

FEATURES

- Practical Operation at Switching Frequencies to 750 KHz
- Dual High Current (1A peak) Totem Pole Outputs
- ±0.5% Trimmed Bandgap Reference
- Multiple Error Amp systems possible
- Extensive library of "soft macro" building block functions available for user design
- 40V bipolar dual layer metal process

BLOCK DIAGRAM



Micro Linear

FB3491

Resonant Mode Controller Array

GENERAL DESCRIPTION

The FB3491 is an application focused tile array intended for resonant mode power supply controller applications. This array, built on our 40 volt technology, consists of customized and general purpose groupings of components to implement the various power supply control circuit blocks. Certain areas, such as the power output section and the oscillator, are customized to obtain a higher level of performance for these critical circuit functions.

The array has four high current (2A peak) output transistors to implement two high current, low cross conduction, totem pole type output drivers. The high current capability allows the quick charge and discharge of the gate capacitance of external power MOSFET devices.

High speed emitter function logic circuits can be implemented to achieve fast current sense circuits. A propagation delay of less than 50ns from current sense to output shutdown can be achieved. An oscillator that is capable of operating up to 3MHz and a precision reference with an accuracy of ±1% and a temperature stability of 50 ppm/°C are examples of the level of performance that can be achieved.

Standard products built on this tile array can be easily modified to create a semi-standard version optimized for a specific customers application.

FEATURES

- Array Optimized for Resonant Mode Power Supply Control Circuits
- High Current (2A) Output Transistors for Fast Output Drivers
- Can Implement all the Circuit Blocks for a High Performance Resonant Mode Controller
- 6 Analog Circuit Blocks and 40 Gate Complexity
- 40 Volt, 400 MHz Technology

ARRAY SUMMARY

NPN Transistors	315
PNP Transistors	126
Power NPN Transistors	4
Schottky Transistors	33
Total Diffused Resistance	570K
Total Implant Resistance	2600K
Total MOS Capacitance	34pF
Total Components	1248
Bond Pads	30
Die Size (mils)	140 × 181

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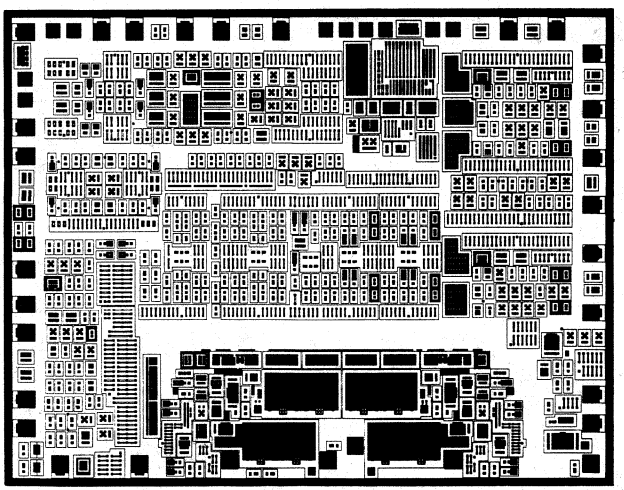


FB3491 — Resonant Mode Controller Array

Micro Linear

FB3492

Phase Modulation Controller Array

GENERAL DESCRIPTION

The FB3492 is an application focused tile array intended for phase modulated power supply controller applications. This array, built on our 40 volt technology, consists of customized and general purpose groupings of components to implement the various power supply control circuit blocks. Certain areas, such as the power output section, the oscillator, and the voltage reference are customized to obtain a higher level of performance for these critical circuit functions.

The array has eight high current (2A peak) output transistors to implement four high current, low cross conduction, totem pole type output drivers. The high current capability allows the quick charge and discharge of the gate capacitance of external power MOSFET devices.

High speed emitter function logic circuits can be implemented to achieve fast current sense circuits. A propagation delay of less than 50ns from current sense to output shutdown can be achieved. An oscillator that is capable of operating up to 3MHz and a precision reference with an accuracy of ±1% and a temperature stability of 50 ppm/°C are examples of the level of performance that can be achieved.

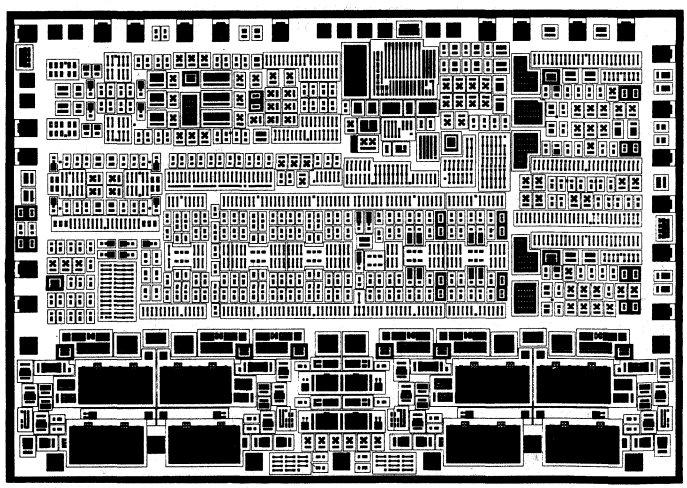
Standard products built on this tile array can be easily modified to create a semi-standard version optimized for a specific customers application.

FEATURES

- Array Optimized for Phase Modulated Power Supply Control Circuits
- High Current (2A) Output Transistors for Fast Output Drivers
- Can Implement all the Circuit Blocks for a High Performance Phase Modulation Controller
- 9 Analog Circuit Blocks and 60 Gate Complexity
- 40 Volt, 400 MHz Technology

ARRAY SUMMARY

NPN Transistors	323
PNP Transistors	131
Power NPN Transistors	8
Schottky Transistors	39
Total Diffused Resistance	580K
Total Implant Resistance	2500K
Total MOS Capacitance	34pF
Total Components	1290
Bond Pads	29
Die Size (mils)	140 × 201



FB3492 — Phase Modulation Controller Array

USICs and Semi-Standard

Section 7

Semi-Standard Overview

SEMI-STANDARD ANALOG ICs

Custom ICs are often required to achieve a proprietary edge in high performance analog systems. Unfortunately, the high risk and long development cycles are often prohibitive, forcing the system designer into specifying much less optimum, and less competitive off-the-shelf standard ICs. Semi-standard analog ICs provide a cost effective alternative that combines the competitive advantage of a custom circuit with the low risk of a standard product.

The level of technical risk and the time-to-market of this approach is significantly reduced over a full custom or semi-custom IC development. The risk is lower because only an incremental change is made to an already proven device. The time-to-market advantage comes from a combination of a much shorter development time for the semi-standard and the added benefit of being able debug the system level issues by using the standard product.

MODIFIED STANDARD PRODUCTS

Semi-standard analog ICs are created by modifying existing standard products. Modifications can span all the way from a functional circuit change to a simple variation in the part marking. Examples of the range of possible semi-standard modifications are as follows:

Circuit Modifications

Modify Functional Blocks
Change Input/Output Levels
Adjust Gain/Thresholds
Shift Logic Levels (ECL, TTL, CMOS)
Move Current Limit Point
Reduce Bandwidth
Improve Power Consumption
Tweak Charge/Discharge Currents
Adjust Voltage Reference

Other Semi-Standard Modifications

Change Part Marking
Extend the Temperature Range
Add Electrical Tests
Modify the Pinout
Change the Package

Circuit modifications are easily made to Micro Linear's standard products because they are built using our proprietary Tile Array technology. Tile Arrays are collections of active and passive components arranged in a pattern on an integrated circuit chip. Each standard product is developed, by designing two layers of metal interconnect to implement the specific circuit functions required for the product.

Micro Linear produces standard products using bipolar tile arrays and CMOS standard cell technologies. The Tile Array technology allows the widest range of functional and performance modification possibilities. The CMOS standard cell technology, while not flexible for functional modifications, can still accommodate performance, specification, or physical changes. A summary of the types of modifications possible for each group of standard products is shown below in Table A.

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	Technology	Functional Modifications	Performance Modifications	Specification or Packaging Changes
Power and Motion Control				
High Frequency PWM Control	BT	Yes	Yes	Yes
Resonant Control	BT	Yes	Yes	Yes
Sensorless Motor Control	BT	Yes	Yes	Yes
Data Communications Transceivers				
Fiber Optic LED Drivers	BT	Yes	Yes	Yes
Fiber Optic Quantizer	BT	Yes	Yes	Yes
10Base-T Trans: AUI/MPR	BT	Yes	Yes	Yes
Analog Telecom/NCTE				
Signal Equalizers	CS	No	Yes	Yes
Gain/Attenuators	CS	No	Yes	Yes
Sine Wave Generators	CS	No	Yes	Yes
Tone Detectors	CS	No	Yes	Yes
Hard Disk Drives				
Pulse Detectors	BT	Yes	Yes	Yes
Data Separators	BT	Yes	Yes	Yes
Dedicated Servo Control	BT	Yes	Yes	Yes
Voice Coil Driver	BT	Yes	Yes	Yes
Data Conversion & Filtering				
8, 10 & 12 A/D Converters	CS	No	Limited	Yes
8-Bit D/A Converters	CS	No	Limited	Yes
Switched Cap Filter	CS	No	Limited	Yes

(Code: BT = Bipolar Tile Arrays; CS = CMOS Standard Cells)

Table A. Semi-Standard Reference Guide

SEMI-STANDARD DEVELOPMENT

A semi-standard circuit can be easily and quickly developed from a standard product. The customer need only define the functional, performance, and physical nature of the modifications necessary to the Micro Linear standard product to meet his system requirements. Micro Linear then will perform the circuit design and complete the performance verification simulations. At this point a design review is held with the customer to make sure all aspects of the development are in accordance with the customers requirements. Micro Linear then proceeds with making the necessary layout changes, manufacturing, testing and delivering the prototypes. This complete development flow is illustrated in figure B.

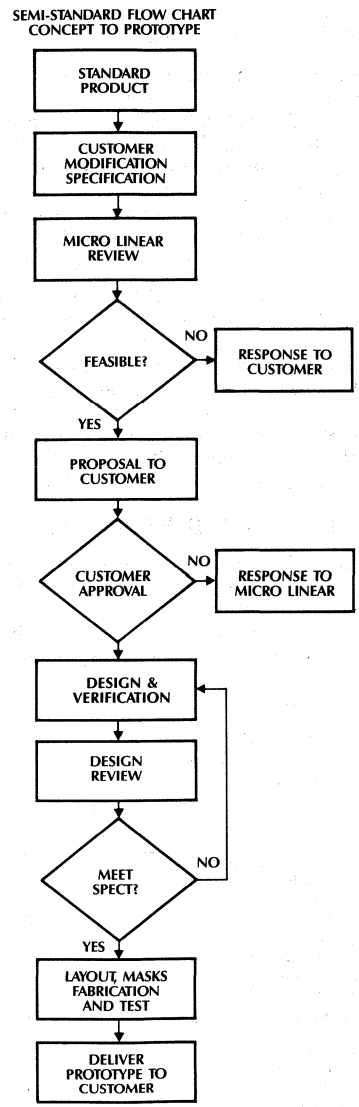


Figure B.

Analog and Mixed Analog/Digital Tile Arrays

Micro Linear's Tile Arrays can implement a wide range of complex circuit and performance applications. They are comprised of uncommitted active and passive components arranged in an organized tile pattern on an integrated circuit chip to provide maximum flexibility and ease of interconnection. After a circuit is designed and simulated, several metal patterns are created to connect the components and produce a customized analog USIC. USIC is an acronym for **U**ser **S**pecific **I**ntegrated **C**ircuit. USICs are ICs that are specific to a customer or user and are commonly referred to as ASICs.

Mini Tile Architecture

The pattern of the components on each array is based on Micro Linear's proprietary mini tile approach. Each mini tile is comprised of a group of components selected and arranged to implement circuit functions. For example, a T1 mini tile has three NPNs, one PNP, and various resistors. This is the most common mini-tile and has the highest frequency of placement on the arrays. A T1 mini tile can implement many of the basic integrated circuit functions such as, differential amplifiers, current mirrors and level shifters. A T5 mini-tile has twelve precision resistors and six small NPN transistors. The precision resistors make this mini tile ideal as the core part of a DAC. A T2 mini tile has two matched NPNs, medium current NPN, PNP output transistors, and most importantly a MOS capacitor. A T2 mini tile is used, with a few T1s, to implement an operation amplifier with the MOS capacitor used for on-chip frequency compensation.

Other mini tiles are optimized for specific aspects of circuit performance. For example, T13 mini tiles are for high frequency design, T16 mini tiles contain a power schottky transistor for non-saturating output stages, and T14 and T15 mini tiles have a 2 amp NPN and a medium current PNP respectively for implementing a high current complementary output stage. Please refer to the mini tile description in this section for a complete listing and explanation of the various mini tiles.

The mini tile architecture is such that is provides an optimum balance between flexibility and low cost. It has the flexibility required to implement a wide range of circuit functions and achieves low cost by an efficient use of silicon. The cost of a circuit utilizing this mini tile architecture is competitive with cost of an equivalent discrete implementation.

Custom Circuit Alternatives

The architecture of most analog arrays are designed to achieve maximum flexibility with high performance. They typically consist of a collection of components arranged in a symmetrical, regular pattern. These general purpose arrays attempt to meet the widest range of circuit function requirements. Micro Linear's FB3610, FB3620, FB3630 are examples of this type of array.

A standard cell, full custom integrated circuit is at the other end of the custom IC spectrum from general purpose arrays. This approach uses previously designed circuit functions and puts them together like a puzzle. The cells can be optimized for the specific application and performance requirements. This approach also carries with it the disadvantages of significantly longer development times and higher costs compared to the array approach. These longer times and costs become extremely painful when considering that most custom ICs require several iterations before production ready devices are achieved.

The increasing performance requirements of potential custom IC applications is slowly pushing the analog arrays to their performance limit. Also, the strong need for shorter development times and lower risk eliminates standard cell as an option. An ideal solution to all of these requirements is an application focused array approach that combines the best of both array and full custom solutions.

Application Focused Arrays

These application focused arrays are optimized for specific application and/or market areas. They consist of custom designed tiles along with general purpose tiles. The custom tiles are optimized for maximum performance for those circuit functions where the performance is critical to the system performance. These custom tiles can then be programmed with two layers of metal to select the functionality required for the specific application. The general purpose mini tiles are provided for added flexibility to implement the less critical circuit blocks.

Since this is an array approach, it has the advantages of short development times and low costs. Because the critical circuit functions are custom, maximum performance is achieved. Because of this, application focused arrays offer an attractive, low risk approach for custom integrated circuits.

Micro Linear's FB3480 Power Supply Controller array is an excellent example of an application focused array. Also the FB3490 General Purpose PWM Controller array, the FB3491 Resonant Mode Controller array and the FB3492 Phase Modulation Controller array are all focused arrays intended for the various aspects of power supply application markets. These arrays are described in further detail in the power supply section of this book.

Our FB3651 LAN Transceiver array is an application focused array for local area network Transceiver applications. This array can implement all of the analog and timing functions for a cable line driver/receiver. Please refer to the Data Communications section for more information on this array.

Another example of application orientation of analog arrays is the FB3623 High Power Array described herein. The FB3623 is divided into two separate sections, one custom designed specifically for high power output drivers and the other section with general purpose mini tiles for maximum circuit flexibility.

Tile Array Families

Two different families of arrays are available depending on the voltage and speed requirements needed for the circuit to be integrated. The FB3600 is a 12-volt, high speed tile array family and the FB3400 is a 40-volt, moderate speed tile array family.

FB3600 Tile Arrays

The FB3600 family of arrays are built using a 12-volt, 1 GHz technology. The arrays are configured with mini-tiles. Each tile is a collection of specific components such as NPN or PNP transistors, resistors, capacitors, etc. The mini tile approach to array design results in an optimum use of silicon such that very cost-effective solutions can be realized.

Array Summary

FB3605 — Small High Frequency
FB3610 — Small General Purpose
FB3620 — Medium General Purpose
FB3621 — Medium High Frequency
FB3622 — Medium with Power Schottky
FB3623 — Medium with High Power NPNs
FB3630 — Large General Purpose
FB3631 — Large Mixed Analog/Digital
FB3635 — Large Mixed Analog/Digital

FB3400 Tile Arrays

The FB3400 family of arrays are built using a 40-volt, 300 MHz technology. A mini tile approach similar to the FB3600 family is used to achieve the same flexibility and efficient use of silicon. Circuits common to automotive and military applications that use ±15 volt power can be integrated on the FB3400 arrays.

Array Summary

FB3410 — Small General Purpoe
FB3420 — Medium General Purpose
FB3430 — Large General Purpose

High Performance and High Complexity Applications

Micro Linear's FB3600 family of arrays are ideal for many applications in areas such as communications, signal processing, telecom, industrial control, computer peripheral, and navigation as examples. High frequency circuits like a 90 MHz voltage controlled oscillator or a 100 MHz cascode amplifier can be implemented. Output drive capability up to 2 amps (4 × 0.5A), precision circuits with 0.5% accuracies and offset voltages as low as 1 mV (trimmed) are possible on the tile arrays. Circuit complexities as high as 24 analog circuit blocks or 8 op amps and 130 gates of ECL logic all can be integrated on a single tile array.

This high level of performance has allowed USICs to be used in a very diverse applications. Any system that requires small board space, low weight, low cost and high performance is a candidate for integration into a tile array. Some examples of circuits/systems that have been successfully integrated on Micro Linear tile arrays are:

- Laser diode bias control circuit for a fiber optic communication system
- Optical receiver for a laser gyroscope
- Fiber optic quantizer for optical transmission systems (see ML4621)
- PWM control circuit for DC motors
- Starlan transceiver for local area networks
- Twisted pair transceiver for serial data communications
- VCO/data detect/signal processing circuits for a high density tape drive
- Complete signal processing function for a hearing aid
- Dual preamp for tape drive storage system
- Aircraft power monitor control circuit
- Chip set that implements the complete servo control loop for hard disk systems (see ML4401, ML4402, ML4403, ML4404)
- Pulse peak detector for hard disk drive (see ML8464C)

Additional application information is available in the application notes section of this catalog.

Packaging

Many types of packaging are available for the tile arrays. Devices can be assembled, tested and produced in volume in plastic and ceramic dual-in-line (DIP), plastic and ceramic chip carriers (PLCC, LCC) as well as new surface mount technologies like small outline packages (SOIC). Tape and reel format shipments are available for automated assembly requirements. Please refer to the USIC package selection guide in this section.

Design Methodology

Micro Linear has extensive experience designing and producing state-of-the-art analog and mixed analog digital USICs. The key aspects of our successful methodology include: computer simulations with very accurate component models; in depth design reviews with the customer; expert mask layout and computer checking; and complete packaging and testing capability.

Computer Simulations

The expected performance of the finished IC is verified with computer simulations. Extensive simulations are performed on a mainframe computer using Micro Linear's proprietary SPICE simulator. The simulations are performed over the worst case conditions of temperature and power supply voltages, as well as the expected process variations, to ensure a reliable and manufacturable device.

The accuracy of the simulations are strongly dependent on the accuracy of the component simulation models. Micro Linear device simulation models are developed from extensive characterization measurements on finished devices. They are verified by matching the characteristics the simulation program predicts versus regularly updated measurements from the finished production worthy devices.

Design Reviews

A thorough design review can have a significant positive impact on the success of a USIC development. At Micro Linear detailed design reviews are conducted with the customer engineer and several Micro Linear engineers in attendance. All aspects of the design are reviewed including system performance, circuit schematics, simulation results, layout plan, test strategies, and package options. Upon completion of this review both the customer and Micro Linear have a high confidence for completely functional prototypes.

USIC Development Program

A brief summary of the steps involved in developing an USIC with Micro Linear are:

1. SEND INFORMATION TO MICRO LINEAR
   Customer sends block diagrams, schematics, and specification requirements on prospective USIC to Micro Linear for review.
2. TECHNICAL REVIEW AND QUOTE
   Micro Linear reviews the customers block diagrams, schematics, and specifications and responds with technical assessment, costs and development times.
3. FINALIZE DEVELOPMENT PLAN
   Micro Linear and customer agree on the development plan.
4. FINALIZE CIRCUIT REQUIREMENTS
   Micro Linear consults closely with the customer to completely understand the functional and performance requirements.
5. CIRCUIT DESIGN AND SIMULATION
   Micro Linear performs the circuit design and simulation verification.
6. DESIGN REVIEW
   Customer participates in a detailed design review with Micro Linear engineers.
7. MASK LAYOUT
   Micro Linear performs the mask layout for the circuit on the chosen tile array.
8. INTEGRATION
   Micro Linear performs the integration steps including: Masks making, wafers processing, wafer test, packaging, and prototype testing.
9. DELIVER PROTOTYPES
   Micro Linear delivers prototypes to customer.
10. CUSTOMER EVALUATES PROTOTYPES

FB3600 Tile Array Selection Guide

Array		FB3605	FB3610	FB3620	FB3621	FB3622	FB3623	FB3630	FB3631	FB3635
Description		Small High Frequency	Small General Purpose	Medium General Purpose	Medium High Frequency	Medium Power Schottky	Medium High Power	Large General Purpose	Large Mixed Analog/ Digital	Large Mixed Analog/ Digital
Mini Tile Summary										
T1	General	10	48	64	48	48	64	112	92	36
T1A	General	10								
T2	Specialized	2	6	12	8	12	12	24	12	4
T2A	Specialized	2								
T3	Power	2	4	4	2		4	4	4	2
T4	Low Noise		4	4	4		2	4		
T5	Precision			4			4	8		2
T6	NPN Intensive				8					8
T7	High Frequency				12	12			4	12
T8	Schottky Core									4
T9	ECL Logic	10							22	42
T10	ECL Logic Bias								1	1
T11	TTL Output	8			4				8	8
T12	Schottky Peripheral									2
T13	High Frequency	4								
T14	High Power NPN						4			
T15	Medium Current PNP						4			
T16	Power Schottky					14				
T17	General								1	
Array Summary										
Complexity*										
Analog		4	6	12	8	12	12	24	12	9
Digital		28							62	130
NPN Transistors		260	178	268	329	276	272	472	690	901
PNP Transistors		32	78	124	88	108	132	232	154	63
Schottky Transistors		16			8	14			16	48
Total Diffused Resistance		240K	288K	425K	495K	432K	425K	768K	850K	818K
Total Implant Resistance		816K	1563K	2048K	2064K	1920K	2048K	3584K	3928K	3064K
Total MOS Capacitance		20pF	30pF	60pF	40pF	60pF	60pF	120pF	60pF	40pF
Total Components		840	742	1092	1508	1370	1360	1944	2806	2805
Bond Pads		24	24	32	32	28	27	46	44	44
Die Size (mils)		70 × 110	82 × 102	102 × 115	102 × 115	112 × 125	115 × 122	131 × 150	142 × 156	131 × 150

* Analog complexity is in one 741 op-amp or two 339 comparator equivalents.
Digital complexity is in two input NAND gate equivalents.

(See also Power Supplies Arrays in section 6)

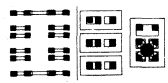
Component Performance

COMPONENT	FB3600 FAMILY
NPN Transistor	h_{FE} = 120 f_T = 750MHz BV_{ceo} = 14V
NPN Large Transistor (FB3623 Only)	h_{FE} = 100 f_T = 750MHz BV_{ceo} = 14V I_C = 0.5A
PNP Substrate Transistor	h_{FE} = 60 f_T = 24MHz BV_{ceo} = 25V
PNP Lateral Transistor	h_{FE} = 30 f_T = 12MHz BV_{ceo} = 25V
Diffused Resistor	2% matching with ±20% absolute value
Precision Resistors	0.5% matching with ±20% absolute value
Implant Resistors	4% matching with ±25% absolute value
MOS Capacitor	±20% absolute value

FB3600 Mini Tile Description

T1 Mini Tile

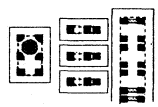
The T1 mini tile contains the components that constitute the major portion of most analog designs. It can implement many common building block functions such as current mirrors, differential gain stages and level shifters. It is the most general-purpose analog building block and has the greatest frequency of placement within the arrays.



Components	Qty.
MLC3600 minimum NPN	3
MLC3611 lateral PNP	1
MLC3620 750Ω base resistor	8
MLC3621 4KΩ implant resistor	4
MLC3622 8KΩ implant resistor	2

T1A Small T1 Mini Tile

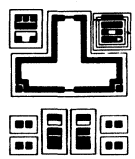
The T1A mini tile is a slightly modified T1 general purpose mini tile. It has the same active device count but has about half the resistor segments. Just like the T1 mini tile this tile is configured to implement many of the fundamental circuit blocks in integrated circuit design such as current mirrors, differential amplifiers and level shifters.



MLC3600 minimum NPN	3
MLC3611 lateral PNP	1
MLC3620 750Ω base resistor	4
MLC3621 4KΩ implant resistor	2

T2 Mini Tile

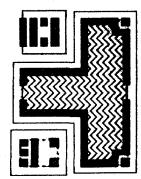
Many analog building blocks, such as op-amps, use a T2 mini tile along with multiple T1 mini tiles. This mini tile has the second greatest frequency of placement within the arrays. The MLC3630 is a silicon dioxide capacitor whose value can be programmed up to 5pF. This capacitor is often used to provide on-chip compensation for operational amplifiers.



MLC3601 circular emtter NPN	2
MLC3602 three emitter NPN	1
MLC3610 minimum vertical PNP	4
MLC3612 2X vertical PNP	1
MLC3630 5pF MOS capacitor	1

T2A Small T2 Mini Tile

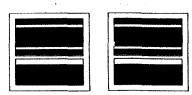
This mini tile is very similar to but smaller than the T2 mini tile. This mini tile is typically used in conjunction with several T1 mini tiles. Operational amplifiers that use an on-chip compensation capacitor are built with a T2 or T2A and T1 mini tiles.



MLC3602 three emitter NPN	1
MLC3612 2X vertical PNP	1
MLC3630 5pF MOS capacitor	1

T3 Mini Tile

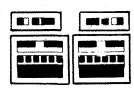
This mini tile contains two NPN power transistors for output stages driving up to 100mA each. These mini tiles are located in peripheral positions around the chips, in close proximity to the bonding pads.



MLC3605 power NPN	2

T4 Mini Tile

This mini tile contains two large six emitter low noise NPN transistors. These transistors are used in circuits which require noise performance of less than $5nV\sqrt{Hz}$. These transistors can also be medium capacity power transistors.



MLC3604 6X low noise NPN	2

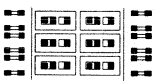
T5 Mini Tile

This mini tile contains six minimum geometry NPN transistors and twelve precision resistor links. These special resistors have a nominal ohmic value of 850Ω and are matched to within an accuracy of 0.5%. It is possible to construct R-2R ladders to be used in the core of an 8-bit DAC by using two T5 mini tiles.

Components	Qty.
MLC3600 minimum NPN	6
MLC3625 850Ω precision resistor	12

T6 Mini Tile

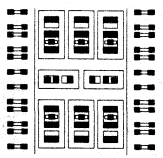
The T6 mini tile is designed for NPN intensive transistor circuit design. ECL logic can be implemented with this tile.



Components	Qty.
MLC3600 minimum NPN	6
MLC3620 750Ω base resistor	8
MLC3621 4KΩ implant resistor	4

T7 Mini Tile

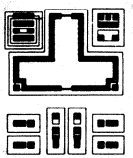
This mini tile contains six dual base contact 10mA high speed, low noise NPN transistors. Each of these small transistors has a 50Ω base resistance. Two T7 tiles can implement 100MHz cascode amplifier or a 60MHz video amplifier.



Components	Qty.
MLC3600 minimum NPN	2
MLC3606 double base NPN	6
MLC3620 750Ω base resistor	16
MLC3621 4KΩ implant resistor	8

T8 Mini Tile

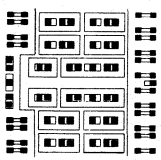
The T8 mini tile contains a mixture of schottky and other components for analog design. The schottky devices are useful for clamping signal levels and in certain high speed comparator designs.



Components	Qty.
MLC3607 minimum schottky NPN	2
MLC3602 three emitter NPN	1
MLC3612 2X vertical PNP	1
MLC3608 minimum schottky diode	4
MLC3630 5pF MOS capacitor	1

T9 Mini Tile

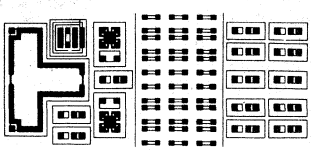
This mini tile contains one basic ECL logic cell which can implement one data latch (with set & reset). Two basic ECL logic cells can implement one edge triggered D-type flip-flop (with set and reset). An alternative usage for one basic ECL logic cell would be to implement three 2-input ECL gates, two 4-input ECL gates or one 8-input ECL gate. The actual gate can be a NAND, AND, OR or NOR gate. Two of the minimum NPNs have their collectors tied to V_{CC}.



Components	Qty.
MLC3600 minimum NPN	8
MLC3600A two minimum NPNs	2
MLC3600B minimum NPN	2
MLC3600C minimum diode	2
MLC3620 750Ω base resistor	12
MLC3621 4KΩ implant resistor	8

T10 Mini Tile

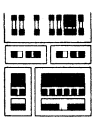
The T10 mini-tile provides the necessary temperature adjusted reference voltages for biasing the ECL logic. Unlike analog voltage references, ECL logic needs the bias reference to vary with temperature. This mini tile has its function predefined for most applications.



Components	Qty.
MLC3600 minimum NPN	13
MLC3611 lateral PNP	2
MLC3612 2X vertical PNP	1
MLC3620 750Ω base resistor	30
MLC3621 4KΩ implant resistor	6
MLC3630 5pF MOS capacitor	1

T11 Mini Tile

This mini tile contains components for building an output buffer for a TTL or CMOS output stage (TTL fanout of 2). The mini tile can convert the on-chip ECL logic levels to TTL or CMOS logic levels.



Components	Qty.
MLC3600 minimum NPN	2
MLC3609 6X schottky NPN	1
MLC3613 2X schottky NPN	1
MLC3620 750Ω base resistor	5
MLC3621 4KΩ implant resistor	1
MLC3624 50Ω emitter resistor	1

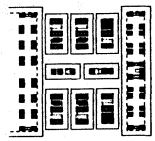
T12 Mini Tile

The T12 mini tile contains additional Schottky components for building TTL or CMOS input or output buffers.

Components	Qty.
MLC3607 minimum schottky NPN	2
MLC3609 6X schottky NPN	2

T13 High Frequency Mini Tile

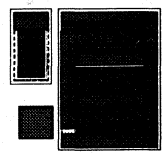
High frequency circuit design requires specially designed components. This mini tile contains transistors with low internal base resistance and low value, small area base resistors essential for high frequency circuit design. The low value resistors are critical in high frequency design as load resistors to achieve a practical output swing with the high currents necessary to maximize the bandwidth of the transistors. The small area of these resistors is also very important because it minimizes the parasitic capacitance that limits high frequency performance. This mini tile contains minimum NPN transistors, circular NPN transistors, double base NPN transistors, base, implant, and small area base resistors.



Components	Qty.
MLC3600 minimum NPN	2
MLC3601 circular emitter NPN	2
MLC3606 double base NPN	4
MLC3620 750Ω base resistor	8
MLC3621 4KΩ implant resistor	4
MLC3629 225Ω base resistor	6

T14 High Power NPN Mini Tile

The T14 mini tile contains a high current NPN power transistor and a clamp diode. These devices along with the PNP transistors on the T15 mini tile can implement a high power output stage with surge protection. The NPN power transistor can handle 0.5 Amps of current. The clamp diode is connected to protect the large NPN from transient surge voltages and currents.



MLC3605A high power NPN (0.5A)	1
MLC3609A clamp diode	1

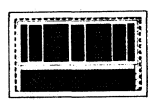
T15 Medium Current PNP Mini Tile

This mini tile has the PNP transistors that work in conjunction with the power devices in the T14 mini tile to implement an output stage. These PNP transistors can supply the necessary base drive current, up to 10 mA, for the large NPN transistors. Also on this mini tile is a smaller PNP that is a scaled version of the large PNP. This PNP is typically connected with the larger PNP as a current mirror with a gain of nine.

MLC3616 36X lateral PNP	1
MLC3615 4X lateral PNP	1

T16 Power Schottky Mini Tile

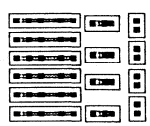
The T16 mini tile consists of one schottky NPN transistor capable of handling 120 mA. This schottky device is useful in the design of output stages that need to drive high current pulses into magnetic heads. Switching speed is enhanced over a regular power transistor because saturation, and the resulting speed degradation, is avoided with the schottky transistor.



MLC3631 large Schottky NPN	1

T17 General Purpose Mini Tile

The T17 mini tile is used for general purpose design. It contains minimum NPN and minimum vertical PNP transistors and implant resistors.



MLC3600 minimum NPN	4
MLC3610 minimum vertical PNP	4
MLC3621 4KΩ implant resistor	12
MLC3622 8KΩ implant resistor	6

FB3605 Small High Frequency Tile Array

GENERAL DESCRIPTION

The FB3605 is a bipolar analog tile array developed for mixed analog and digital applications that require high frequency performance. This FB3600 family tile array utilizes our proprietary mini tile architecture. The mini tile approach combined with our 12 volt, 1 GHz technology allows high complexity, high speed circuits to be easily integrated.

High frequency circuits like a 90 MHz voltage controlled oscillator or other similar performance circuits can be integrated using the FB3605 tile array. In addition to this particular circuit block the array can also contain 4 full function op amps (741 type) as well as 28 gates of ECL logic and 8 digital output buffers capable of interfacing to ECL, TTL, or CMOS.

A new high frequency mini tile was designed for this array. This mini tile contains 4 double base, high frequency NPNs and 6 low value (225 ohm) base resistors along with other NPNs and resistors. The double base NPNs and the low value base resistors are the key to implementing high frequency circuits.

The FB3605 is the smallest of the FB3600 family of arrays. The small die, 70 by 110 mils, allows it to fit into a very small package. The FB3605 can be assembled in a 0.15 inch wide SOIC package for minimum board space.

FEATURES

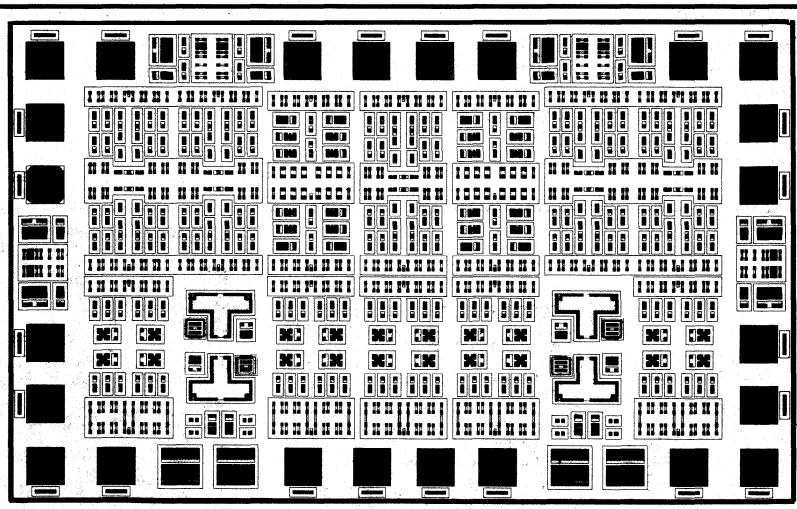
- High frequency operation
- Small die size — Fits in narrow SOIC Package
- Mixed Analog and Digital circuitry
- 5 analog circuit blocks with 28 ECL gates
- On chip MOS capacitors
- 12 volt, 1 GHz technology

ARRAY SUMMARY

NPN Transistors	260
PNP Transistors	32
Schottky Transistors	16
Total Diffused Resistance	240 K
Total Implant Resistance	816 K
Total MOS Capacitance	20 pF
Total Components	840
Bond Pads	24
Die Size (mils)	70 × 110

MINI TILE SUMMARY

T1 General	10
T1A Small T1	10
T2 Specialized	2
T2A Small T2	2
T3 Power	2
T9 ECL	10
T11 TTL Output	8
T13 High Frequency	4



FB3605 — Small High Frequency Tile Array

FB3610, FB3620, FB3630 General Purpose Tile Arrays

GENERAL DESCRIPTION

The FB3610, FB3620, and FB3630 are general purpose analog tile arrays capable of implementing a wide range of circuit functions. These FB3600 family arrays use our proprietary mini-tile architecture. The mini-tile approach combined with our 12-volt, 1 GHz technology allows high complexity, high speed circuits to be easily integrated.

Each of these general purpose arrays have the same basic structure. The difference is in the number of mini-tiles and therefore the number of total components available on each array. The different arrays can incorporate differing levels of circuit complexities. The FB3610 is the smallest and able to contain approximately six full function operational amplifiers or twelve comparators. The largest general purpose array, the FB3630, can incorporate 24 operational amplifiers or as many as 48 comparators.

Both the FB3620 and FB3630 contain precision resistor mini-tiles which allows precision circuits to be integrated on these arrays. The typical resistor match of 0.5% enables an 8-bit DAC to be implemented. All three of these arrays also contain low noise and power devices. The low noise transistors allow circuits with less than $5nV/\sqrt{Hz}$ input referred noise to be realized. The power transistors can supply up to 100mA each and can be paralleled for higher currents. Other FB3600 arrays can achieve up to 2 amps.

High performance circuits can be implemented on these arrays. Amplifiers with bandwidths up to 70 MHz and voltage controlled oscillators up to 50 MHz can be implemented on the FB3610, FB3620 or FB3630 arrays. Higher frequency performance can be achieved on other FB3600 family tile arrays.

FEATURES

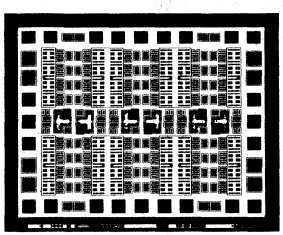
- High complexity and high performance
- Operates with supplies up to 12 volts, ±10%
- Flexible mini-tile architecture
- Precision and high current components
- 12 volt, 1 GHz technology

ARRAY SUMMARY

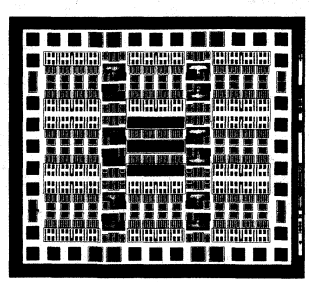
	FB3610	FB3620	FB3630
NPN Transistors	178	268	472
PNP Transistors	78	124	232
Total Diffused Resistance	288K	425K	768K
Total Implant Resistance	1563K	2048K	3584K
Total MOS Capacitance	30pF	60pF	120pF
Total Components	742	1092	1944
Bond Pads	24	32	46
Die Size (mils)	82 × 102	102 × 115	131 × 150

MINI-TILE SUMMARY

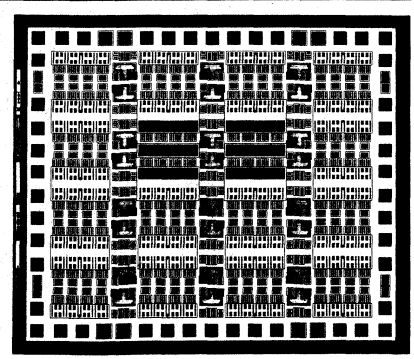
		FB3610	FB3620	FB3630
T1	General	48	64	112
T2	Specialized	6	12	24
T3	Power	4	4	4
T4	Low Noise	4	4	4
T5	Precision		4	8



FB3610



FB3620



FB3630

FB3621 Medium High Frequency Tile Array

GENERAL DESCRIPTION

The FB3621 array is ideal for applications that have high frequency and low noise requirements. This FB3600 family tile array utilizes our proprietary mini-tile architecture. The mini tile approach combined with our 12-volt, 1 GHz technology allows high complexity, high speed circuits to be easily integrated.

High frequency and low noise circuits require transistors with low parasitic base resistance. This array contains a large number of transistors with dual base contacts and therefore low base resistance. In addition to these high frequency/low noise NPNs the array has a high percentage of regular NPN devices. The high overall number of NPN transistors enables a large number of high frequency circuit blocks to be implemented. ECL logic, which uses mostly NPN devices, can also be integrated on this array.

Typical types of circuit functions that can be implemented on the FB3621 array are 100 MHz cascode amplifiers, VCOs, wideband/low noise amplifiers, and high speed comparators (T_D < 5ns).

FEATURES

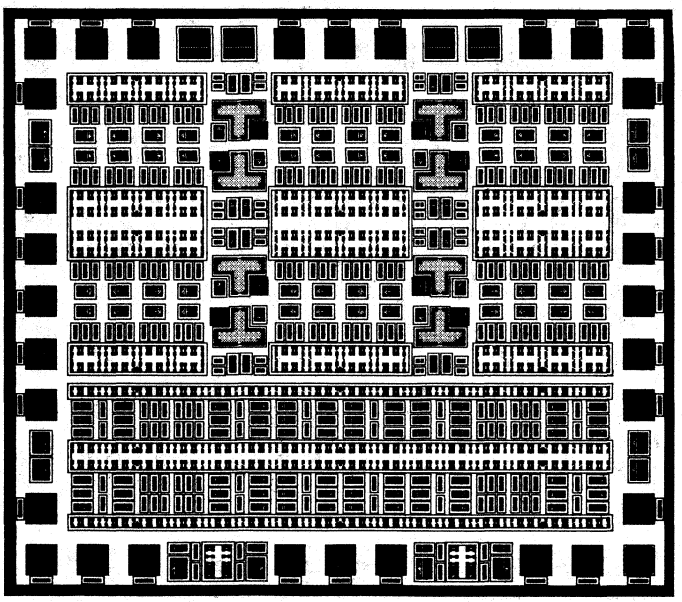
- High frequency operation
- Low noise circuits
- On-chip MOS capacitors
- 12 volt, 1 GHz technology

ARRAY SUMMARY

NPN Transistors	329
PNP Transistors	88
Schottky Transistors	8
Total Diffused Resistance	495K
Total Implant Resistance	2064K
Total MOS Capacitance	40pF
Total Components	1508
Bond Pads	32
Die Size (mils)	102 x 115

MINI TILE SUMMARY

T1 General	48
T2 Specialized	8
T3 Power	2
T4 Low Noise	4
T6 NPN Intensive	8
T7 High Frequency	12
T11 TTL Output	4



FB3621 — Medium High Frequency Tile Array

FB3622 Medium Power Schottky Tile Array

GENERAL DESCRIPTION

The FB3622 is a bipolar analog tile array developed for applications that require fast high current outputs. This FB3600 family tile array utilizes our proprietary mini tile architecture. The mini tile approach combined with our 12 volt, 1 GHz technology allows high complexity, high speed circuits to be easily integrated.

Around the perimeter of the die are fourteen large schottky NPN power transistors. These power transistors, capable of handling over 100 mA each, make this array ideal for applications which call for driving inductive loads with high currents such as magnetic write heads. Twelve high frequency tiles expand the capabilities of this array. These high frequency tiles allow high frequency circuit blocks to be included on this array.

This array can accommodate eighteen functional blocks of the approximate complexity of a 324 operational amplifier.

FEATURES

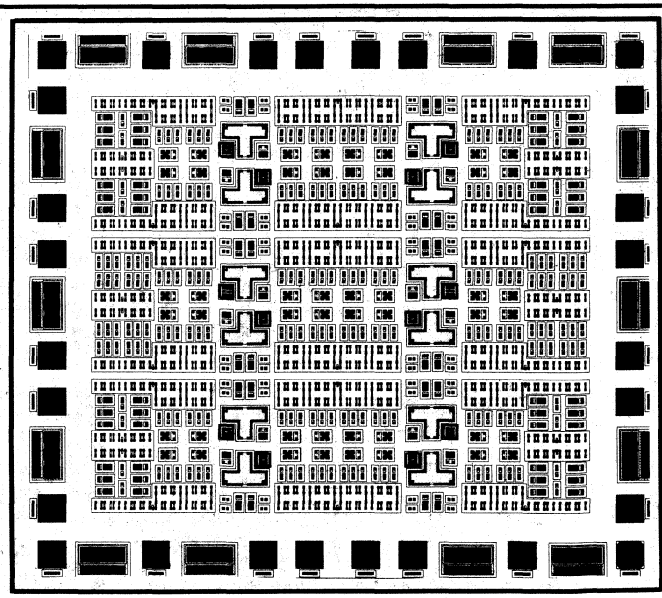
- 14 power schottky NPN transistors
- Design complexities of 18 functional blocks
- Precision and high frequency mini tiles
- On chip MOS capacitors
- 12 volt, 1 GHz technology

ARRAY SUMMARY

NPN Transistors	276
PNP Transistors	108
Schottky Transistors	14
Total Diffused Resistance	432 K
Total Implant Resistance	1920 K
Total MOS Capacitance	60 pF
Total Components	1370
Bond Pads	28
Die Size (mils)	112 × 125

MINI TILE SUMMARY

T1 General	48
T2 Specialized	12
T7 High Frequency	12
T16 Power Schottky	14



FB3622 — Medium Power Schottky Tile Array

FB3623 Medium High Power Tile Array

GENERAL DESCRIPTION

The FB3623 is a bipolar analog tile array capable of handling up to 2 amps of current. This FB3600 family tile array utilizes our proprietary mini tile architecture. The mini tile approach combined with our 12 volt, 1 GHz technology allows high complexity, high speed circuits to be easily integrated.

The array has two distinct sections, one with the power output devices and the other for general purpose circuits. The general purpose section, the larger area, is configured for circuits that can be designed using the various types of mini tiles. Op Amps, comparators, video amplifiers, voltage controlled oscillators, analog multiplexers, and mixers, are some examples of the types of circuit functions that can be realized using these mini tiles.

The other section of the array has components designed for high current output stages. Consisting primarily of four 0.5 A power NPNs, four 10 mA lateral PNPs, and four high current clamp diodes, this area can integrate output stages with a wide variety of configurations such as a four by 0.5A, two by 1 A, or 1 by 2 A for examples. The clamp diodes protect the output transistors from spurious transient signals on the output.

The two sections are separated by a diffused region which minimizes any coupling from the output transistor section back into the rest of the circuit which might cause problems due to high gain or low signal levels.

FEATURES

- High Current Capability — up to 2 A
- Mixed High Power and Low Level Circuits
- High complexity with High Performance
- On chip MOS capacitors
- 12 volt, 1 GHz technology

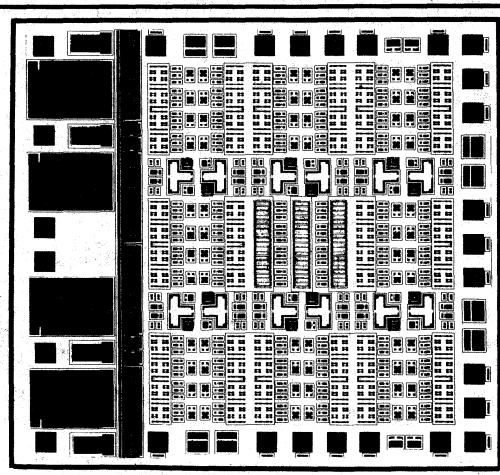
ARRAY SUMMARY

NPN Transistors	272
PNP Transistors	132
Total Diffused Resistance	425 K
Total Implant Resistance	2048 K
Total MOS Capacitance	60 pF
Total Components	1360
Bond Pads	27
Die Size (mils)	115 x 122

MINI TILE SUMMARY

T1 General	64
T2 Specialized	12
T3 Power	4
T4 Low Noise	2
T5 Precision	4
T14 High Power NPN	4
T15 High Power PNP	4

7



FB3623 — Medium High Power Tile Array

FB3631 Large Mixed Analog Digital Tile Array

GENERAL DESCRIPTION

The FB3631 tile array was developed for mixed analog digital applications. This FB3600 family tile array utilizes our proprietary mini tile architecture. The mini tile approach combined with our 12 volt, 1 GHz technology allows high complexity, high speed mixed signal circuits to be easily integrated.

This array is optimized for high complexity analog with a moderate amount of digital circuitry. For example, twelve 324 style operational amplifiers, sixty-six gates of logic, eight digital output buffers, and 3 other circuit blocks can all be implemented on a FB3631 tile array.

Our 1 GHz bipolar process allows us to achieve high performance circuits on our FB3600 tile arrays. Amplifiers with a bandwidth of 100 MHz and digital ECL gates with delays of 2 ns can be implemented on Micro Linear tile arrays.

FEATURES

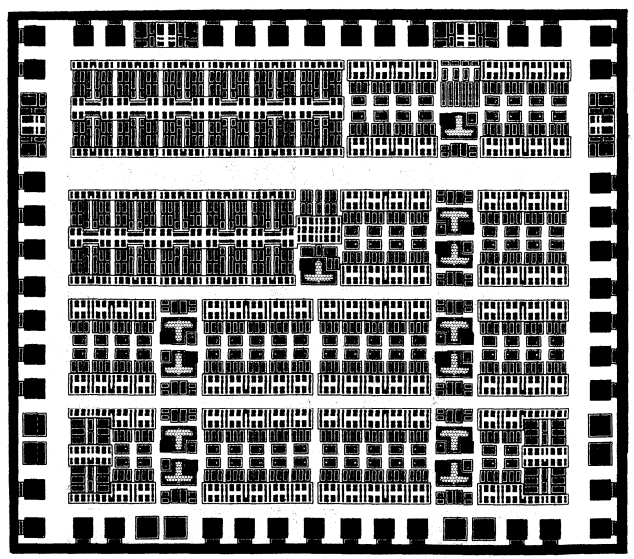
- Mixed Analog and Digital Circuitry
- 15 Analog circuit blocks with 66 ECL Gates
- 2800 Components, 44 Bond Pads
- On chip MOS Capacitors
- 12 volt, 1 GHz technology

ARRAY SUMMARY

NPN Transistors	690
PNP Transistors	154
Schottky Transistors	16
Total Diffused Resistance	850 K
Total Implant Resistance	3928 K
Total MOS Capacitance	60 pF
Total Components	2806
Bond Pads	44
Die Size (mils)	142 × 156

MINI TILE SUMMARY

T1 General	92
T2 Specialized	12
T3 Power	4
T7 High Frequency	4
T9 ECL	22
T10 ECL Bias	1
T11 TTL Output	8
T17 General	1



FB3631 — Large Mixed Analog Digital Tile Array

FB3635 Analog and Digital Tile Array

GENERAL DESCRIPTION

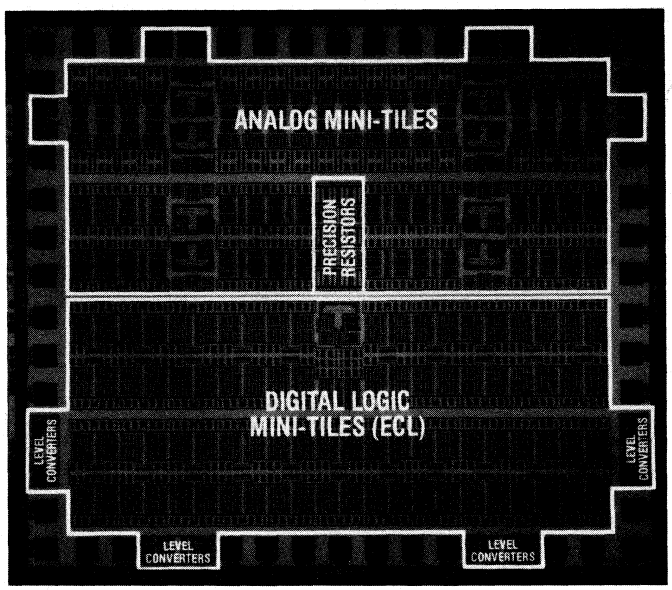
The FB3635 offers both analog and digital circuit design on a single tile array. The top half of the FB3635 contains components for analog circuit design. The bottom half of the array contains npn components for digital design.

The analog section can implement eight LM324 type op amps or twelve LM339 type comparators. Many comparator applications can use a comparator with npn transistors in the input stage. In this case, the analog section of the array can be filled with eighteen comparators. A two quadrant analog multiplier, AGC circuit, analog multiplexer (switch), video amplifier or a MC1496 type modulator/demodulator can also be implemented. Each of these functions requires roughly the same number of components as one op amp. In addition, the array can also implement one 8-bit DAC, four 100MHz cascode amplifiers and a voltage reference.

The digital section of the FB3635 contains forty two digital logic cells. Each digital logic cell can implement a one bit latch (with set and reset), or three NAND gates. Two digital logic cells can implement an edge triggered D type flip-flop with set and reset. All logic functions are implemented using ECL logic. This provides for 2 nanosecond gate propagation delays and flip-flop toggle rates of 80MHz. The logic area can be powered off of a single 5V supply. On-chip logic level converters can convert the arrays ECL logic levels to standard TTL, CMOS or ECL logic levels.

FEATURES

- Mixed analog and digital tile array
- Analog section
  - npn f_t 720MHz
  - pnp f_t 25MHz
  - Eight 5pF MOS capacitors
  - Operates up to 12V ±10%
- Digital section
  - 132 NAND gates or 42 latches
  - 2ns gate propagation delay
  - ECL logic using a single +5 volt supply
  - TTL, ECL, and CMOS compatibility



FB3635 Tile Array

FB3400 Tile Array Selection Guide

FB3400 Family (±18V or up to 36V supply operation)

Array		FB3410	FB3420	FB3430
Description		Small General Purpose	Medium General Purpose	Large General Purpose
Mini Tile Summary				
T1	General Purpose	16	32	44
T2	Special Devices	4	12	16
T3	Power Devices	4	4	4
T4	Low Noise Devices	0	4	0
T5	Precision Resistors	0	2	3
Array Summary				
Complexity*		4	12	16
NPN Transistors		132	296	394
PNP Transistors		52	124	168
Total Diffused Resistance		176K	384K	538K
Total Implant Resistance		1600K	3200K	4400K
Total MOS Capacitance		40pF	120pF	160pF
Total Components		524	1132	1500
Bond Pads		32	46	66

* Analog complexity is in one 741 op amp or two 339 comparator equivalents. Digital complexity is in two input NAND gate equivalents.

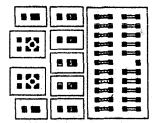
Component Performance (under typical operating conditions)

COMPONENT	FB3400 FAMILY
NPN Transistor	h_{FE} = 120 f_T = 300MHz BV_{ceo} = 40V
NPN Large Transistor (FB3623 Only)	
PNP Substrate Transistor	h_{FE} = 60 f_T = 20MHz BV_{ceo} = 45V
PNP Lateral Transistor	h_{FE} = 30 f_T = 3MHz BV_{ceo} = 45V
Diffused Resistor	2% matching with ±20% absolute value
Precision Resistors	0.5% matching with ±20% absolute value
Implant Resistors	4% matching with ±25% absolute value
MOS Capacitor	±20% absolute value

FB3400 Mini Tile Description

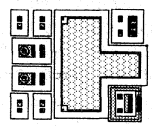
T1 Mini Tile

This is a general-purpose analog tile. It can implement many common building block functions, such as current mirrors, differential gain stages and level shifters. A T1 tile contains seven small geometry NPNs (ft 300MHz), two quad collector PNPs (ft 4MHz), eleven 1kΩ resistors, and ten 10kΩ resistors.



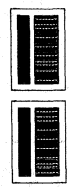
T2 Mini Tile

The T2 tile contains a collection of specialized components. Many analog building blocks, such as op-amps, use a T1 tile and a T2 tile. The T2 tiles contain two medium size low noise NPN transistors, four small substrate PNPs (ft 8MHz), one large substrate PNP (ft 8MHz), one triple emitter NPN, and a MOS capacitor whose value can be programmed up to 10pF.



T3 Mini Tile

The T3 file contains two NPN power transistors for output stages driving up to 100mA each. These tiles are situated in peripheral positions around the chips, in close proximity to the bonding pads.

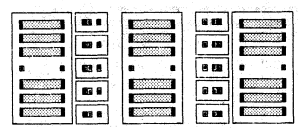


T4 Mini Tile

The T4 tile contains two low-noise NPN transistors which are used in circuits requiring low noise performance.

T5 Mini Tile

This mini tile contains ten minimum geometry NPN transistors and eighteen precision resistor links. These special resistors have a nominal ohmic value of 900Ω and are matched to within an accuracy of 0.5%. It is possible to construct R-2R ladders used in the core of an 8-bit DAC by using 24 resistors.



FB3410, FB3420, FB3430
General Purpose Tile Arrays

GENERAL DESCRIPTION

The FB3400 family has been designed to utilize the traditional analog ±15V signal swings and power supply rails. A single power supply of up to 36V or split power supplies of up to ±18V can be utilized. Significant board space and cost savings are possible with the FB3400 family of analog tile arrays.

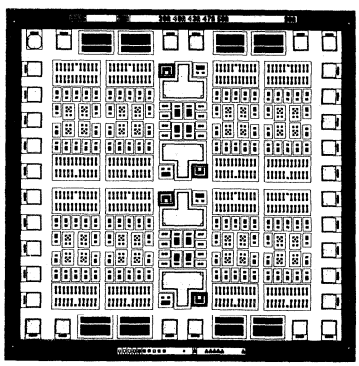
A single FB3400 Analog ASIC can typically replace ten to twenty standard analog building block components. In addition, many of the active and passive components surrounding the discrete building blocks can be incorporated on-chip.

The FB3400 family utilizes Micro Linear's new mini-tile architecture concept. The FB3400 family uses five different mini-tiles. One or more mini-tiles can be combined to implement functional blocks such as op-amps, comparators, voltage references, video amplifiers, transconductance amplifiers, modulators, demodulators, RS-232, RS-432, RS-422, V.35 drivers & receivers, D/A and pulse width modulation circuits.

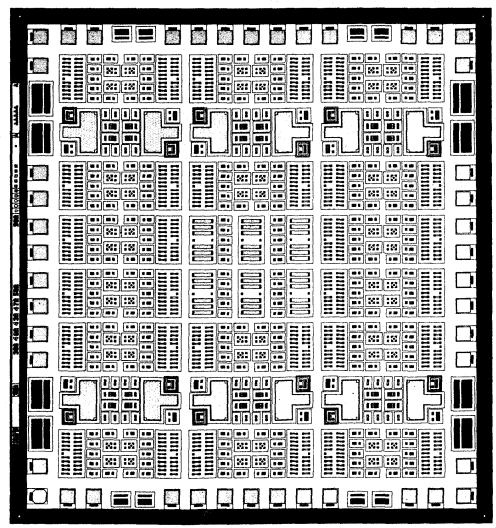
FEATURES

- Optimized for up to 36V operation
- High Component Density, dual layer metal process
- 300MHz array technology
- Three high performance family members
- Design complexities of up to 16 op-amps
- On-chip precision resistors and compensation capacitors

GENERAL PURPOSE ANALOG ARRAYS



FB3410



FB3420

Package Selection Guide

Package	FB3605	FB3610	FB3620	FB3621	FB3622	FB3623	FB3630	FB3631	FB3635	FB3410	FB3420	FB3430
SDBRZ-8	X	X	X	X	X	X	X		X	X		
SDBRZ-14	X	X	X	X	X	X	X		X	X		
SDBRZ-16	X	X	X	X	X	X	X		X	X		
SDBRZ-18	X	X	X	X	X	X	X		X	X		
SDBRZ-20	X	X	X	X	X	X	X		X	X		
SDBRZ-22	X	X	X	X	X	X	X	X	X	X	X	
SDBRZ-24	X	X	X	X	X	X	X	X	X	X	X	
SDBRZ-28	X	X	X	X	X	X	X	X	X	X	X	X
SDBRZ-40	X	X	X	X	X	X	X	X	X	X	X	X
LCC-28	X	X	X	X	X	X	X	X	X	X	X	X
CDIP-8	X	X								X		
CDIP-14	X	X								X		
CDIP-16	X	X	X	X	X	X	X			X		
CDIP-18	X	X	X	X	X	X	X		X	X		
CDIP-20	X	X	X	X	X	X				X		
CDIP-22	X	X	X	X	X	X	X	X	X	X	X	X
CDIP-24	X	X	X	X	X	X	X	X	X	X	X	X
CDIP-28	X	X	X	X	X	X	X	X	X	X	X	X
CDIP-40	X	X	X	X	X	X	X	X	X	X	X	X
PDIP-8	X	X	X	X	X							
PDIP-14	X	X	X	X	X	X				X		
PDIP-16	X	X	X	X	X	X				X		
PDIP-18	X	X	X	X	X	X				X		
PDIP-20	X	X	X	X	X	X				X		
PDIP-22	X	X	X	X	X	X	X	X	X	X	X	
PDIP-24	X	X	X	X	X	X	X	X	X	X	X	X
PDIP-28	X	X	X	X	X	X	X	X	X	X	X	X
PDIP-32	X	X	X	X	X	X	X	X	X	X	X	X
PDIP-40	X	X	X	X	X	X	X	X	X	X	X	X
PDIP-48	X	X	X	X	X	X	X	X	X	X	X	X
PCC-20	X	X	X	X	X	X	X	X	X	X	X	
PCC-28	X	X	X	X	X	X	X	X	X	X	X	X
PCC-32	X	X	X	X	X	X	X	X	X	X	X	X
PCC-44	X	X	X	X	X	X	X	X	X	X	X	X
PCC-68	X	X	X	X	X	X	X	X	X	X	X	X

Package	FB3605	FB3610	FB3620	FB3621	FB3622	FB3623	FB3630	FB3631	FB3635	FB3410	FB3420	FB3430
SOIC-8												
SOIC-14												
SOIC-16	X	X	X	X	X	X				X		
SOIC-18	X	X	X	X	X	X	X		X	X	X	
SOIC-20	X	X	X	X	X	X				X	X	
SOIC-24	X	X	X	X	X	X	X		X	X	X	
SOIC-28	X	X	X	X	X	X	X	X	X	X	X	
SOIC-32	X	X	X	X	X	X	X	X	X	X	X	X

X — Indicates the array is available in this package

Package Descriptions

SDBRZ = Sidebrazed DIP
LCC = Leadless Chip Carrier
CDIP = Ceramic DIP
PDIP = Plastic DIP
PCC = Plastic Leaded Chip Carrier
SOIC = Small Outline

Quality and Reliability

Section 8

Quality and Reliability

Micro Linear is dedicated to excellence in its people and products. By adopting a policy of continuous improvement, we pledge to provide defect free products and services which meet or exceed our customers' expectation.

Total Quality Control

At Micro Linear we are committed to total quality control by building quality into every step of the manufacturing process from design to product qualification; from receiving to shipping. The Quality and Reliability Assurance program at Micro Linear Corporation is a detailed program involving engineering and manufacturing and is designed to produce the highest quality linear integrated circuits available.

Wafer Inspection

Emphasis is placed on statistical analysis, electrical measurements on specially designed Process Control Monitors in accordance with MIL-STD-414 (sampling by variables), visual inspection, and film measurements. Potential reliability hazards are investigated and detected early by utilizing diagnostic and device structures on each wafer and periodic SEM analysis.

Assembly Inspection

Comprehensive receiving inspection for all materials and piece-parts is performed in accordance with the strictest quality assurance procedures. To assure conformance and control to specifications, documented quality control checks and monitors are performed on-line.

Testing

Micro Linear has invested in the latest "state-of-the-art" analog testers to achieve the most complete and thorough parametric testing of integrated circuits in the industry. Data sheets provide the customer a precise listing of parameters which are 100% tested. The calibration system is in compliance with MIL-STD-45662.

Traceability

For complete traceability to wafer fab and assembly lot, a mark is placed on all packages giving information on a unit-by-unit basis.

Micro Linear considers traceability to be essential for good engineering control and additional insurance for its customers.

ESD (Electro Static Discharge)

Products are fully characterized to MIL-STD-883C, Method 3015 and strict controls on handling and packaging are observed. A full ESD program, from design through manufacturing, incorporates training of all employees who handle Micro Linear products.

Major Change Control

Major change controls are in place to notify customers in accordance with MIL-M-38510. Micro Linear reviews all process, product, and package changes. All changes with possible impact are submitted for a re-qualification which may include electrical, mechanical, and/or thermal characterization. If applicable, reliability requalification is performed.

Process Control

Process monitors and gate inspections insure that all devices are properly tested and that the required sample tests are performed prior to shipment. Inspection records and reports concerning monitors and inspection data are used to status the quality level of products through the final test operations. Statistical sampling plans insure the quality of the product.

Micro Linear welcomes OEM quality system surveys. Micro Linear is qualified by a number of customers to MIL-Q-9858A and MIL-I-45208 for military programs.

Failure Analysis and Reporting of Customer Returns

A formal program exists to record, analyze, and take appropriate corrective action on all returns. A Corrective Action Committee reviews all discrepancies and assigns responsibility to implement solutions or improvements on a weekly basis. A report is generated and sent to the customer stating our findings and corrective action.

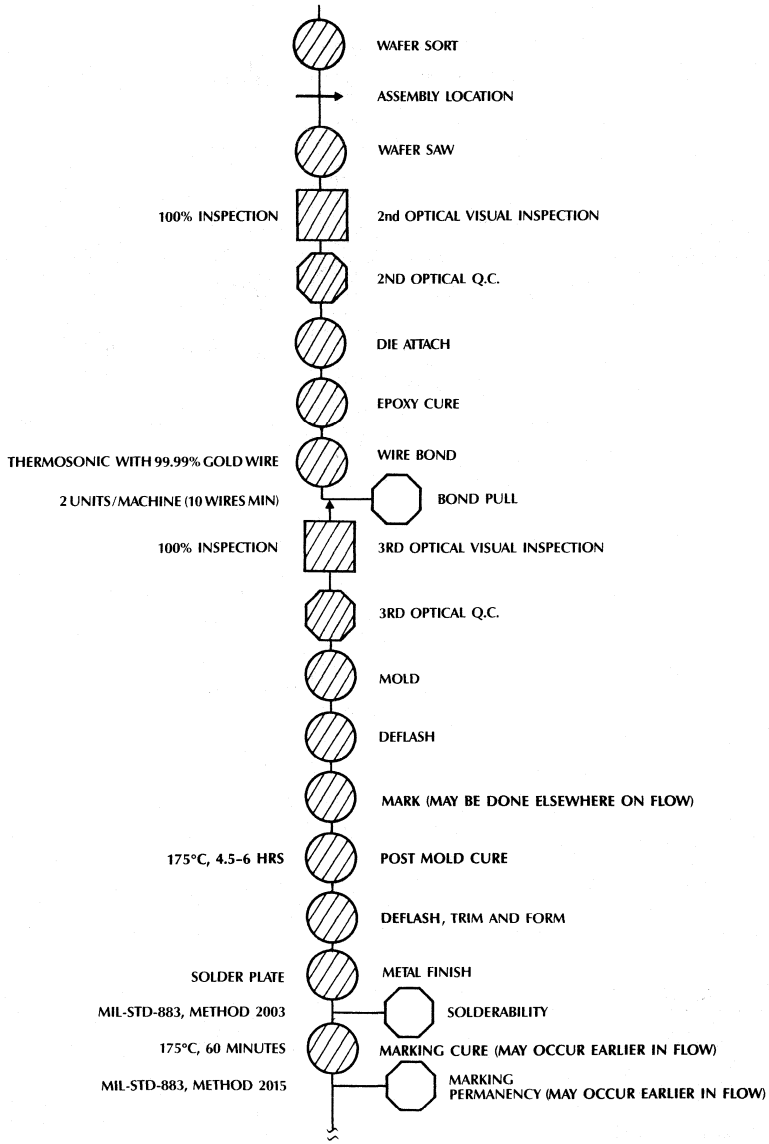
Document Control

All records providing product traceability are maintained in accordance with MIL-M-38510. All company documents for procedures, specifications, drawings, travelers, flow charts, schematics, etc. that define customer requirements, raw material requirements, design, manufacture, and testing of products are controlled by a Document Control organization within the Micro Linear's Quality Assurance group.

Audits

Critical manufacturing areas are audited by a quality inspector at specified intervals. The audit verifies adequacy of operator training, correct revisions, the procedures, proper data entry, and record maintenance. In addition, weekly audits include an ESD program, particle count, calibration, and document control programs.

Molded Package Flow



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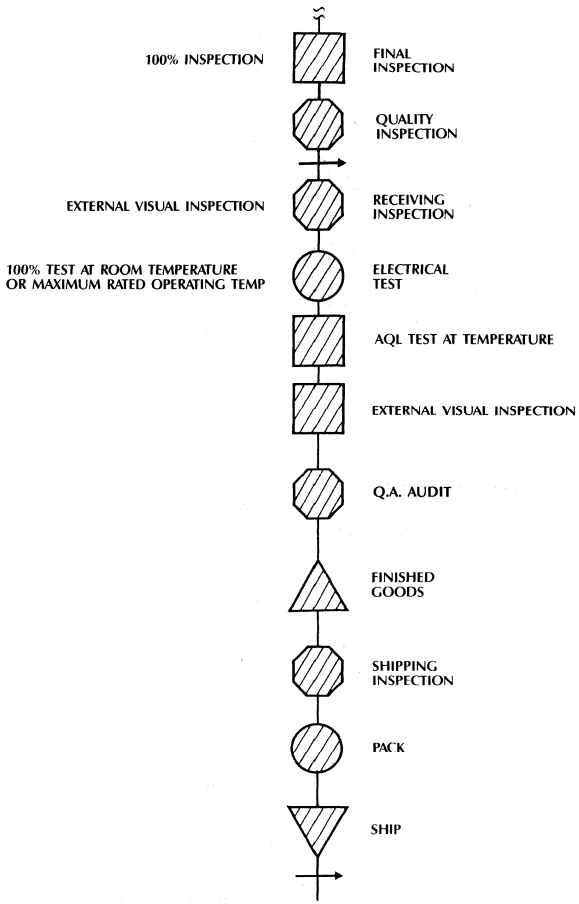
Molded Package Flow (Continued)



FLOW CHART SYMBOLS

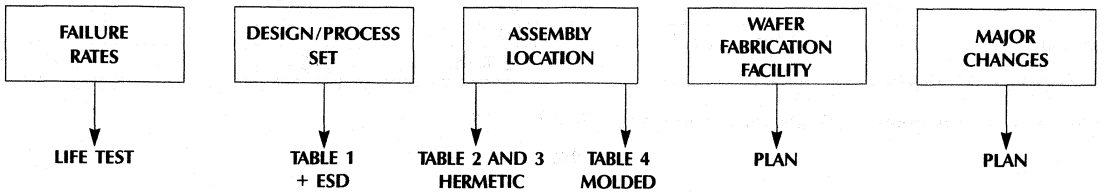
- Production
- Production Inspection
- Quality Inspection
- Transport
- Store Inventory
- Quality Monitor

Reliability Program

Micro Linear's Reliability Program consistent with those of other semiconductor manufacturers utilizes various accelerated life tests as tools for establishing reliability status and progress. These tests are undertaken to identify infant mortality and wearout failure mechanisms for specific or generically similar device families.

Micro Linear's Reliability Program has two components: Qualification and Quality Conformance Inspection. Each design/process technology set, each wafer fabrication facility, and each assembly location by package type is initially qualified. Periodic re-evaluation (Quality Conformance Inspection) is performed. The plan is illustrated in Figures 1 and 2 and detailed in Tables 1 through 4.

Micro Linear's product reliability is monitored closely and we have an extensive reliability data base for both hermetic and molded devices. This data is published on a quarterly basis. Micro Linear is seeing reliability failure rates of less than 10 FITS at 55°C.



Note: "PLAN" are the appropriate stresses and tests determined by reliability engineering.

Figure 1. Qualification Testing

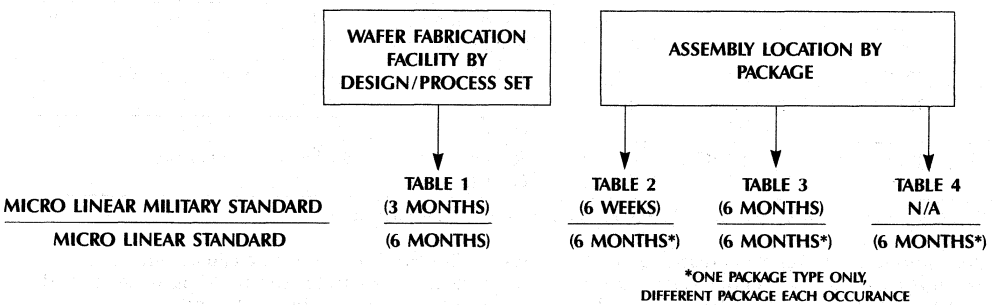


Figure 2. Quality Conformance Inspection

Test	Method	Condition	Quantity
Life Test	1005	1000 hrs @ 125°C	100

The die related test of Table 1. Evaluates the wafer fabrication process, the design rules, and die to package material interface reliability.

Table 1.

Test	Method	Condition	Quantity
Resistance to Solvents	2015		4
Bond Strength	2011		15
Solderability	2003	245°C	15

Table 2 inspects hermetic package related parameters for quality conformance.

Table 2.

Test	Method	Condition	Quantity
Physical Dimensions	2016		15
Thermal Shock Temp. Cycle Moist Resistance Seal Visual Electrical	1011 1010 1004 1014	B, 15 cycles C, 100 cycles	15
Lead Integrity Seal	2004 1014	B2	15
Internal H_2O Vapor	1018	5000 PPM max	3

Test	Method	Condition	Quantity
Adhesion of Lead Finish	2025		15
Mech Shock Vibration Acceleration Seal Visual Electrical	2002 2007 2001 1014	B A E	15
Salt Seal Visual	1009 1014	A	15
Lid Torque	2024		45

Table 3 evaluates hermetic packages for integrity and reliability.

Table 3.

Test	Method	Condition	Quantity
Physical Dimensions	2016		15
Resistance to Solvents	2015		4
External Visual	QAP 34001		15
Thermal Shock	1011	–65°C to +150°C 100 cycles	45
Temperature Cycle	1010	–55°C to +125°C 1000 cycles	45

Test	Method	Condition	Quan
HAST		130°C, 85% RH 50 hrs, Biased	45
Solderability	2003		3
Resistance to Soldering Heat	QAP 36002	260°C	15
Autoclave	QAP 36004	121°C, 2 Atm 168 hrs	45
High Temperature OP Life	QAP 36005	125°C 1000 hrs	77

Note: All methods in Tables 1 through 4 are from MIL-STD-883. All QAPs are Micro Linear procedures.

Table 4 evaluates molded packages for integrity and reliability. Micro Linear uses HAST (Highly Accelerated Stress Test) at 130°C and 85% RH for 50 hours instead of the conventional 85°C and 85% RH test for 1000 hours. The HAST procedure evaluates the effect of moisture as it penetrates the molding material and reaches the die while voltage biased.

Table 4.

Process Control/Quality Conformance

Reliability evaluations provide a snapshot of the product at a particular point in time. Process control is necessary to insure the picture obtained is accurate. Process control provides consistency and hence, predictability.

Defect-free material is a pre-requisite to shipping cost-effective products which conform to specified requirements. The system for doing this is shown in Figure 3. The focal point to this system is the Vendor Qualification Board comprised of representatives from Manufacturing Engineering, Quality, Reliability, and Purchasing. In addition, a Corrective Action Committee with representatives from the above disciplines meets weekly to evaluate all discrepant material reports. These reports are the result of any non-conformance both internal and external (vendors) to Micro Linear.

Because of the extreme sensitivity of wafer fabrication on product reliability, special care is taken to evaluate wafer process control. This is shown in Figure 4.

Wafer Fab Process Control

MASKING

- Resist Thickness-Control Chart
- CD Calibration
- Exposure-Control Chart
  - — Intensity
  - — Time

GLASSIVATION/INSULATOR

- Uniformity-Control Chart
- Thickness-Control Chart
- Phosphorus Content-Irend Chart
- Defect Count-Control Chart

ENVIRONMENT

- Air Temperature Control Chart
- Air Flow Control Chart
- Air Humidity Control Chart
- Water Bacteria Control Chart
- Water Resistivity Monitored
- Water Solids
- Organic Impurities in Water
- Chlorine Content of Water

METAL DEPOSITION

- Thickness-Control Chart
- CV Plots
- SEM Inspection

Each assembly location is also required to monitor and maintain control of operations as shown below.

Assembly Process Control

Micro Linear is certified to MIL-Q-9858 and MIL-I-45208, and is product compliant with all the requirements of MIL-STD-883C.

- DI water $>$ 10MΩ
- Two internal visual inspections
- Die shear monitor
- Wire bond monitor
- Air monitors (temperature, humidity, particles)
- Marking permanency test
- External visual inspection
- Plating monitor
- Raw material evaluation
- CERDIP sealing environment

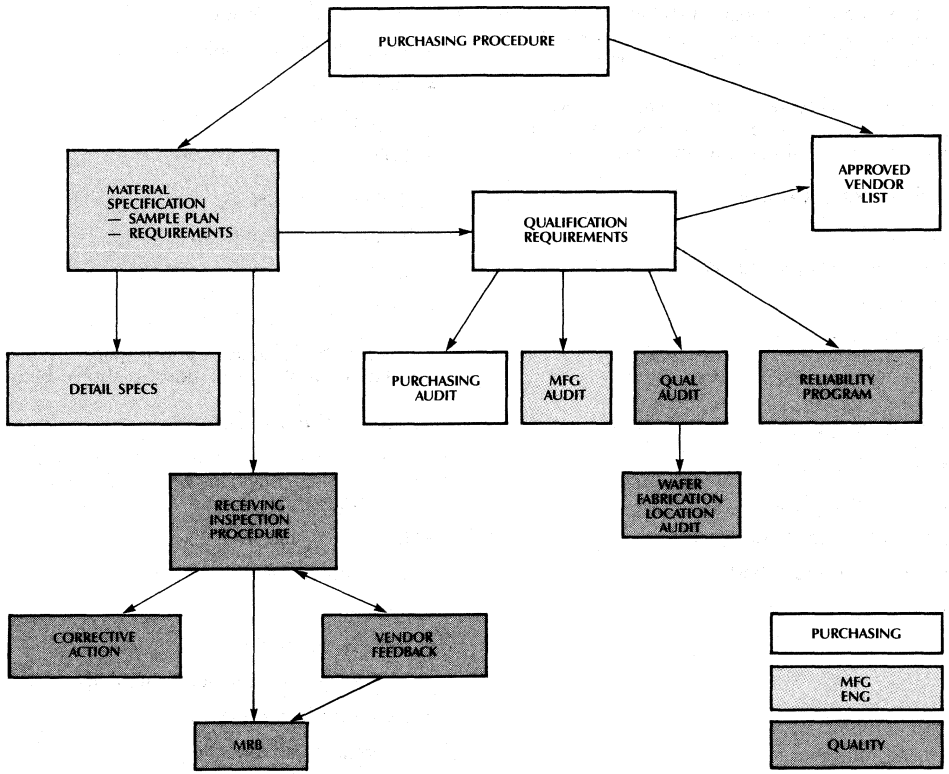


Figure 3. Vendor Control System

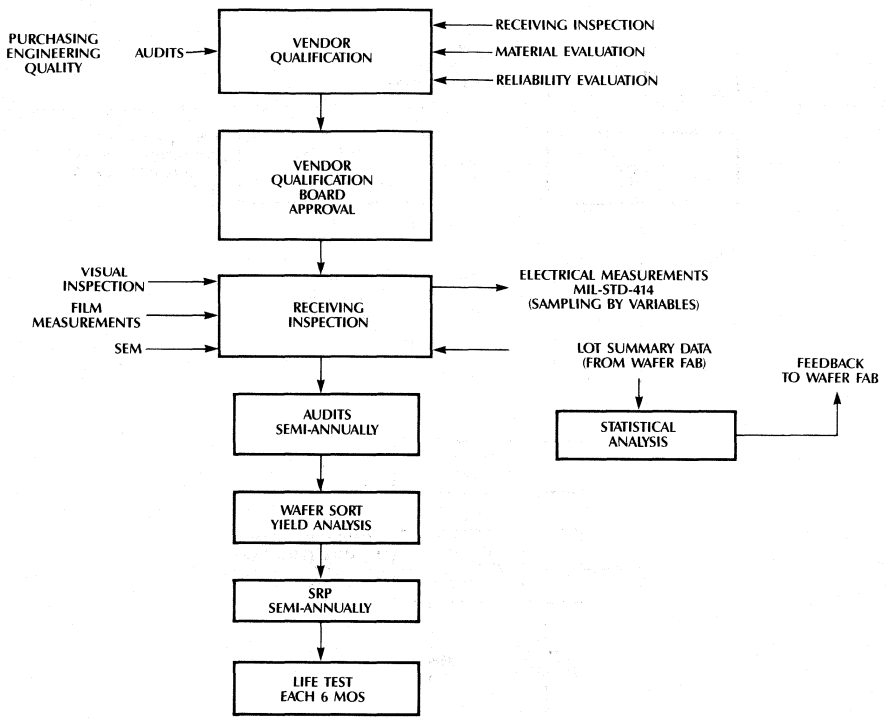


Figure 4. Process Control System

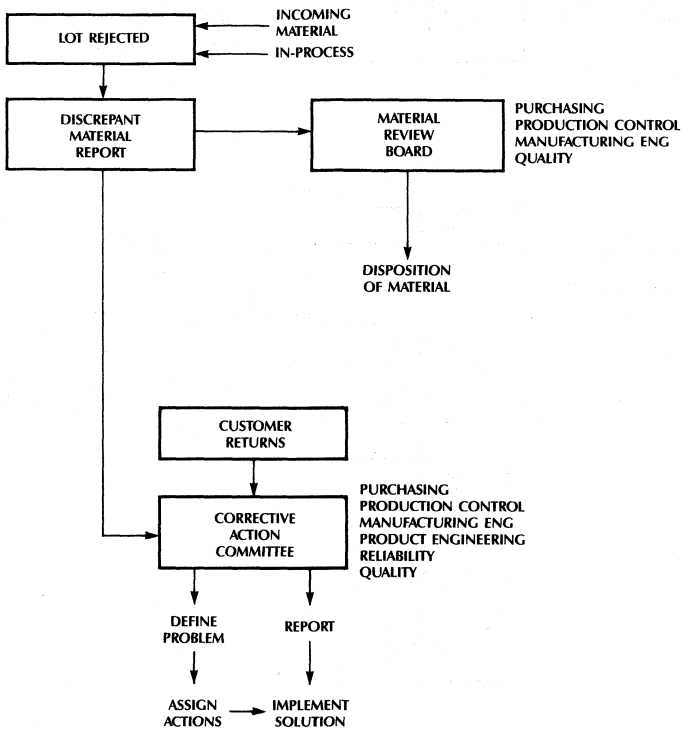


Figure 5. Corrective Action Program

APPENDIX A. Failure Rate Calculations

In order to predict the rate at which product will fail, it is necessary to accelerate the life of the product. This is most commonly done by a temperature and/or voltage stress, a process known as burn-in. The equation for both stresses is exponential, hence large acceleration factors can be achieved. In our studies, only temperature was used in the acceleration equation; the devices were biased at nominal voltages. The equation is shown below. It is known as the Arrhenius Reaction Rate Equation, named for the man who modeled the relationship between temperature and the chemical reaction property of materials.

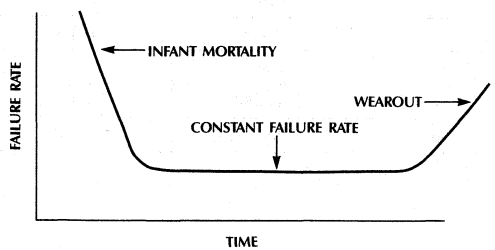
Arrhenius Reaction Rate Equation

$$Af = Exp\left[\frac{Ea}{K}\left(\frac{1}{T1} - \frac{1}{T2}\right)\right]$$

Af: Acceleration Factor
Ea: Activation Energy (in electron volts)
K: Boltzmanns Constant (8.67×10^{-5})
T1: Temperature of System Operation (°K)
T2: Temperature of Life Test (°K)

Burn-in when run for 1000 hours, is called "life test". Interim readouts normally occur at 160 and 500 hours. The hypothesis is that a "bathtub curve" will result. This curve, shown below, illustrates a device's failure rate versus time. Certain manufacturing defects have a tendency to cause failures early in the life of a device (infant mortality). The failure rate associated with these defects can be accelerated by applying stresses, such as temperature and voltage, which do not appreciably affect the normal failure rates or wear out mechanisms.

Bathtub Curve



Activation Energies

In order to calculate the acceleration factor, the activation energies for various failure modes encountered in the semiconductor industry are required. Initially, failure modes are assumed based on industry experience. As failures occur, they are rigorously analyzed and the failure modes then used to determine which activation energies are appropriate for determining failure rates. The following table describes the most common failure modes and their activation energies.

Table 1.

Failure Mechanism	Ea	Stress
Oxide Defects	0.3 eV	High Voltage Op Life
Contamination	1.0 eV	High Voltage Bias
Silicon Defects	0.5 eV	High Voltage
Metal Line Electromigration	0.5 eV	High Voltage Op Life
Contact Electromigration	0.9 eV	High Voltage Op Life
Masking Defects Assembly Defects	0.5 eV	Hi Temp. Storage Op Life
Microcracks	N/A	Temperature Cycling
Short Channel Charge Trapping	-.06 eV	Low Voltage Hi Vol Op Life

Acceleration Factors

Once the activating energy is determined for a given failure mechanism, the acceleration factor can be calculated using the Arrhenius equation. The following table lists some of the common activation engergies and its associated acceleration factors between different ambient temperature.

Table 2.

Est. T_J Accelerated Temperature	Estimated T_J, Typical Application Temperatures				Activation Energy (eV)
	25°C	40°C	55°C	70°C	
125°C	132	52	22	10	0.5
150°C	313	123	53	24	
125°C	1522	376	106	33	0.75
150°C	5530	1367	384	121	
125°C	6587	1231	268	67	0.9
150°C	30994	5793	1262	314	

8

Failure Rates

At Micro Linear, failure rate are generally stated at 60% confidence level using Chi square statistic per the following formula.

$$\lambda_{max} = \frac{\chi^2_{1-\alpha}\ [\text{width df} = 2(\gamma H)]}{2t}$$

where:

λ_{max} = maximum failure rate
χ^2 = chi square distribution
γ = number of failures
df = degree of freedom
t = total number of test hours
α = statistical error expected in estimate.
For 60% confidence level, α = 0.4 or 1-α = 0.6

Selected values of Chi Square distribution are listed in Table 3.

Table 3. Percentiles of the Chi Square Distribution. (Values of chi² corresponding to certain selected probabilities)

		60% Confidence Level	90% Confidence Level
Probability in %		60.0	90.0
1 - α		0.60	0.90
df	Total Failures		
1		0.708	2.71
2	0	1.830	4.61
3		2.950	6.25
4	1	4.040	7.78
5		5.130	9.24
6	2	6.210	10.60
7		7.280	12.00
8	3	8.350	13.40
9		9.410	14.70
10	4	10.500	16.00
11		11.500	17.30
12	5	12.600	18.50
13		13.600	19.80
14	6	14.700	21.10
15		15.700	22.30
16	7	16.800	23.50
17		17.800	24.80
18	8	18.900	26.00
19		19.900	27.20
20	9	21.000	28.40

Failure rate may be expressed a number of ways. Table 4 compares various ways of expressing failure rates.

Table 4. Failure Rates

NO. OF FAILURES PER DEVICE HOURS	FAILURE RATE	% PER 1000 HOURS	PPM (HOURS)	FITS	MTBF (HOURS)
$1/1 \times 10^9$	0.000000001	0.0001	0.001	1	1×10^9
$1/1 \times 10^8$	0.00000001	0.001	0.01	10	1×10^8
$1/1 \times 10^7$	0.0000001	0.01	0.1	100	1×10^7
$1/1 \times 10^6$	0.000001	0.1	1	1000	1×10^6
$1/1 \times 10^5$	0.00001	1	10	10000	1×10^5
$1/1 \times 10^4$	0.0001	10	100	100000	1×10^4
$1/1 \times 10^3$	0.001	100	1000	1000000	1×10^3

APPENDIX B. Radiation Hardness of 12V Bipolar Process

The Micro Linear 12V bipolar process has demonstrated selective hardness to radiation exposure. The components most commonly used in the 12V process which are described in table 1, were exposed up to 10^6 Rads total dose ionizing radiation. A second group of the same components were exposed to non-ionizing radiation of up to 10^{14} fluence neutrons/sq cm. Neither group was exposed to both types of radiation.

DESCRIPTION	BIAS DURING IRRADIATION	POST IRRADIATION MEASUREMENTS	FIGURES
Minimum Geometry NPN	V_{CES} = +5V	Δh_{fe}	1, 4
Lateral Quad Collector PNP	V_{CES} = -5V	Δh_{fe}	2, 5
Vertical PNP	V_{CES} = -5V	Δh_{fe}	3, 6
45Ω N+ Resistor	No bias	ΔR	3, 6
850Ω P+ Resistor	No bias	ΔR	3, 6
10KΩ Implanted P Resistor	No bias	ΔR	3, 6
10pF Capacitor	No bias	ΔI_L	3, 6

Table 1. Components

Figures 1 through 3 show the results of the ionizing radiation tests. Figures 4 through 6 show the results of the non-ionizing radiation tests.

* The resistors and capacitors were not significantly altered by exposure to these radiation levels. They are not included in the figures.

Summary

The h_{fe} of the NPN transistors degrade by approximately 50% at 10^5 Rads and 80% at 10^6 Rads. The PNPs degrade more severely by approximately 80% at 10^5 Rads and reach unity at 10^6 Rads. Degradation vs. neutron fluence is similar but less severe.

Micro Linear circuits, exclusively using NPN devices and passive components, can be designed to perform in a high radiation environment.

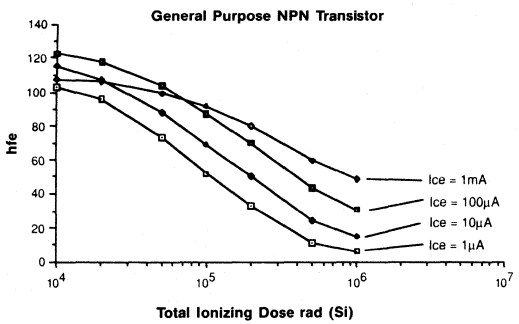


Figure 1.

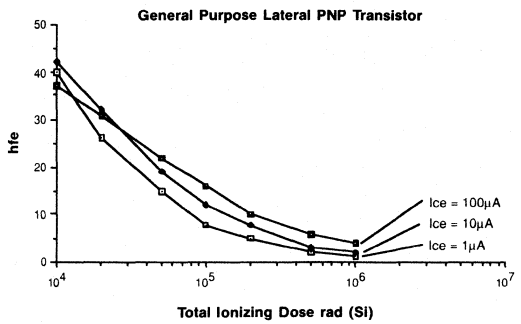


Figure 2.

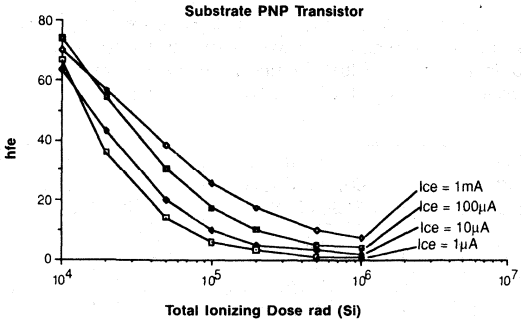


Figure 3.

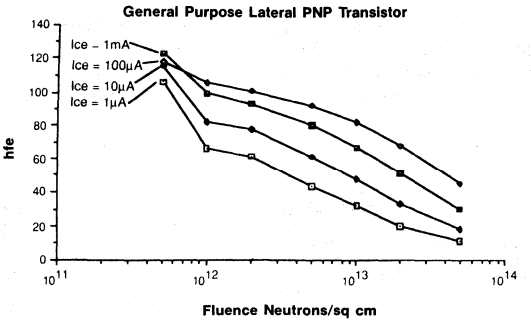


Figure 4.

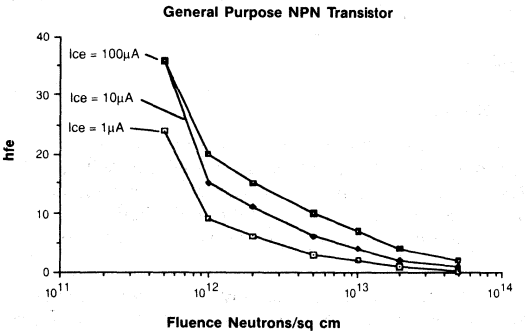


Figure 5.

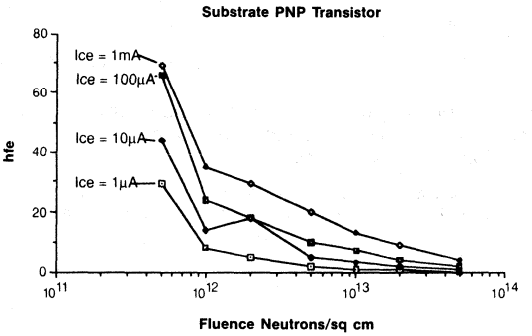


Figure 6.

/M8 Military Product Flow

Section 9

Military Product Flow

A specification to establish the general test methods and procedures for purchase of integrated circuits to military quality and reliability assurance requirements.

Micro Linear is committed to supplying the military marketplace with service, as well as, quality and reliable components second to none. The Micro Linear /M8 program is designed to provide off-the-shelf high integration linear integrated circuits with extended screening and testing utilizing the methods of MIL-STD-883C, Class B as its reference documentation.

The Quality and Reliability Assurance program at Micro Linear Corporation is a wide ranging program involving engineering and manufacturing designed to produce the highest quality linear integrated circuits available.

Wafer Inspection

Emphasis is placed on statistical analysis, electrical measurements on specially designed Process Control Monitors in accordance with MIL-STD-414 (sampling by variables), visual inspection, and film measurements. Potential reliability hazards are investigated and detected early by utilizing diagnostic and device structures on each wafer and periodic SEM analysis.

Assembly Inspection

Comprehensive receiving inspection for all materials and piece-parts is performed in accordance with the strictest quality assurance procedures. To assure conformance and control to specifications, documented quality control checks and monitors are performed on-line.

Testing

Micro Linear has invested in the latest "state-of-the-art" analog testers to achieve the most complete and thorough parametric testing of integrated circuits in the industry. Data sheets provide the customer a precise listing of parameters which are 100% tested. The calibration system is in compliance with MIL-STD-45662.

Traceability

For complete traceability to the wafer fab and assembly lot, a mark is placed on all units giving information on a unit-by-unit basis.

Micro Linear considers traceability to be essential for good engineering control and additional insurance for its customers. The information provided exceeds the seal week control required by MIL-M-38510.

ESD (Electro Static Discharge)

Products are fully characterized to MIL-STD-883C, Method 3015 and strict controls on handling and packaging are observed. A full ESD program, from design through manufacturing, incorporates training of all employees who handle Micro Linear products.

Major Change Control

Major change controls are in place to notify customers in accordance with MIL-M-38510. Micro Linear reviews all process, product, and package changes. All changes with possible impact are submitted for a re-qualification, which may include electrical, mechanical, and/or thermal characterization. Reliability requalification is performed if applicable.

Quality Assurance

Process monitors and gate inspections insure that all devices are properly tested and that the required sample tests are performed prior to shipment. Inspection records and reports concerning monitors and inspection data are utilized to status the quality level of products going through final test operations. Statistical sampling plans ensure the quality of the product.

Micro Linear welcomes OEM quality system surveys. Micro Linear is qualified by a number of customers to MIL-Q-9858A and MIL-I-45208 for military programs.

Failure Analysis and Reporting of Customer Returns

A formal program exists to record, analyze and take appropriate corrective action on all returns. A Corrective Action Committee reviews on a weekly basis all discrepancies and assigns responsibility to implement solutions or improvements. A report is generated and sent to the customer stating our findings and action.

/M8 Product Screening Flow

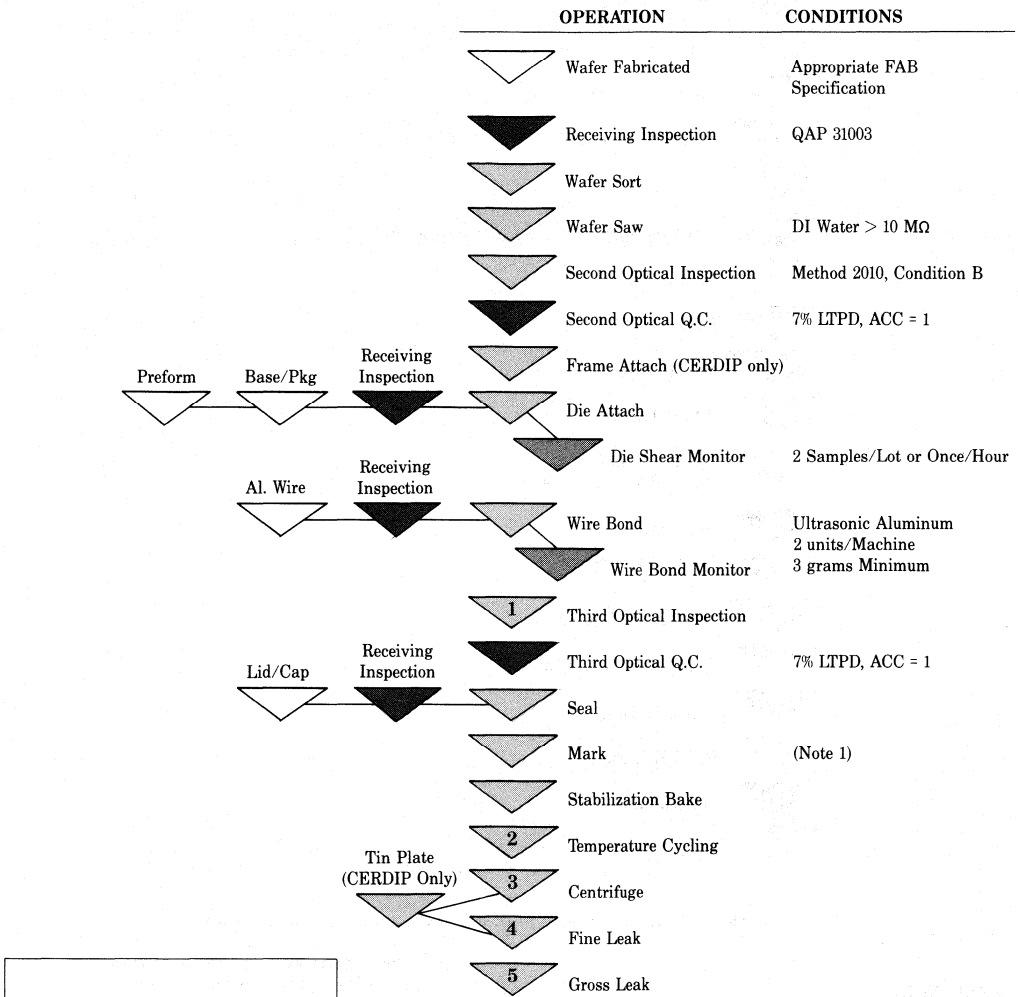
Micro Linear's standard extended screening process outlined below utilizes the methods of MIL-STD-883C, Class B as it's reference documentation.

Despite lower cost and faster delivery of the following standard /M8 flow, there are cases where a custom or special flow is required. Micro Linear is ready to discuss and accomodate custom flows to meet design or other mandatory requirements.

	OPERATION	CONDITION
1	100% Internal Visual	Method 2010, Condition B
2	100% Temperature Cycling	Method 1010, Condition C
3	100% Constant Acceleration, Y1 Orientation Only	Method 2001, Condition E
4	100% Seal Fine Leak	Method 1014, Condition A
5	100% Seal Gross Leak	Method 1014, Condition C
6	100% Pre Burn-In Electrical, 25°C	Data Sheet, 100% Noted Parameters
7	100% Burn-In, 160 Hrs at 125°C	Method 1015
8	100% Post Burn-In Electrical, 25°C	Data Sheet, Parameters Noted 100% Tested
9	Percent Defective Allowable Calculation	PDA = 5%
10	100% Final Electrical Test, -55°C and +125°C	Data Sheet Parameters Noted 100% Tested
11	QA Sample 116/0 Electrical Test, -55°C, +25°C, and +125°C	Group A, Subgroups 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11 Data Sheet Parameters Noted 100% Tested
12	Quality Conformance Inspection Test Sample Selection	Method 5005.11 Group B
A	Resistance to Solvents	Method 2015
B	Solderability, Soldering Temperature of 245 ± 5°C	Method 2022 or 2003
C	Bond Strength, Ultrasonic	Method 2011, Condition C or D
13	Sample LTPD = 2, C = 1 Seal Fine Leak	Method 1014, Condition A
14	Sample LTPD = 2, C = 1 Seal Gross Leak	Method 1014, Condition C
15	100% External Visual	Method 2009
SHIP		

/M8 Manufacturing Flow

Screening to the /M8 flow is part of the manufacturing flow shown below. The numbered steps correspond to the operations of the /M8 product screening flow.



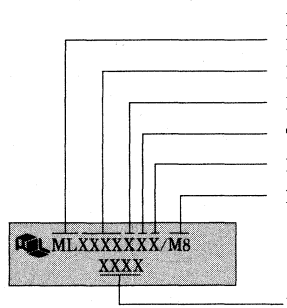
/M8 Manufacturing Flow (Continued)

	OPERATION	CONDITIONS
A	Marking Permanency	
	Lead Trim	
	Visual Inspection	
	Quality Monitor	7% LTPD, ACC = 1
	Pack and Ship	
	Receiving Inspection	PUR 34001 (Note 2)
6	Electrical Test	
7	Burn-in	
8	Electrical Test	
9	PDA Calculation	
10	Electrical Test, Min. and Max. Temperature	
11	Q.A. Sample	
12	Quality Conformance Inspection	
13	Q.A. Fine Leak Sample	
14	Q.A. Gross Leak Sample	
15	External Visual	
	Finished Goods	
	Shipping Inspection	QAP 35030
	SHIP	

OPERATION KEY

- incoming material
- production
- production or quality monitors
- quality inspection

Note 1: Marking of product screened to /M8 test methods and procedures is as follows:



Micro Linear prefix or for second source devices prefix is the same as original source
Four digit product part number
Number or letter indicates electrical grade of part
Temperature range (Example: "M" — 55°C to +125°C)
Package type (Example: "J" Hermetic Ceramic DIP)
Indicates /M8 processing
Four digit date code

Note 2: Country of origin may be United States, Korea, Hong Kong or Thailand.

/M8 Product Qualification

Generic data can be provided for the following qualification conditions or methods.

Actual qualification on a given lot can be performed on a customer lot basis. Contact your Micro Linear sales representative for any additional price adder and delivery information.

Group C Die-Related Tests

Test	Condition	Quantity/Accept No.
1. Steady-State Life (Burn-In Circuit Available Upon Request)	Method 1005 1000 Hr at 125°C or equivalent	LTPD 5
End Point Life Test Electricals 25°C	Data Sheet, 100% Noted Parameters	
	Group D Package-Related Tests	
1. Physical Dimensions	Method 2016	LTPD 15
2. a. Lead Integrity	Method 2004	LTPD 15
b. Seal Fine Gross	Method 1014 Condition A Condition C	
3. a. Thermal Shock	Method 1011 Test Condition B 15 Cycles	LTPD 15
b. Temperature Cycling	Method 1010 Test Condition C 100 Cycles	
c. Moisture Resistance	Method 1004	
d. Seal Fine Gross	Method 1014 Condition A Condition C	
e. Visual Examination	Method 1004 Method 1010	
f. End Point Electricals 25°C	Data Sheet 100% Noted Parameters	
4. a. Mechanical Shock	Method 2002 Condition B	LTPD 15
b. Vibration, Variable Frequency	Method 2007 Condition A	
c. Constant Acceleration	Method 2001 Condition E Y1 Orientation	
d. Seal Fine Gross	Method 1014 Condition A Condition C	
e. Visual Examination		
f. End Point Electricals 25°C	Data Sheet 100% Note Parameters	

REFERENCES

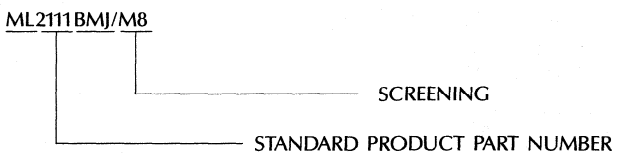
Government documents and specifications.

FED-STD-2090	Clean Room and Work Station Requirements, Controlled Environment.
MIL-M-38510	Micro Circuits, General Specification for.
MIL-Q-9858	Quality Program Requirements.
MIL-STD-414	Sampling Procedures and Tables for Inspection by Variables for Percent Defective.
MIL-STD-883	Test Methods and Procedures for Microelectronics.
MIL-STD-11331	Parameter to be Controlled for the Specification of Microcircuits.
MIL-STD-45662	Calibration Systems Requirements.

ORDERING INFORMATION

Product processed to the /M8 flow is ordered by adding /M8 to the standard product part number.

Example:



All /M8 product are shipped with a certificate of conformance. Information with regard to non-standard electrical testing or preconditioning, and wafer traceability may be obtained by contacting your Micro Linear sales representative.

Application Notes

Section 10

Micro Linear

Application Note 1

FB3600 Digital Logic Design

Micro Linear's Bipolar ASIC Technology allows the mixture of both analog and digital circuitry on an integrated circuit. Micro Linear has combined the advantages of TTL, and ECL logic on our FB3600 family of bipolar tile arrays. Our +5 volt version of ECL can interface to the outside world at standard TTL, CMOS or 10K ECL levels. It requires the use of only a standard +5 volt power supply. On-chip, gate propagation delay times as low as 2 nanoseconds are possible. High density ECL digital components occupy fifty percent of Micro Linear's FB3635 tile array. In addition, a certain amount of digital logic can be implemented on all of the FB3600 tile arrays.

Traditionally, 10K ECL logic uses -5.2 volts supply. This additional supply is only needed for applications requiring an external ECL logic interface. Our FB3635 and FB3621 tile arrays contain schottky components. These components are often useful for implementing high speed TTL & CMOS output drivers. On-chip ECL Logic requires a voltage reference which changes over temperature. Normally, on-chip voltage references are designed to be stable over variations in temperature. The schematic diagram for this circuit has been provided.

This application note has been designed to aid a design engineer using a workstation with Micro Linear's analog ASIC design libraries. The circuits provide basic building blocks which can be integrated on our FB3600 family of tile arrays. The circuitry and discussion provided in this application note provide a starting point for the design engineer's own workstation circuit design and simulations.

Two Input ECL NOR Gate

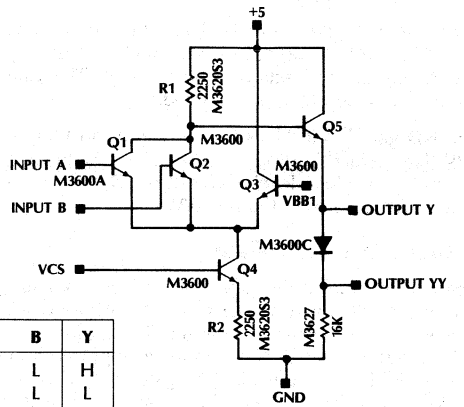
One of the major advantages of ECL logic is that the transistors never saturate. This plus the small signal swings reduce the propagation delay time through the gate. The propagation delay can be adjusted by changing the current level used by the circuit. The gate propagation delay decreases as the operating current level increases.

The ECL NOR gate, shown in figure 1, is designed for conventional +5 volt power supply operation. VCS is a preset bias voltage of 1.35 volts. This develops a voltage drop of 750mV across R2. The two ECL inputs (Input A & Input B) have a logic high (true) value of 4.25 volts and a logic low (false) value of 3.50 volts. VBB1 is a preset bias voltage which is about half way between the logic high and logic low voltages.

Micro Linear's single +5V operation is different from traditional 10K ECL logic which uses a single -5.2 volt supply. This establishes the 10K ECL logic high level in between -.810 and -.960 volts and a logic low level is in between -1.650 and -1.850 volts.

The NOR gate operates on the current flow from Q4. All the current from Q4 will be steered through either the Q3 leg or the Q1/Q2 leg of the circuit. If either Input A

Figure 1. NOR Gate



A	B	Y
L	L	H
H	L	L
L	H	L
H	H	L

or Input B logic voltage is high, all the current will flow up the Q1/Q2 leg of the circuit. This occurs because either or both transistors (Q1, Q2) have an input voltage which is above Q3 input voltage. Current flowing up the Q1/Q2 leg will cause a 750mV voltage drop to occur across R1 (same resistance as R2). This also results in Output Y being set at 5 volts minus 750mV minus 750mV (Q5 base to emitter voltage drop). Thus, Output Y is set at a logic low level (3.05 volts).

Both inputs need to be logic low for Output Y to have a logic high result (4.4 volts). In this case, the voltages on both Q1 and Q2 bases are less than the voltage on the base of Q3. This will cause all the current from Q4 to flow up the Q3 leg. The base of Q5 will be about 5 volts since the voltage drop across R1 is close to zero.

It is important to note that R1 always equals R2 and that the voltage drops (typically 750mV) across the base emitter will change with temperature. Since all the transistors on this IC are about the same temperature, they and the ECL voltage references will all track together with temperature. Thus the ECL logic works well over variations in temperature. The absolute values of the voltages stated above will change slightly with temperature. The values of resistors R1, R2, and R3 are adjusted for the desired speed vs power tradeoffs. The values shown in the NOR gate (figure 1) are typical values.

Figure 1 also shows an Output YY terminal. Some ECL logic gates need to have an extra diode voltage drop for its output. We will call this the "bias level B" output/input. The Output Y terminal does not have this extra diode voltage drop. Thus, we will call this the "bias level A" output/input.

Two Input ECL NAND/AND Gate

The basic operation of this gate's differential pair and the two output stages is very similar to the NOR gate discussion. The NAND/AND gates input stage requires Input A to be a "bias level A" input and Input B to be a "bias level B" input. A "bias level A" input needs to be driven by a "bias level A" output. Similarly, a "bias level B" input needs to be driven by a "bias level B" output.

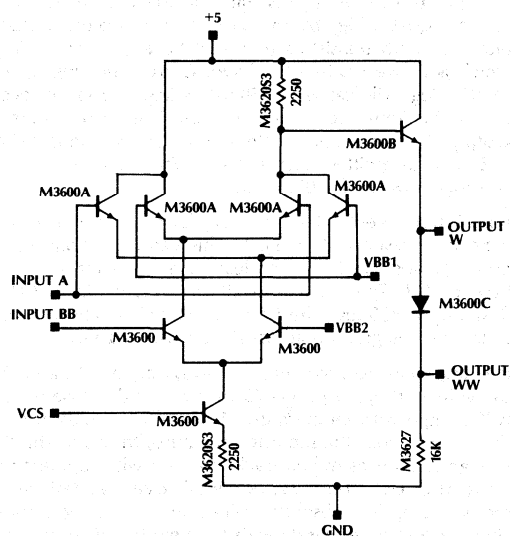
The NAND/AND gate shown in figure 2 has two output sections. The NAND output uses section A output stage. The AND output uses section B output stage. This gate can have either output stages omitted.

The NAND gate has its "bias level A" result on Output X and its "bias level B" output on Output XX. Similarly, the AND gate has its "bias level A" result on Output W and "bias level B" output on Output WW.

Two Input ECL XOR Gate

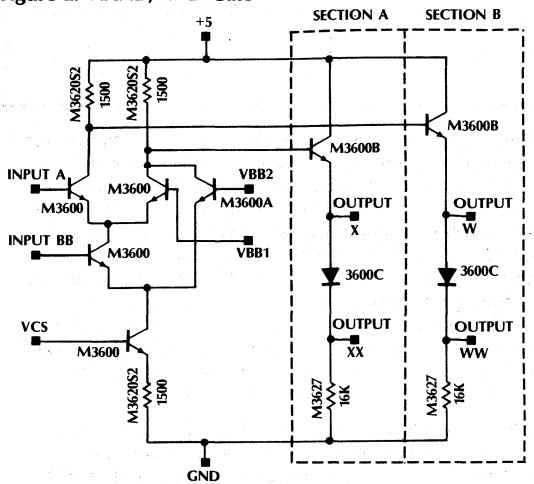
The basic operation of this gate's two differential pair and the output stages is very similar to the NAND/AND gate discussion. Figure 3 contains a circuit diagram for this gate. It uses one "bias level A" (Input A) input and one "bias level B" input (Input BB). The gates output is available as "bias level A" (Output W) and as "bias level B" (Output WW).

Figure 3. XOR Gate



A	B	W
L	L	L
H	L	H
L	H	H
H	H	L

Figure 2. NAND/AND Gate



A	B	X	W
L	L	H	L
H	L	L	L
L	H	L	L
H	H	L	H

ECL Data Latch

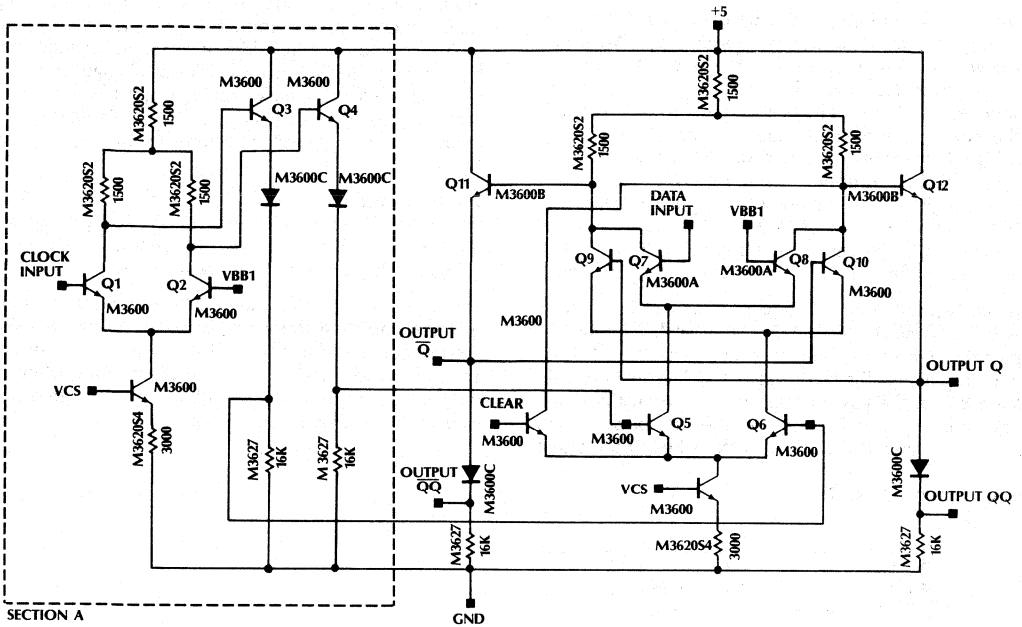
The circuit diagram for a single bit ECL data latch is shown in figure 4. As long as the Clock Input is logic high, the data latch will pass the data from the Data Input through to the output. If the input data changes, the output will track the change. This is called the pass through mode of operation. The pass through mode will end as soon as the Clock Input signal changes to logic low. When this transition occurs, the current value of input data will latch. The data latch will remain fixed as long as the clock remains low. Should the Clock Input return to the high state, the data latch will return to the pass through mode of operation. The data latch is level triggered instead of edged triggered.

Both the Clock Input and the Data Input are "bias level A" inputs. The "bias level A" outputs are Q and $\overline{Q}$. The "bias level B" outputs are QQ and $\overline{QQ}$.

When the Clock Input is high, the current value of the Data Input will be present at the Q and QQ outputs. An inverted version of Data Input will be present at the $\overline{Q}$ and $\overline{QQ}$ outputs. When the Clock Input is low, the latched value of the previous Data Input will be present at the Q and QQ outputs.

The data latch circuit contains circuitry to adjust the Clock Input signal. The circuitry shown in section A contains a circuit for converting a "bias level A" logic input into two "bias level B" output signals. The two output signals reflect the input signal and a complement of the input signal.

Figure 4.



The "bias level A" clock input signal drives the base of Q1. Transistor Q1 and Q2 form a different pair. The base of Q2 is driven by a reference voltage which is midway between logic high and logic low. When the Q1 input signal is high, the current will flow only through the Q1 leg of the differential pair. This will cause the collector of Q1 to have a voltage of about 4.25 volts and the collector of Q2 to have a voltage of about 5 volts. Substantial current will now flow through Q3. Thus, a "bias level A" logic low is present at the emitter of Q3. The diode in series with Q3 emitter shifts the output voltage to a "bias level B" output. This "bias level B" output will have a logic low value. Note that the Q3 outputs represent the complement of the Clock Input signal. Thus, a low Clock Input signal will result in a logic high output at the emitter of Q3.

A buffered version of the Clock Input signal is provided. This output will have the same logic level as the Clock Input signal. A "bias level A" version of the Clock Input signal is available at the emitter of Q4. The diode in series with Q4 emitter shifts the output voltage to a "bias level B" output.

The buffered Clock Input signal and its buffered complement will drive the bases of Q5 and Q6, respectively. When the data latch is in the data pass through mode (Clock Input high), transistor Q5 is turned on and transistor Q6 is turned off. If the Data Input is logic high, all of the current in the differential pair (Q7 & Q8) will flow in the Q7 leg. The current flow through the resistor in the Q7 leg will produce a 750mV drop. This sets the collector of Q7 at 4.25 volts. This will cause Q11 emitter to be at "bias level A" logic low (output $\overline{Q}$). Output $\overline{QQ}$ will be "bias level B" logic low. The lack of current flow in the Q8 leg will cause the collector of Q8 to be at about 5 volts. This will cause the emitter of Q12 to be logic high ("bias level A"). Output QQ will be at "bias level B" logic high.

When the Data Input is logic low, then all of the current will flow through the Q8 leg. Transistor Q11 emitter will now be at logic high. Output $\overline{QQ}$ will be at "bias level B" logic high. Transistor Q12 emitter will now be at logic low and the output QQ will be at logic low.

The data latch will store the current state of the output when the Clock Input signal changes to logic low. This will cause transistor Q5 to turn off and transistor Q6 to turn on. The base of Q9 gets its input from output Q. The base of Q10 gets it's input from the output $\overline{Q}$. Since it takes a few nanoseconds for Q11 and Q12 to change state after the input data changes, the data latch is now getting its input data from the previous output data. This feedback loop causes the data latches output to remain fixed.

The data latch also contains a CLEAR input. This input should normally be logic low ("bias level B"). A logic high will reset the data latch to logic low. As long as the CLEAR input is logic high, the data latch will remain reset.

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One Bit ECL Register or Flip Flop

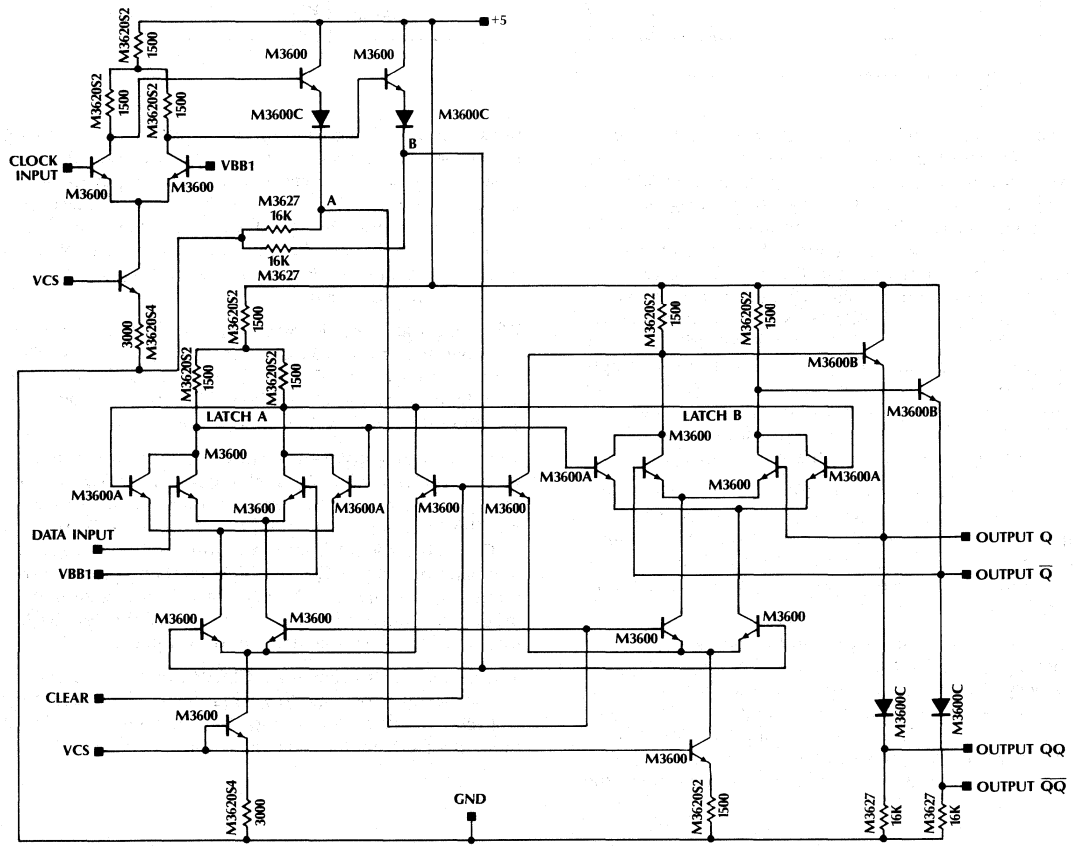
The circuit shown in figure 5 can be used as a single bit positive edge triggered register or as a flip flop. We shall first review its operation as a one bit register. This circuit latches the Input Data upon the Clock Input changing from logic low to logic high. The data will remain latched until the next time the Clock Input changes from logic low to logic high. Similar to the data latch circuit, the Clock Input and Data Input signal are both "bias level A" inputs. The register has four outputs. The outputs are available in both "bias level A" (Q and $\overline{Q}$) and "bias level B" (QQ and $\overline{QQ}$). The register's stored value (Q and QQ) and its complement value ($\overline{Q}$ and $\overline{QQ}$) are also provided.

This circuit is simply two data latches in series. Both data latches use a common clock. When one latch is in the data pass through mode, the other latch is latched. When the Clock Input signal is high, data latch A is latched and data latch B is in the pass through mode. When the Clock Input signal is low, data latch A is in the data pass through mode and data latch B is latched. If the Clock Input signal changes from low to high, latch A will latch its current input data and data latch B will pass data latch A output values directly to its output. This can change the data register's output. If the Clock Input signal changes from high to low, the output data will not change since latch B will latch itself using data provided by latch A previous outputs. Note that a flip flop can be implemented by connecting the register's $\overline{Q}$ output to the register's Data Input.

The register also contains a CLEAR input. This input should normally be logic low ("bias level B"). A logic high will reset the register to logic low. As long as the CLEAR input is logic high, the register will remain reset.

The Clock Input circuit has two "bias level B" outputs (point A and B). If these output connections are switched, the register will latch upon a logic high to low transition. This will cause it to be in pass through mode whenever the Clock Input is low. The data register will latch its data whenever the Clock Input is high.

Figure 5. Register or Flip Flop

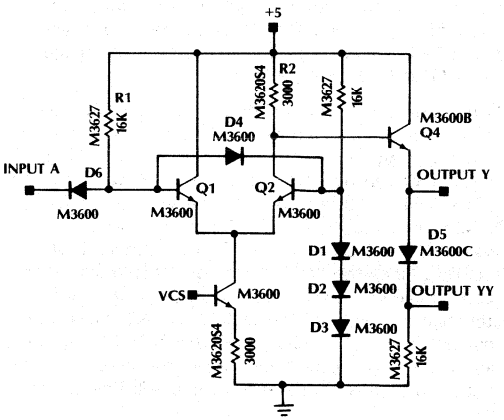


TTL and CMOS Input Interface Circuit

This circuit, shown in figure 6, converts a TTL or CMOS logic level input into an on-chip ECL level input. Output Y is a "bias level A" version of Input A. Output YY is a "bias level B" version of Input A. Transistors Q1 and Q2 forms a differential pair. The string of three diodes (D1, D2, and D3) sets the base of transistor Q2 at 2.25 volts. Given a high TTL/CMOS logic level drive at Input A, resistor R1 will bias the base of Q1 to be above the base Q2. This will cause all of the current to flow through the Q1 leg of the differential pair. Since the voltage drop across R2 will be about zero, the base of Q4 will be at 5 volts. The emitter of Q4 will be "bias level A" logic high. A "bias level B" version of this output will be produced at Output YY.

When Input A is driven by a TTL/CMOS low logic level, the base of Q1 will be biased below the base of Q2. Now all of the current will flow through the Q2 leg of the differential pair. The current flow will causes a 750mV voltage drop to occur across R2. The emitter of Q4 (Output Y) is now set at a "bias level A" logic low. Diode D5 produces a "bias level B" version of this output.

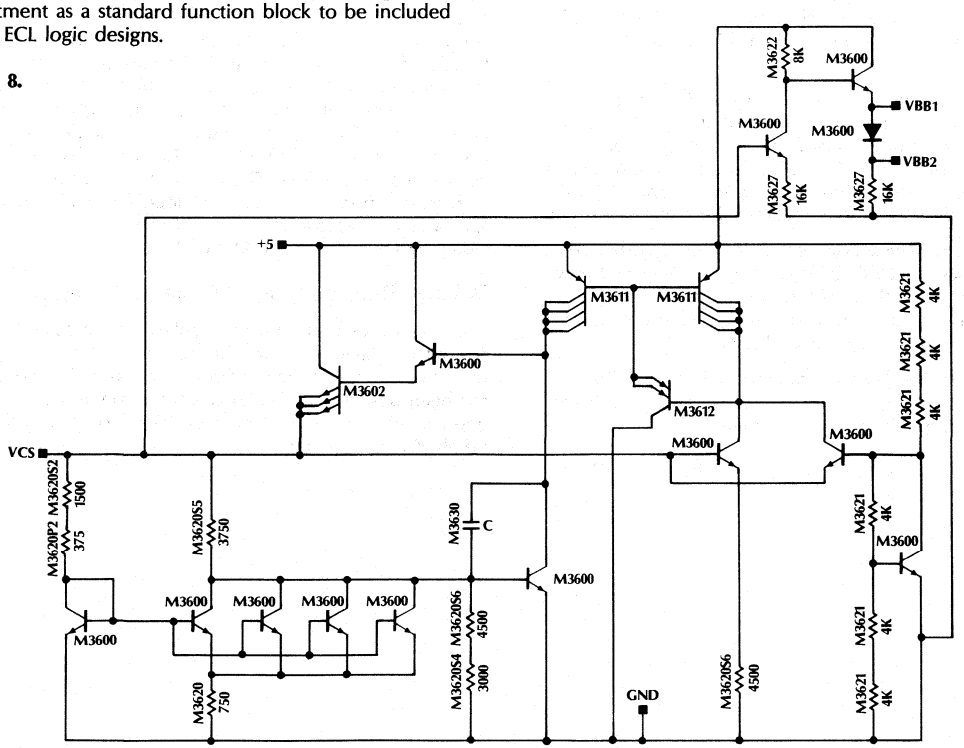
Figure 6. Input Interface



Voltage Reference for FB3600 ECL Logic

The circuit shown in figure 8 supplies the necessary reference voltages for our ECL logic. It has been designed to vary the output voltage with temperature. This block has been designed by Mirco Linear's engineering department as a standard function block to be included on all ECL logic designs.

Figure 8.



On-chip ECL to TTL or CMOS Output Interface

The circuit shown in figure 7 takes an on-chip "bias level A" ECL input and produces a TTL/CMOS compatible output. If the input is logic high (true) then the output will be logic high (true). The circuit simply buffers and shifts the logic voltage level from on-chip ECL voltage levels to TTL/CMOS voltage levels.

Section A contains circuitry similar to the CLOCK input for the data latch circuit. It converts the input into two signals (buffered version and a complement buffered version). If the input is driven by a high logic level, Q1 will be turned on and Q2 will be turned off. This causes the base of Q3 to be 4.25 volts and the base of Q4 to be 5 volts. Transistors Q3 and Q4 drives the bases of Q5 and Q6 respectively. Since the base voltage of Q4 is greater than the base voltage of Q3, the base voltage of Q6 will be greater than the base voltage of Q5. This will cause all of the current in the Q5 & Q6 differential pair to flow in the Q6 leg. If Input A is driven by a logic low level, all of the current in the Q5 & Q6 differential pair will flow in the Q5 leg.

The collector of Q6 drives the final output circuitry in section B. When Input A is at logic high, the collector of Q6 will be at .9 volts. The voltage drop across the base and emitter (.75 volts) of Q7 and Q8 will result in the bases of Q11 and Q12 being driven by less than .2 volts. Transistors Q11 and Q12 will be switched off. Since Q11 is off, the base of Q13 will be close to 5 volts. This turns Q13 on and results in a voltage of about 4.2 volts at the Output.

If Input A is at logic low, the collector of Q6 will be at 1.5 volts. The voltage drop across the base and emitter of Q7 and Q8 will result in the bases of Q11 and Q12 being driven by about .9 volts. This will turn on Q11 and Q12. With Q11 turned on, Q13 will be turned off and Q12 will be switched on. The output voltage will be about .75 volts.

We have just reviewed how section A circuitry drives the differential pair of Q5 & Q6. We have also reviewed how the collector of Q6 drives the output drive circuitry contained in section B. Next, we will examine how the Q5 & Q6 differential pair have been biased.

Section D contains a circuit known as a base emitter voltage multiplier. The voltage at the collector of Q15 will be determined by the following equation,

$$\text{Voltage at collector of Q15} = [1 + (R1/R2)] \times .75$$

The value of R1 and R2 is 10KΩ and 4KΩ respectively. The .75 represents the typical voltage drop across a transistors base to emitter. This sets voltage at the collector of Q15 at 2.6 volts. The voltage drop across the base and emitter of Q14 will set the collector voltage of Q5 at 2.6 – .75 = 1.85 volts.

When all of the current flows in the Q5 leg of the differential pair (Q5 & Q6), there will not be a voltage drop across the circuitry in section E (no current flow). The collector of Q6 is now set at 1.85 volts. If all of the current flows in the Q6 leg of the differential pair, there will be a .75 voltage drop across the diode. This sets the collector of Q6 at 1.1 volts.

The circuitry in section F provides a bias current for a current mirror. Resistor R3 value was chosen for a .5mA current flow with a 4.4 voltage drop across it. This input bias current generates the base to emitter voltage for Q16 which drives the bases of Q17, Q18, Q9 and Q10. Each of these transistors will sink .5mA.

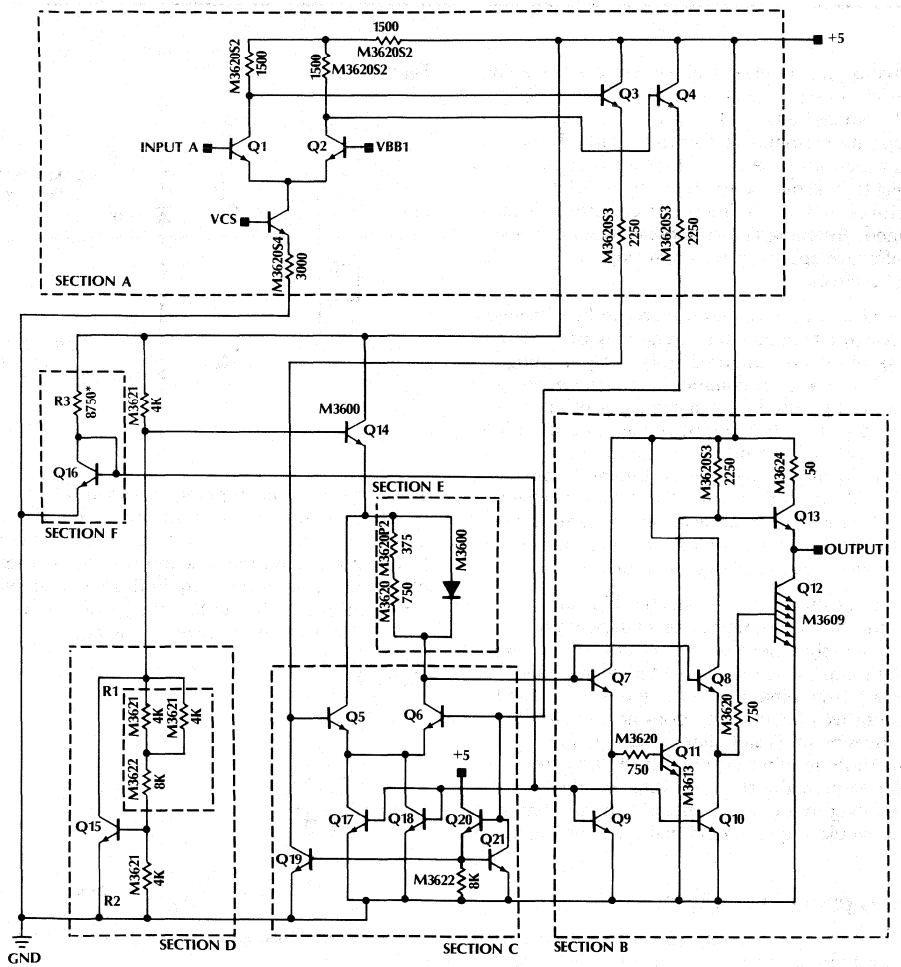
Transistors Q19, Q21 and Q20 also form a current mirror. Transistor Q20 and its 8K emitter resistor have been added for stability. The purpose of the current mirror is to keep the curent flowing through Q3 and Q4 approximately equal.

Transistors Q11 and Q12 are schottky clamped transistors. They consist of a npn transistor with a schottky diode connected between the base and the collector. The function of this diode is to limit the current flowing into the base. This prevents the transistor from saturating. The schottky diode sends the excess base current into the collector. This limits the voltage drop across the collector and the emitter to about 200mV. The typical base emitter voltage drop is .75 volts. These devices can be replaced with regular npn transistors if the logic's switching rates are low (a few MHz). Saturated transistors have much slower switching times than non saturated transistors.

Voltage Reference for FB3600 ECL Logic

The circuit shown in figure 8 supplies the necessary reference voltages for our ECL logic. It has been designed to vary the output voltage with temperature. This block has been designed by Mirco Linear's engineering department as a standard function block to be included on all ECL logic designs.

Figure 7. Output Interface



* BUILD UP OUT OF M3620s

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Micro Linear

Application Note 2

Trimming Analog Bipolar Arrays

High performance analog integrated circuits are becoming a necessity in the design of state of the art analog/digital systems. With standard analog IC's this requires the designer to specify premium performance parts. These same premium performance circuit functions are not typically available in semicustom arrays. By utilizing trimming techniques, though, improved performance can still be obtained. Trimming analog bipolar arrays is a very viable, cost effective approach for improving the key parameters of a circuit.

If tighter specifications are required than can be obtained using good design techniques the circuit may be trimmed at the wafer level by a technique of selectively shorting zener diodes. This is known commonly as zener zapping. This technique can be used to trim the input offset voltage of an op amp or the output voltage of a precision reference. For example, the offset voltage of our MLC350[1] operational amplifier can be trimmed from a maximum of 7mV to less than 1mV. The MLC340 voltage reference can be trimmed to an accuracy of better than 1%. Many types of parameters may be trimmed within the limitations of the technique as described below.

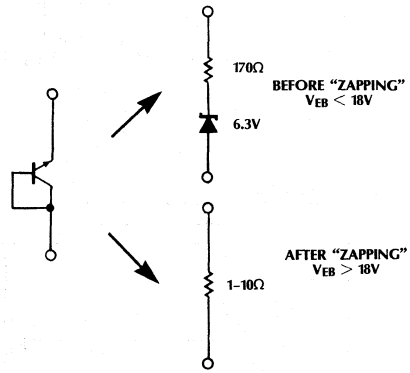
Although there are other ways in which a bipolar integrated circuit may be trimmed, zener zapping has become well established because it does not require extra processing steps and can be implemented at the wafer level. Unlike laser trimming, the technique is not limited to altering a resistive element, and does not require a large capital investment. Fusible links, another well-established method, requires currents in the ampere range in order to blow the standard 1 micron thick aluminum, resulting in a questionable blown connection. A thinner link would require additional wafer processing steps.

The Zener Zapping Technique

This process is called zener zapping because the emitter-base diode of a bipolar transistor is permanently shorted by passing a relatively large current through it while in the reverse breakdown avalanche mode. It produces a reliable 1-10 ohm link between the emitter and base pads. (See Fig. 1) This is a very reliable connection because of the double short which actually occurs. The first short is caused by the destruction of the pn junction. In addition, the presence of a large electric field during thermal runaway causes metal to migrate across the silicon surface beneath the oxide layer, producing a second short.

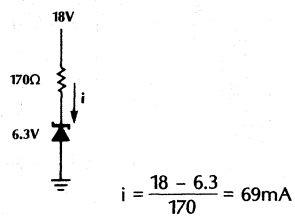
This set of events occurs when the voltage across the emitter-base junction is increased beyond the 6.3V

Figure 1.



avalanche breakdown point, to above 18V. At about 18V the instantaneous power dissipation exceeds 1.2W (figure 2) and an oscillatory, thermal runaway condition occurs. In less than a second the junction is destroyed leaving a 1-10 ohm short. The current required is less than 300mA, so remote probe pads (the bonding pads) can be used without damage to the pads or traces.

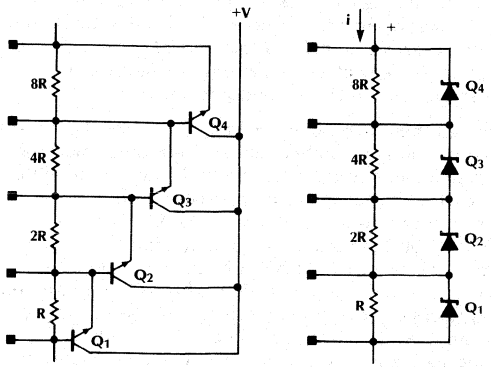
Figure 2.



Power Dissipation = iV = (69mA)(18V) = 1.24W

The circuit in figure 3 illustrates a simple implementation of this technique to alter the total resistance of a circuit path. Before any of the zeners are blown the total resistance equals 15R. This value can be altered to equal any integer multiple of R from 1R to 15R by selectively blowing only four zeners in a binary fashion. This is possible due to the binary arrangement of the resistor values. For example, to obtain a resistance of 5R, Q_2 and Q_4 should be shorted resulting in 4R + 1R = 5R. Note that 5 equals 0101 in binary which is represented by Q_4, Q_3, Q_2, Q_1 with shorts being 0's and opens being 1's.

Figure 3.



This type of circuit arrangement has two restrictions of which the designer should be aware. During normal operation of the circuit, the current through the resistor string should not be allowed to flow opposite to the direction indicated in the drawing. This would forward bias the base-emitter junction of the transistors, and effectively short out a resistor intended to be used. In addition, the forward voltage drop across each of the resistors should not exceed the zener breakdown voltage, about 6.3V. This would allow current to flow out of the resistor string and through the zener, altering the intended operation of the circuit.

The preceding example illustrates the use of zener zapping to alter a resistive element in a circuit. In many cases modifying a current source is a more useful way of trimming a design. Figure 4a shows trimmable current sources used to reduce the input offset voltage of an op amp.

In this example the balance of current in two circuit paths is altered using zener zapping. This technique is particularly useful for reducing the input offset voltage of an operational amplifier which has added emitter degeneration in the input stage in order to improve slew rate (figure 4b). The emitter resistors used in this circuit, R_6 and R_7, will contribute significantly to the offset voltage of the input stage. By modifying the balance of current between I_A and I_B the increased offset voltage V_{OS} can be compensated. In this example there are again 4 bits of trimming resolution with the 3 least significant bits controlling one current path and the most significant bit controlling the other. With this configuration the balance of current can be altered in either direction. In other words, the current in T_1 can be increased or decreased relative to T_2.

Figure 4a.

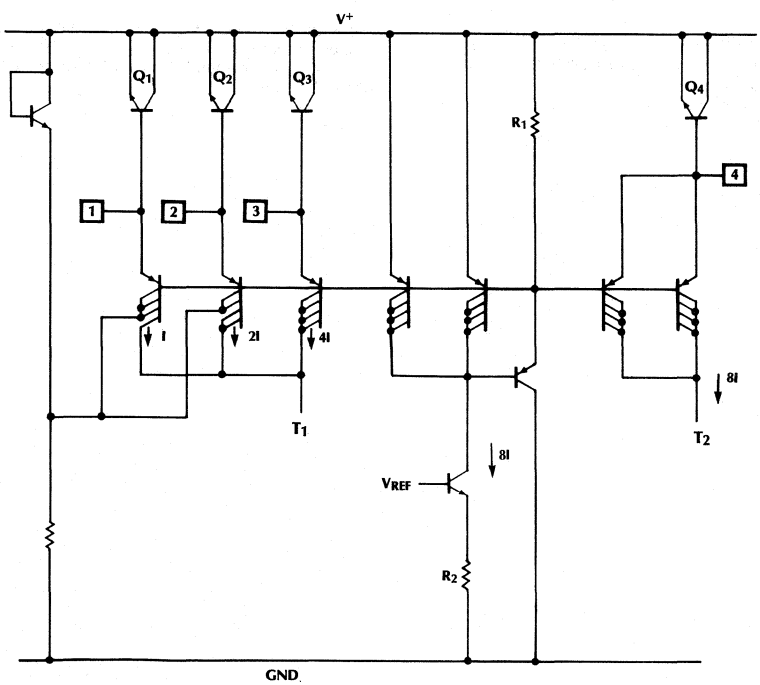


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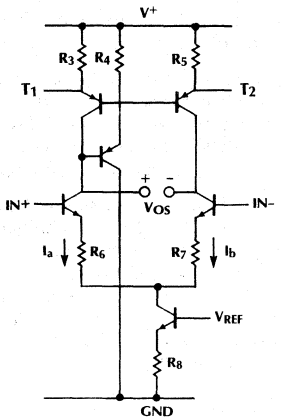
Figure 4b.



To increase the current through T_1 relative to T_2 you simply short Q_1, Q_2, and Q_3 in a binary fashion to get increments of I from 1I to 7I. To increase the current through T_2 relative to T_1 you short Q_4 which increase the current through T_2 by 8I. Then if you want less current, short Q_1, Q_2, and Q_3 in a binary fashion to offset the increase in T_2 by increments of I down to 1I.

The source of current in the trim circuit should be of the same type as the circuit to be trimmed so their temperature coefficients will match. In this case the V_{REF} in both circuits should be the same, and resistors R_2 and R_8 should be of the same type.

Shorting zeners is an irreversible process. Thus, it is important to check the results of a trim bit pattern before actually destroying the junctions. This is done by shorting the probe pads externally in the desired pattern through relays. In this way all combinations can be tried and the best results can be chosen and implemented.

Although these two examples both use 4 bits (4 zeners) to trim a circuit, any number can be used to get more or less resolution. The designer should be aware though of the practical limitations of each circuit to be trimmed. Other error terms like temperature coefficients will eventually become significant, and additional trimming beyond this point would be fruitless. In addition, the more zeners you use, the more probe pads are required. In a full custom circuit where minimum die size is the ultimate goal, the additional die area required for the diodes, pads and trim circuitry may become significant. An array, however, typically has unused components available for the trim circuitry, and you only have to be concerned with the number of bonding pads available. If all of the pads are already being used for pinouts then a larger array would be required.

These examples illustrate the usefulness and flexibility of zener zapping. There are many other potential applications for this technique though, and with a good understanding of the basic diode shorting process the design engineer can be creative in its application.

[1] The MLC350 is one of the circuits in Micro Linear's library of macrocells. Performance details of this circuit and other macrocells can be found in the FB300 Macrocell and Component Library booklet.

Design Techniques for Low Input Bias Current

Analog systems often require high impedance inputs to accommodate the demand for higher accuracy. Measurement systems which interface to photodetectors or high impedance transducers require devices with low offset voltage and low input bias current. This is necessary to receive and amplify the signal without introducing any significant errors. Under this constraint, the designer will often select a FET as the primary input device. Although a FET input stage may be appropriate in a discrete circuit design, there are other all bipolar techniques which are just as effective and better suited to an analog array. In some cases, these techniques will out perform the FET alternative.

This application note describes three alternatives for obtaining low input bias currents. The design techniques described can be applied to many different types of circuits from simple emitter followers to complex amplifiers. For example, a typical all bipolar operational amplifier can achieve input bias currents of about 100nA with an offset voltages of about 1mV[1]. Unfortunately these characteristics are still not good enough for many of the applications previously mentioned. The input bias current can be minimized by using one of the following design techniques, **1)** reducing the collector current **2)** using a Darlington configuration **3)** employing current cancellation techniques. This document will briefly describe the first two methods but will provide a detailed analysis of the cancellation technique as it provides the best performance trade-off and is the most involved.

Reducing the Collector Current

The simplest approach to achieve low input bias current is to reduce the collector current of the input transistors. Since the base current tracks the collector current by a factor of beta, reducing the collector current of the input transistors will reduce the input bias current into the bases. Beta will degrade at lower collector currents (figure 1), however, setting a practical limitation on this technique at about 50pA base current. If the circuit does not require a high slew rate or high gain bandwidth, this may be an acceptable method.

The Darlington Configuration

Figure 2 shows a differential Darlington configuration which will reduce the input bias requirements by a factor of beta. It will also double the offset voltage and reduce the voltage gain by 2. The offset voltage doubles due to the additional mismatching of the added devices, while the voltage gain suffers because only one-half of the input signal appears across the inner pair of transistors. A higher slew rate and gain bandwidth, though, can be achieved with this technique, over simply reducing the collector current, but it requires more components.

Figure 1. Current Gain vs. Collector Current

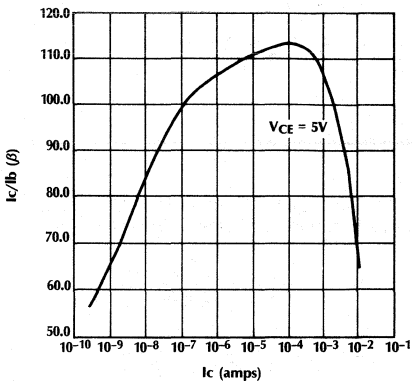
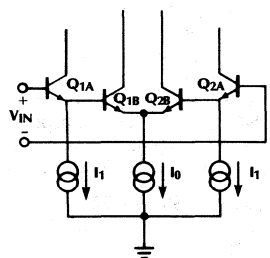


Figure 2.



$I_1 \ll I_0$

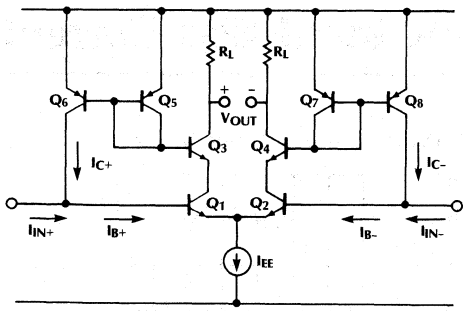
The Cancellation Technique

An all bipolar solution to low input bias current with low offset voltage while maintaining high collector currents for noise, slew rate or bandwidth reasons requires a technique called Input Bias Current Cancellation.

Input bias current cancellation is a circuit design technique which measures the input current and forces an equivalent amount back into the input nodes (figure 3). Ideally, this results in perfect cancellation of the input current. In the circuit in figure 3, the base currents into Q_3 and Q_4 duplicate the base currents into Q_1 and Q_2. These currents are then sensed by Q_5 and Q_7 and equivalent currents are fed back, via Q_6 and Q_8, into the input nodes. The total current at each input is thus,

$$I_{IN} = I_B - I_C$$

Figure 3.



Assuming all PNP betas (β_P) are equal, all NPN betas (β_N) and all base-emitter voltage drops are equal,

$$I_C = I_B \frac{\beta_N}{(1+\beta_N)} \frac{\beta_P}{(2+\beta_P)}$$

$$I_{IN} = I_B \left(1 - \frac{\beta_N}{(1+\beta_N)} \frac{\beta_P}{(2+\beta_P)}\right)$$

If all betas are very high,

$$I_C = I_B$$
$$\text{so}$$
$$I_{IN} = 0$$

The main contributor to cancellation errors in this circuit is the low beta of the PNP devices. This sets a practical limitation on this technique at about 5–10% of the uncanceled current, as shown by the following example.

Assumptions: $\beta_N = 100$, $\beta_P = 30$, $I_B = 70nA$

$$I_{IN} = 70 \left(1 - \frac{100}{1+100} \frac{30}{2+30}\right)$$

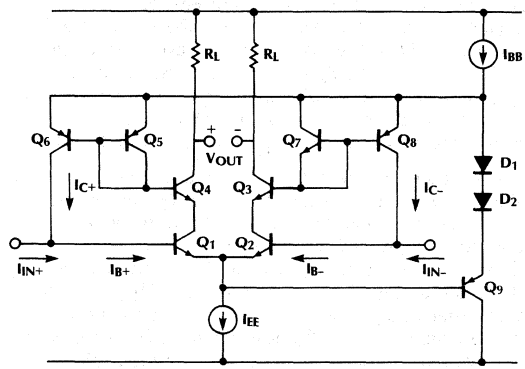
$I_{IN} = 70\ (.0718)$

$I_{IN} = 5nA$

This technique does not reduce the input *offset* current. In fact, the additional circuitry, with its additional mismatches, increases the offset current by a factor of about 3. The input bias current can be reduced to about the same value as the offset current, setting the limitation on this technique at about 1–10nA.

In the equations above, the betas of PNPs in the current mirror were assumed to be equal. To enhance the viability of this assumption, the V_{CE} of each PNP should be kept equal. With the cancellation circuitry tied to the positive supply the V_{CE} of Q_6 and Q_8 will change with the input voltage, while the V_{CE} of Q_5 and Q_7 will remain constant. This further aggravates any beta mismatch which already exists. To reduce this effect the circuit can be self-biased using current source I_{BB}, diodes D_1 and D_2, and transistor Q_9, as shown in figure 4.

Figure 4.



This circuit keeps the voltage across the cancellation circuitry fixed as the input common mode voltage changes, which in turn keeps the beta of each device constant.

These techniques for reducing input bias current demonstrate the reality of achieving levels sometimes thought only possible with JFETs or MOSFETs. Circuits being considered for analog array integration which contain discrete FETs or FET input op amps should not be categorized as not possible. Rather, each individual circuit should be analyzed for its critical parameters, keeping in mind the trade-offs described above. If none of the bipolar solutions is adequate an external FET can always be used as an input buffer.

(1) The offset voltage can be reduced by making use of wafer trimming techniques. At Micro Linear a process called zener zapping is used. For more information about this process see the application note titled "Trimming Bipolar Arrays".

Micro Linear

Application Note 4

High Frequency Complex Filter Design Using the ML2111

Charles Yager
Carlos Laber

1.0 Introduction

Switched capacitor filters have been growing in popularity because of their advantages over active filters. Switched capacitor filters don't require external precision capacitors like active filters. Their cutoff frequencies have a typical accuracy of ±0.3%, and they are less sensitive to temperature changes. This allows consistent, repeatable filter designs. Another distinct advantage of switched capacitor filters is that their cutoff frequency can be adjusted by changing the clock frequency. Switched capacitor filters offer higher integration at a lower system cost.

Until the introduction of the ML2111, commercially available switched capacitor filters were limited to about 20 KHz center frequencies. The ML2111 uses the versatile architecture of the MF10 with enhanced performance to reach center frequencies of up to 150 KHz with Q values up to 20.

Designing high frequency, high order filters using the ML2111 is the main topic of this application note. Particular attention is focused on mode 1c, which has the advantage of operating at high frequencies while allowing the center frequency to clock ratio to vary based on external resistors. A flexible building block is introduced which implements all the necessary types of bi-quads to realize high order complex filters. Finally an example is given which illustrates the design of an eighth order Elliptic bandpass filter with a center frequency of 90 KHz and a passband from 81 KHz to 100 KHz.

The first part of the application note covers a variety of issues: layout, how fast the system clock can be changed for sweeping filters, and some differences between continuous and sampled data filters. For the reader who is already familiar with sampled data filters, section 2 on Effects of Sampling, Aperature, Aliasing, and Signal Reconstruction may be skipped.

2.0 Effects of Sampling

Since the ML2111 is a switched capacitor filter, it behaves as a sampled data system. Switched capacitor filters, as opposed to digital filters, are analog sampled data systems. The signal remains in the analog domain, as the charge on a capacitor. Whether using an analog or digital sampled data system, the effects of sampling the signal must be considered.

Figure 1 shows a time domain input and output signal of an analog sampled data system. In the ideal case, the sampled data system, samples the input signal instantaneously, or with an impulse function. The amplitude of each sample is equal to the instantaneous amplitude of the input signal. The output is a series of narrow pulses, each separated by time T, the sampling period.

2.1 Aperture

Since an impulse function in the time domain corresponds to a flat spectrum in the frequency domain, the input spectrum is exactly reproduced in the frequency domain, however, in reality the sampling signal is periodic and has a finite pulse width. When convoluting a finite pulse width with an input spectrum F(jω) with unity amplitude, the result is found to be:

$$F_{st}(j\omega) = \frac{\tau}{T}\,\frac{\sin(\omega\tau/2)}{\omega\tau/2}\sum_{n=-\infty}^{\infty} F[j(\omega - n\omega_s)] \qquad (1)$$

Figure 1: Signal Processing Systems

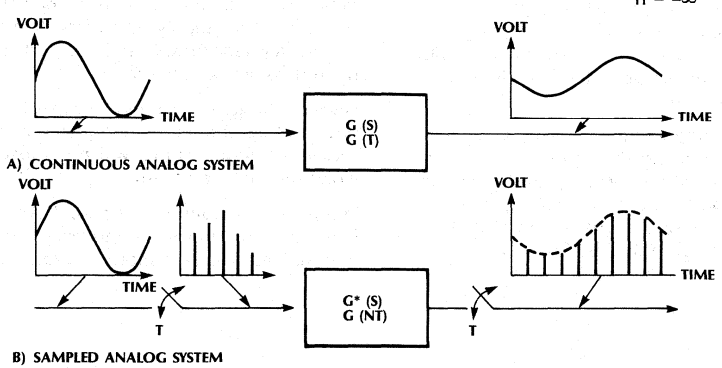


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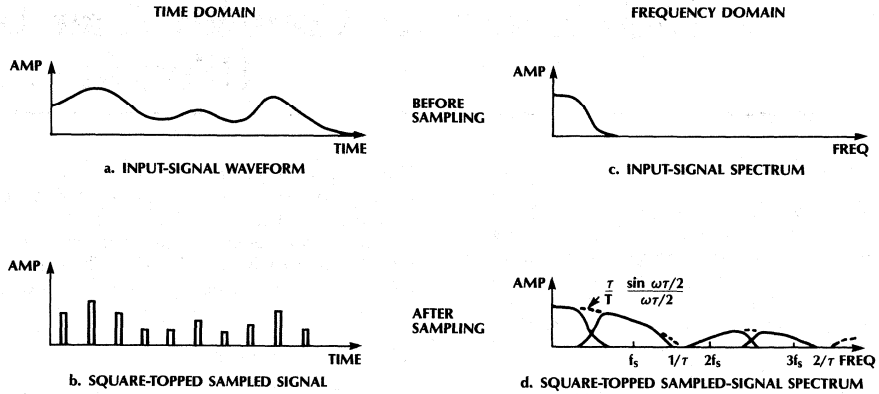
Figure 2: Analysis of a Sampled Signal



From this equation, the gain is a continuous function of frequency defined by (τ/T) (sin $(\omega\tau/2)/(\omega\tau/2)$) where τ is the sample pulse width in seconds, T is the sample period in seconds, and ω the frequency in radians per second.

The time and frequency domain plots for the finite pulse width sampled signal are shown in figure 2. Figure 2 is a plot of the previous equations where the frequency spectrum is formed around multiples of the sampling frequency. As long as the adjacent spectra do not overlay (aliasing distortion), the continuous signal can be reconstructed from the discrete samples.

To evaluate the amplitude distortion caused by having a finite pulse width, one can simply solve equation 1. Since the ML2111 has a zero-order hold τ/T is unity. Assuming a 7.5 MHz sampling frequency and a bandwidth of 150 KHz, the amplitude distortion or attenuation is 5.7×10^{-3} dB.

The equation shows that when the sampling frequency is 40-50 times greater than the bandwidth, the aperture effects are negligible.

2.2 Aliasing

Another potential source for distortion in a sampled data system is aliasing. Aliasing distortion occurs when the input frequency to a sampled data system contains frequency components above one half the sampling frequency. These higher frequency components beat with the sampling frequency and are reflected back into the baseband causing aliasing distortion.

The additional spectral components caused by sampling the input signal are the sum and differences of the input frequencies with multiples of the sampling frequency. For example, assume the input to a sampled data system is a sine wave with a frequency of 100 KHz (f_i) sampled at 250 KHz (f_s), as shown in figure 3a. The first few spectral components will be at: (f_i = 100 KHz; original signal, $f_s - f_i$ = 150 KHz, $f_s + f_i$ = 350 KHz, $2f_s - f_i$ = 400 KHz, $2f_s + f_i$ = 600 KHz, . . .) Now assume f_i has a second harmonic, which would be at 200 KHz, the spectral components are shown in figure 3b. If our bandwidth of interest were from DC to $f_s/2$, then the $f_s - 2f_i$ component interferes with the original signal. If we were to reconstruct the original signal by lowpass filtering it, we could not separate the aliased component, $f_s - 2f_i$ = 50 KHz, from the original signal.

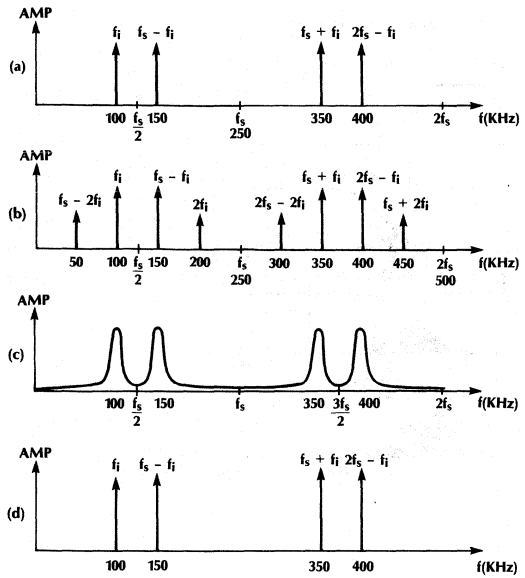
If our bandwidth of interest is a bandpass, the aliased component may not interfere. For example, if the ML2111 were to be used as a four pole bandpass filter with a center frequency at 100 KHz and a Q = 10 as shown in figure 3c, then the aliasing components in the above example would be filtered out as shown in figure 3d. But if the ML2111 were to be used as a low pass filter, then the $f_s - 2f_i$ aliased component would not be filtered out by the ML2111, and an anti-aliasing filter would be needed.

If the input signal is not band-limited, and the aliasing components fall within the bandwidth of interest, then a lowpass filter or anti-aliasing filter must be placed in front of the ML2111. This filter must be a continuous filter rather than a sampled data filter, however, the complexity of this filter is typically much less than the ML2111 filters, and its frequency response is less critical allowing for relaxed component tolerances.

Since no frequency component can be totally eliminated, one must determine the acceptable amplitude of the aliasing components that will *not* impact the Signal to Noise ratio of the system.

The higher the ratio of sampling frequency to input bandwidth, the lower the requirements on the anti-aliasing filter. Figure 4 shows the effects of sampling rate

Figure 3. Aliasing Distortion Using Sample Data Filters



rate on the separation of sampled signal spectra. Note the amount of overlap increases as the sampling frequency is decreased for a fixed input signal bandwidth. In general, the higher the sampling frequency, the less aliasing distortion. Since the ML2111's sampling frequency is typically either 50 or 100 times greater than the input bandwidth, the aliasing distortion may be negligible.

2.3 Signal to Noise Ratio and Aliasing Distortion

To determine whether aliasing distortion could be a problem, one must first determine the Signal to Noise Ratio of the overall system. Aliasing distortion less than the signal to noise ratio is of no concern.

The data sheet specifies noise based on Q and bandwidth. From these specs one can deduce the S/N ratio of one bi-quad in the ML2111. Using a simplified example, a bandpass filter with a Q = 10 and a system clock to center frequency ratio of 50:1 has noise that is 262 μVrms over a 750 KHz bandwidth; taken from the specs in the data sheet. To determine the maximum input signal amplitude, one must consider the slew rate spec. The typical value is 2 V/μsec, however a comfortable safety margin is 1.495 V/μsec for the commercial temperature range and 1.256 V/μsec for the military temperature range. The slew rate = $2\pi fA$, where f is the maximum input frequency, and A is the peak amplitude in volts. Therefore A = 1.495E6/(2*π*100E3) = 2.3 Volts; and the S/N = 78 dB.

Based on a 100 KHz bandpass filter with a Q = 10, f_{CLK}:f_0 = 50:1, and a signal to noise ratio of 78 dB, what sort of anti-aliasing filter would be sufficient? One must first look at the spectrum of the input signal, particularly in the 4.895 MHz to 4.905 MHz frequency range since this is the range that will be reflected back into the bandwidth of interest, 95 KHz to 105 KHz. If the frequency components in the 4.895 MHz to 4.905 MHz are below 78 dB, they will have a minimum impact on the signal to noise ratio. Let's assume that these frequency components are down only 20 dB. Then the anti-aliasing filter will have to attenuate the frequencies in the 4.895 MHz to 4.095 MHz range by 78 - 20 = 58 dB, and pass the frequencies in the 95 KHz to 105 KHz frequency range with no attenuation. A simple two pole Butterworth filter with a cutoff frequency of 170 KHz will be sufficient, however there will be an attenuation of about 0.5 dB at 100 KHz due to this filter.

Figure 5a shows a Sallen-Key active filter capable of implementing two poles, and figure 5b shows a Rauch filter also implementing two poles. These two active filters are good examples to use for anti-aliasing and reconstruction filters. Using the Rauch filter for the above example, C_5 = 400 pF, C_8 = 90 pF, and R = R_4 = R_6 = R_7 = 5 KΩ. Fortunately the cutoff frequency for the antialiasing and reconstruction filters are not critical since capacitors can vary 5% and resistors can vary 1%. Taking into account component tolerance for our example, the cutoff frequency can vary worst case from 152 KHz up to 178 KHz.

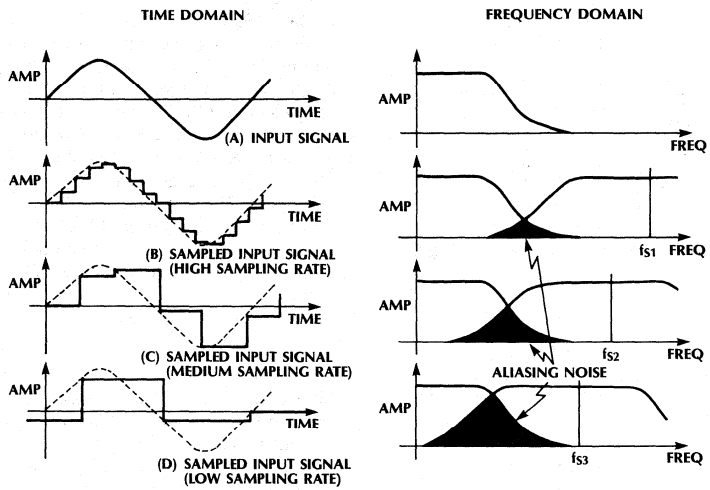
The important aspects to note are that one must first determine the signal to noise ratio in the bandwidth of interest. Based on this bandwidth, are there any frequencies that will be reflected back into the bandwidth of interest, and if so how much will they need to be attenuated? Remember that frequency components reflected back outside of the bandwidth of interest, will be filtered by the ML2111. Since the ratio of the sampling frequency to the center frequency is large on the ML2111, most designs will not need an anti-aliasing filter, and if they do, a simple two pole butterworth should suffice.

2.4 Signal Reconstruction

The output signal of a switched capacitor filter contains higher frequency components since it is a sampled signal. Many systems can accommodate these higher frequency components; however, if they interfere with the system's performance, then a signal reconstruction filter can be employed.

A time domain and frequency domain plot of the output from the ML2111 is given in figure 6. The output signal changes amplitude every clock period. These sharp transitions elicit high frequency components in the output signal. Once again, the fact that the ratio of the sampling frequency to the input bandwidth is high, reduces these distortion effects. As a result of the sin (x)/x envelope, the higher frequency components are attenuated. For example, assuming the input bandwidth is 100 KHz and

Figure 4: Effects of Sampling Rate on Aliasing Noise



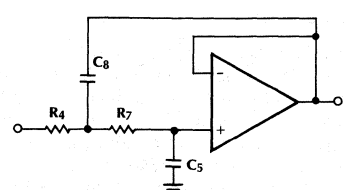
the sampling rate is 5 MHz, the frequencies around 4.9 MHz are down 34 dB, and they degrade towards zero as the frequency reaches 5 MHz. A single pole reconstruction filter with a cutoff frequency at 200 KHz would add an additional attenuation of 27 dB at 4.9 MHz but would attenuate the output by 1 dB at 100 KHz. A two pole Butterworth as in figure 5a or 5b would yield 58 dB of attenuation at 4.9 MHz and only 0.5 dB at 100 KHz.

3.0 Layout Considerations

The layout of any board with analog and digital circuitry combined mandates careful consideration. The most important steps in designing a low noise system are:

1. All power source leads should have a bypass capacitor to ground on each printed circuit board (PCB). At least one electrolytic bypass capacitor (50 μF or more) per board is recommended at the point where all power traces from the ML2111 join prior to interfacing with the edge connector pins assigned to the power leads.
2. Layout the traces such that analog signal and capacitor leads are far from the digital clock.
3. Both grounds and power supply leads must have low resistance and inductance. This should be accomplished by using a ground plane where ever possible. Either multiple or extra large plated through holes should be used when passing the ground connections through the PCB.
4. Use a separate trace for clock ground, and connect it to the edge connector board ground.
5. Use ground plane on both sides of PC board.
6. All power pins on ICs should have 0.1 μF and a 0.01 μF capacitors in parallel tied to ground, and as close to the power pins as possible.
7. Stray capacitance, lead lengths, and traces, on pin 4 and 17, the negative input of the op amp, should be kept to a minimum, particularly for high frequency filters which are more sensitive.

Figure 5a. Sallen-Key Filter

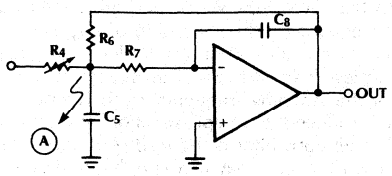


$$\frac{1}{s^2B + sC + 1}$$

$B = R_4R_7C_5C_8 = 1/\omega_0^2$ $\quad R_4 = R_7$

$C = C_5 (R_4 + R_7) = 1/Q\omega_0$

Figure 5b. Rauch Filter



DC Gain: $\frac{R_6}{R_4} = H(0)$ [Minimize Parasitic C at Node (A)]

Transfer function: $\frac{H(0)\ (1/B)}{s^2 + s(C/B) + 1/B} = \frac{H(0)\ \omega_0^2}{s^2 + s(\omega_0/Q) + \omega_0^2}$

$B = R_6R_7C_8C_5$

$C = \frac{R_6R_7C_8 + C_8(R_6 + R_7)R_4}{R_4}$

Choose Butterworth response for example:

$\omega_0 = 2\pi[170\ KHz] \approx 1.06 \times 10^6$ rad/s
$Q = .707$

say $R_4 = R_7 = R_6 = R \Rightarrow 1/\omega_0^2 = R^2C_8C_5$

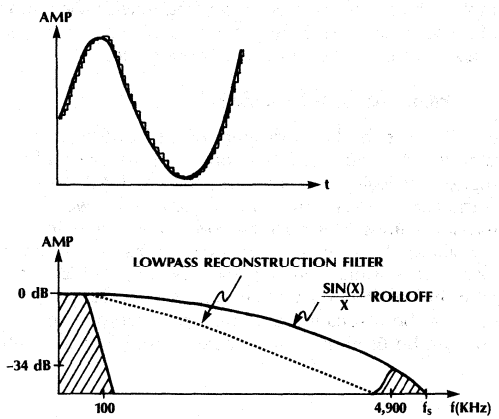
$C = RC_8 + C_8(R_6 + R_7) = RC_8 + 2C_8R = 3RC_8$

$$\Rightarrow \frac{C}{B} = \frac{3RC_8}{R^2C_8C_5} = \frac{3}{RC_5} = \frac{\omega_0}{Q}$$

$$\Rightarrow \begin{cases} C_5 = \frac{3Q}{R\omega_0} \\ C_8 = \frac{1}{\omega_0^2R^2C_5} \end{cases}$$

say R = 5 KΩ
∴ C_5 = 400 pF
C_8 = 90 pF

Figure 6: Signal Reconstruction



3.1 Clocks and Output Loading

It is important to properly terminate the clock input to prevent overshoot. Each pin has protection diodes for Electro-Static Discharge (ESD), and any overshoot of more than 0.3 to 0.5 volts will be injected directly into the ML2111's ground and/or supplies. Matching the characteristic impedance of the line will prevent any ringing thus reduce clock noise.

When operating with high clock frequencies, the output of the op amp and integrators should be properly loaded. Ideally these outputs—LP, BP, and N—like to drive a total of 2 to 3 mA of peak current each. Assuming the output voltage swing is ±2 volts, the sum of R_5 and R_6, in mode 1c for example, should be 2 V/2 mA or about 1,000 ohms; assuming no other resistors are connected. Sometimes this is difficult to do if the ratios and loading cannot simultaneously be achieved. In this case an additional loading resistor placed as close as possible to the output pin will serve the purpose of properly loading the outputs.

4.0 Sweeping Filters

One particularly nice feature of sampled data filters is the fact that the center frequency of a filter is directly related to the clock frequency. For a lowpass filter, increasing the clock frequency increases the cutoff frequency. Even though the center frequency increases proportionally with the clock, Q stays constant. Therefore in a bandpass filter, increasing the clock frequency increases the center frequency as well as the bandwidth. Table 2 in the data sheet illustrates this relationship. (Note that there is some Q deviation as the system clock goes beyond a certain value. Refer to figure 2E in the data sheet for a graph of this phenomenon)

A good rule of thumb for the maximum rate a filter can be swept is that the Sweep Rate should be less than the square of the bandwidth of the filter. This will reduce attenuation of the passband as a result of sweeping the filter. The theoretical derivation of this approximation is as follows.

Assume we have a bandpass filter with an in-band signal that starts at t = 0. The output of the filter will exponentially increase until it reaches the steady state gain of the passband. After 4 time constants (τ), the output sine wave will be at 98% of its final amplitude.

Sweeping a filter is analogous to keeping the filter constant and sweeping the input frequency. To prevent the filter from attenuating the sweeping input signal by more than 2% or 0.16 dB:

$$\text{Sweep Rate} < BW/4\tau \quad (2)$$

but the time constant can be approximated by:

$$\tau \simeq Q/2\pi f_0 \quad (3)$$

and,

$$Q = f_0/BW \text{ or } BW = f_0/Q \quad (4)$$

substituting τ and BW into equation (2) results in:

$$\text{Sweep Rate} < \pi BW^2/2 \quad (5)$$

5.0 High Frequency Operation

There are three basic modes for the ML2111 — mode 1, 2 and 3. Within each mode there are several variations as shown in the table below.

Mode 1*	High Frequency Mode
1, 1a, 1d	f_0 up to 150 KHz; Q up to about 20**
1b, 1c	f_0 up to 100 KHz; Q up to about 30
Mode 2	**Flexible for Notches**
2, 2a, 2b	f_0 up to 30 KHz; Q up to about 30
Mode 3	**Most Flexible/Low Component Count**
3, 3a	f_0 up to 30 KHz; Q up to about 30

* Q and f_0 have an inverse relationship. This table is only an approximation. Actual performance depends on board layout and stray capacitance.

** 15% or less Q deviation. Higher Q's can be realized with greater deviation.

Mode 1 is the only mode which has the input amplifier outside the resonant loop. This is important because the input amplifier reduces the bandwidth potential of the filter. *Only Mode 1 can achieve filters with resonant frequencies up to 150 KHz.*

Inserting an ML2111 into an MF10, LMF100, or LTC1060 socket and increasing the clock frequency does not automatically increase the bandwidth potential up to 150 KHz. If these pin-compatible parts were designed using Mode 1, the bandwidth improvements would be realized; however if they were used in another mode, there would be limited bandwidth improvements.

Complex, high order filters usually have pole pairs with different center frequencies; Elliptical and Chebyshev filters are two examples. To realize two pole pairs in one ML2111 with different center frequencies, one must either use two different clocks, or use a mode which allows the center frequency to be modified by external resistors.

Using different clock frequencies to realize poles with different center frequencies is not recommended. Besides the additional expense of providing more than one clock, the two system clocks may beat with each other and possibly result in side tones that falls within the passband of the filter. Additionally if anti-aliasing is needed, separate anti-aliasing filters would be needed for each stage.

Looking at tables 1 and 2 in the ML2111 data sheet, one can see the modes that allow the center frequency to be modified by external resistors. These modes each have an additional coefficient multiplied by $f_{CLK}/100(50)$. From the block diagrams one can see that the modes which allow the center frequency to be modified, feedback the LP output using a resistor divider. The modes that restrict the ratio to 50 or 100 have a unity gain LP feedback.

If the coefficient multiplied by $f_{CLK}/100(50)$ is greater than or equal to 1, as in Mode 1b, then the ratio of f_{CLK} to f_0 can be less than 50 or 100. Whereas if this coefficient is less than or equal to 1, then the ratio of f_{CLK}:f_0 can be greater than or equal to 50 or 100. Reducing the ratio of f_{CLK} to f_0 to less than 40 to 50 is not recommended. As the ratio of the sampling frequency to the center frequency is reduced, the approximation of a sample data filter to a continuous filter is reduced. Aperture effects increase, aliasing effects may increase, harmonics in the output increase, and the warpage between the discrete and the continuous filter increase. 40 to 50:1 is the minimum recommended ratio of f_{CLK} to f_0.

Based on the above arguments one might conclude that 100:1 is better than 50:1. In general this is true for switched capacitor filters, but not for the ML2111. The specifications in the data sheet show that a 50:1 ratio provides a more accurate Q than a 100:1, and a 50:1 ratio allows higher frequency filters.

Mode 3 is the most flexible since the center frequency can be greater than or less than $f_{CLK}/100(50)$ by selecting R_2 and R_4. Its also the most efficient since it has the lowest component count. However mode 3 can only work up to 30 to 40 KHz or Qs up to the 10 to 30 range; higher f_0 can be obtained with lower Qs. Sometimes a small capacitor (C_4) across R_4 can compensate the filter response and offer less Q deviation. The value should be selected by setting C_4 equal to $1/2\pi R_4 BW$ where BW is approximately equal to 2 to 4 MHz.

Another reason mode 3 can only be used at lower frequencies is that there is a true sample and hold at the positive input of the summer. This sample and hold adds a 7.2 degree delay at the center frequency when using a 50:1 ratio (360°/50). By using a higher ratio this delay is lowered. Since the ML2111 allows a higher system clock than other competing devices, this delay can usually be made smaller for similar center frequencies.

In conclusion, for high frequency filters use Mode 1. For complex filters with various center frequencies use Mode 1c. In most cases one should choose 50:1 over 100:1 ratio for more accurate Q's and center frequencies.

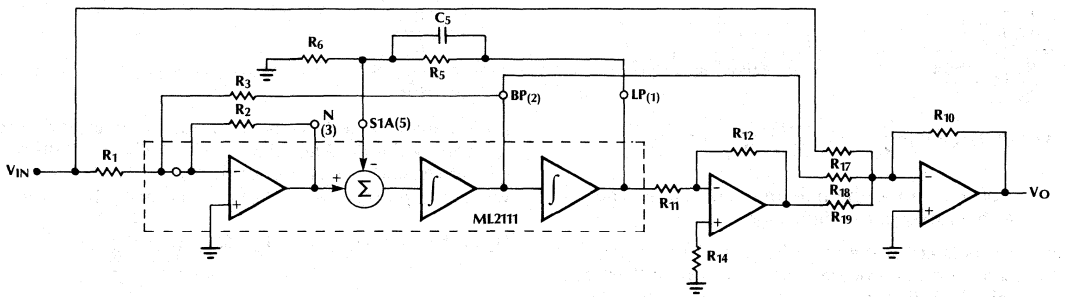
5.1 A Flexible Building Block

Figure 7 shows the block diagram of a second order section which includes both a complex pole pair and a complex zero pair. The poles are provided by the ML2111 and the zeros realized by one and sometimes two external op amps. This building block uses mode 1c which allows the poles to have a center frequency based on external resistors as well as the clock, plus it can be used in higher frequency filters since the op amp is outside of the resonant loop. The same feedforward circuit can be used on other modes as well, but for high

frequency filters, where each complex pole pair has a different center frequency, mode 1c is the best choice. As mentioned before, only when Butterworth filters are desired, use mode 1 to achieve higher frequencies and a higher dynamic range. The transfer function for the flexible building block is given below.

$$\frac{V_O}{V_{IN}} = \left(-\frac{R_{10}}{R_{17}}\right)\left[\frac{s^2 + \frac{R_2}{R_3}\left[1 - \frac{R_{17}}{R_{18}}\frac{R_3}{R_1}\right]s\omega_1 + \left[1 + \frac{R_2R_{12}R_{17}}{R_1R_{11}R_{19}}\left(1 + \frac{R_5}{R_6}\right)\right]\frac{R_6}{R_5 + R_6}\omega_1^2}{s^2 + \frac{R_2}{R_3}s\omega_1 + \frac{R_6}{R_5 + R_6}\omega_1^2}\right] \quad (6)$$

Figure 7: Flexible Building Block



At least one and sometimes two external op amps are required to realize the zeros. The first op amp serves as an inverter, while the second one sums the input signal with the lowpass and bandpass outputs. A fast op amp should usually be used with greater than 10 MHz bandwidth to minimize signal phase shifts. Depending on the application, sometimes a slower amplifier will suffice. In some cases no external op amp is necessary and the second op amp in the ML2111 if not being used will suffice. This was done in figure 34 in the data sheet.

With the Flexible Building Block a lowpass, highpass, notch, and allpass section can be realized by properly positioning the zero locations. Zero locations are chosen by selecting the appropriate resistors. The difference between the lowpass output provided by the ML2111 in mode 1c and the lowpass function realized by the flexible building block is that in mode 1c the response is monotonically decreasing, while the Flexible Building Block has a complex zero pair which inserts a ripple in the stop band and flattens out at high frequency.

Since the Flexible Buidling Block uses mode 1c, the pole equations remain the same whether there is feedforward or not. What changes is the zero location and the DC gain. The following equations are used to determine the pole locations and Q for the Flexible Building Block, which uses mode 1c.

$$f_0 = \frac{f_{CLK}}{100(50)}\sqrt{\frac{R_6}{R_5 + R_6}}$$

$$Q = \frac{R_3}{R_2}\sqrt{\frac{R_6}{R_5 + R_6}}$$

A handy set of equations to convert pole and zero locations given in rectangular coordinates to f_0 and Q values is as follows:

Complex Pole = $\sigma + j\omega$;

$$f_0 = \frac{\sqrt{\sigma^2 + \omega^2}}{2\pi} \quad Q = \frac{1}{2}\sqrt{1 + (\omega/\sigma)^2} \quad (7)$$

By cascading several of these building blocks, complex high frequency Elliptical filters can be realized.

5.2 Lowpass

For a lowpass design with a notch, the zeros should be placed on the $j\omega$ axis at frequencies greater than the poles' center frequency. In the numerator of the transfer function for equation 6, the coefficient for $s\omega_1$ should be set to zero; setting $\frac{R_3}{R_1} = \frac{R_{18}}{R_{17}}$.

Since $\frac{R_6}{R_5 + R_6}\omega_1^2 = \omega_0^2$, the coefficient

$1 + \frac{R_2R_{12}R_{17}}{R_1R_{11}R_{19}}\left(1 + \frac{R_5}{R_6}\right)$ determines the center frequency of the zero. In this form it is always greater than one, therefore the center frequency of the zero is always greater than the center frequency for the poles; hence a lowpass filter. The pole/zero location and the frequency response are shown below.

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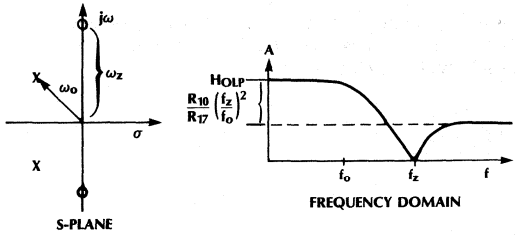


Equations for the lowpass configuration:

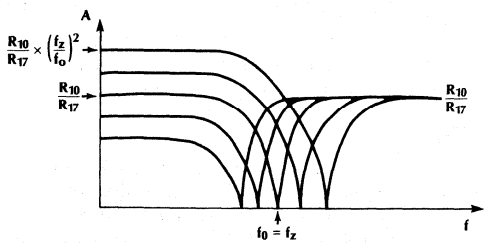
$$\frac{R_{17}}{R_{19}} = \frac{\left(\frac{f_Z}{f_0}\right)^2 - 1}{\frac{R_2}{R_1}\left(1 + \frac{R_5}{R_6}\right)} \qquad f_Z = f_0\sqrt{1 + \frac{R_2R_{12}R_{17}}{R_1R_{11}R_{19}}\left(1 + \frac{R_5}{R_6}\right)}$$

$$\text{DC Gain} = H_{OLP} = \left(-\frac{R_{10}}{R_{17}}\right)\left(1 + \frac{R_2R_{12}R_{17}}{R_1R_{11}R_{19}}\left(1 + \frac{R_5}{R_6}\right)\right)$$

The ratio of the zero to the pole frequency determines the DC to high frequency attenuation.

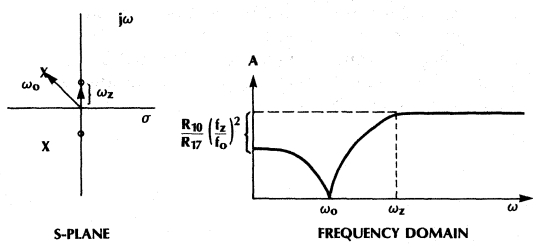
When the zeros are at the same frequency as the poles the bi-quad becomes a notch, and there is no difference between the high frequency and low frequency gain. The larger the difference between the pole and zero frequencies, the greater the rejection. Figure 8 illustrates the relationship between pole/zero location and gain.

Figure 8: Varying f_Z and Keeping f_0 and Q Constant



5.3 Highpass

For a highpass filter the zeros must be less than the center frequency for the poles. The pole/zero plot and the frequency plot are shown below.



To place the zeros at a lower frequency than the poles the coefficient $1 + \frac{R_2R_{12}R_{17}}{R_1R_{11}R_{19}}\left(1 + \frac{R_5}{R_6}\right)$ must be less than one. This can be done by removing the inverter in figure 7, which makes the sign of R_{19} negative. To place the zeros on the jω axis, once again $\frac{R_3}{R_1} = \frac{R_{18}}{R_{17}}$. Equations for the highpass configuration:

$$f_Z = f_0\sqrt{1 - \frac{R_2R_{12}R_{17}}{R_1R_{11}R_{19}}\left(1 + \frac{R_5}{R_6}\right)}$$

$$H_{OHP} = -\frac{R_{10}}{R_{17}}$$

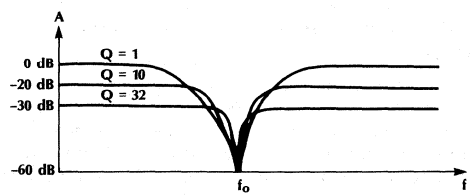
5.4 Notch

Even though mode 1c provides a notch output, the notch realized by the flexible building block achieves 0 dB of gain at DC and at high frequencies regardless of the Q value. The problem with the notch in mode 1c is that

$$H_{ON1}\ (f \rightarrow 0) = H_{ON2}\ (f \rightarrow f_{CLK}/2) = \frac{\sqrt{\frac{R_6}{R_5 + R_6}}}{Q}.$$

As Q increases $H_{ON1,2}$ must decrease otherwise the bandpass output node, BP pin 2 or 19, will saturate. The restriction is that $H_{OBP} = 1 = -R_3/R_1$. Let's take a simple case when $R_5 = 0$, then $H_{ON1} = H_{ON2} = 1/Q$. The plot below shows the notch for different Q's in mode 1c.

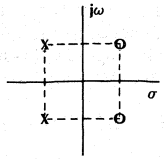
Figure 9: Mode 1c Notch when $R_5 = 0$



To realize the notch using the Flexible Building Block the zeros must be placed on the jω axis at the same resonant frequency as the poles. Therefore from equation 6, $\frac{R_3}{R_1} = \frac{R_{18}}{R_{17}}$ and $R_{19} \rightarrow \infty$. Setting R_{19} equal to infinity means removing it from the circuit; which saves an op amp and a few resistors. H_{OBP} still must equal one, however the gain at DC and $f_{CLK}/2$ is independent of Q; $H_{ON1}\ (f \rightarrow 0) = H_{ON2}\ (f \rightarrow f_{CLK}/2) = -R_{10}/R_{17}$. Tuning R_{18} adjusts the depth of the notch. See figure 34 in the data sheet for an example.

5.5 Allpass Equalizer

An allpass filter is used to linearize the filter's phase response. A linear phase response results in a constant group delay. An allpass filter keeps the gain constant and just shifts the phase. To keep the gain constant and only shift the phase, the poles and zeros must be equal but on opposite sides of the s-plane as shown below.



S-plane representation of 2nd order Allpass Filter

The Flexible Building Block can function as an allpass when $R_{19} \rightarrow \infty$ and $\frac{R_{17}R_3}{R_{18}R_1} = 2$. The Transfer function for the allpass is:

$$\frac{V_O}{V_{IN}} = \left(-\frac{R_{10}}{R_{17}}\right) \frac{s^2 - \frac{R_2}{R_3}\omega_1 s + \frac{R_6}{R_5 + R_6}\omega_1^2}{s^2 + \frac{R_2}{R_3}\omega_1 s + \frac{R_6}{R_5 + R_6}\omega_1^2} \quad (8)$$

5.6 Frequency Compensation

In some cases it is possible to improve the Q accuracy and minimize Q deviation by adding a capacitor (C_5) in parallel with R_5 in figure 7. This capacitor serves as compensation for a pole at around 2.4 MHz in the output of LP. The zero location should be placed at around 2.4 MHz, where the internal pole is. Unfortunately C_5 adds a pole as well as a zero to this branch. If this pole is too close to the zero, the benefit of C_5 is diminished. The zero location is: $f_Z = 1/2\pi R_5C_5$ and the pole location is: $f_p = 1/2\pi(R_5 \parallel R_6)C_5$, ($R_5 \parallel R_6$ is the parallel equivalent resistance). The larger the ratio of the pole frequency to the zero frequency, the better this capacitor will serve.

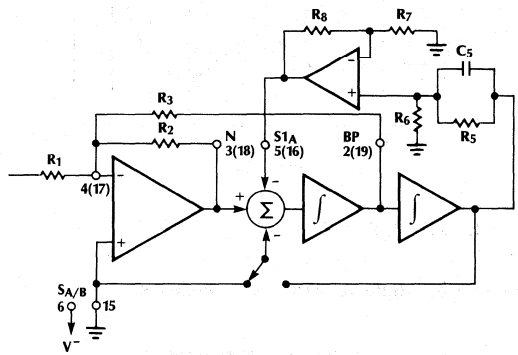
The highest center frequency attained is when R_5 equals zero. (Note: Practically speaking R_5 should never be zero, to allow fine tuning of f_0.) Unfortunately C_5 cannot properly compensate the 2.4 MHz internal pole with a negligible value for R_5. To overcome this problem, compensation can be achieved at high frequencies using an op amp in the LP feedback branch as shown in figure 10.

The center frequency in mode 1c is calculated by the following equation:

$$\frac{f_{CLK}}{f_0} = \frac{50}{\sqrt{k}}$$ where k = Transfer function

With a passive feedback loop using R_5 and R_6, $k = \frac{R_6}{R_5 + R_6}$. However when using the op amp configuration as in figure 10, $k = \left(\frac{R_6}{R_5 + R_6}\right)\left(1 + \frac{R_8}{R_7}\right)$. When k = 1 the ratio is 50. Using active feedback in mode 1c has the unique advantage of allowing the ratio of clock to center frequency to be less than 50 by setting k greater than 1. It is not recommended to use ratios less than 40-50, however this feature does allow more freedom in tuning the center frequency of the pole above or below the ratio of 50. If the circuit uses a crystal for f_{CLK}, and the pole needs to be tuned, R_8 could be a potentiometer to allow tuning of the pole. For this compensation to work $\frac{R_8}{R_7}$ should be 4-9 to provide phase lead before phase lag.

Figure 10: Compensation Using Active Feedback for High Frequency Poles



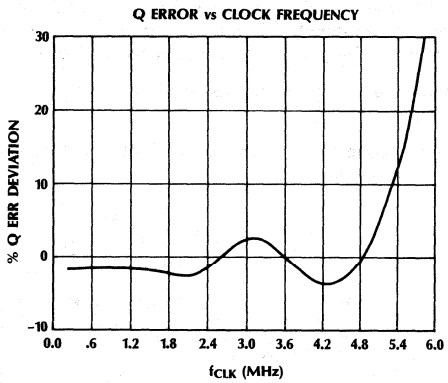
C_5 = 33-66pF (Depends on board's parasitics)
R_8 = 1800Ω; R_7 = 200
R_6 = 100Ω, R_5 = 900Ω

Using mode 1 instead of mode 1c as configured in figure 7, is a better solution for high frequency poles; however there are certain cases where mode 1 cannot be used. For example, if one of the two bi-quads in the ML2111 is already used in mode 1c, then the other one must also operate in mode 1c. It would be less expensive to add an op amp to the second bi-quad of an existing ML2111 than to add an additional ML2111 just to use one bi-quad operating in mode 1.

Figure 11a shows the Q accuracy vs. clock frequency in mode 1c using passive feedback for a Q approximately equal to 10. Q inaccuracy dramatically increases just beyond 100 KHz center frequency. Figure 11b shows Q accuracy vs. center frequency in mode 1c using active feedback with a DC transfer function of 1. The op amp used for this measurement was an AD5539, where

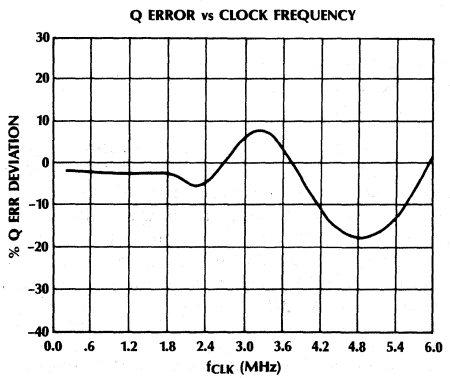
$\frac{R_8}{R_7} = \frac{R_5}{R_6} = 9$. This op amp is a good choice because it has a wide bandwidth, 220 MHz, and is low cost. The figure shows that Q deviation does not dramatically increase until well beyond 120 KHz; therefore for higher frequency operation and high Q, the use of mode 1c with active feedback is recommended.

Figure 11a: Mode 1c with Passive Feedback



$\frac{R_3}{R_2} = 10$; $R_5 = 0$; $R_1 = R_3 = 20K$

Figure 11b: Mode 1c with Active Feedback



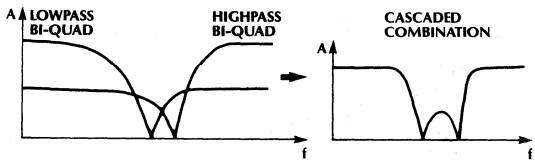
$C_5 = 33pF$; $\frac{R_3}{R_2} = 10$; $R_5 = 0$; $R_1 = R_3 = 20K$

6.0 Design Methodology for Complex Filters

The previous section described how to use the Flexible Building Block to implement lowpass, highpass, notch, and allpass second order sections. Higher order filters are achieved by cascading these second order sections. For example an Elliptical notch is accomplished by cascading lowpass and highpass sections as shown in figure 12.

An Elliptical bandpass is also a combination of highpass and lowpass sections, except for a bandpass filter the cutoff frequency for the highpass bi-quads are lower than the cutoff frequency for the lowpass.

Figure 12: Fourth Order Elliptic Notch



Once the pole and zero location have been determined for the filter desired, the next step is to choose the proper mode of operation and translate the center frequency and Q values for each pole and zero into resistor values. If the pole and zero locations are given in real and imaginary values, they can be converted to f_0 and Q by using equation 7.

For center frequencies between 0 and 20 KHz, either mode 3 or mode 1c can be used. Sometimes mode 3 or mode 3a will result in a lower component count. However mode 3 should be used with caution since high Qs and high parasitic capacitance on pin 4 and 17 can lead to oscillations. This can usually be compensated by using a capacitor across R4, which provides some phase lead, and low value resistors such as 1-2 Kohms.

For center frequencies between 20 to 100 KHz, where each pole has a different center frequency, mode 1c should be used. This range can be extended up to 120 KHz with active compensation in the LP feedback path as shown in figure 11b. The combination of high Qs (20 to 30), and high frequencies (above 80 to 100 KHz), and parasitic capacitance across R_6, can lead to oscillations. This can be dealt with by placing a capacitor C_5 across R_5, or by using active compensation. Additionally the signal swing should be limited to about 1 to 1.4 volts peak-to-peak.

For filters where f_0 is the same for all pole locations, such as Butterworth, Lowpass or Highpass. High order filters with cutoff frequencies up to 150 KHz can be realized using mode 1. In this case the signal level can be increased to 2.82 volts peak-to-peak.

7.0 Design Example

The following is an example an eighth order Elliptic bandpass filter with a center frequency of 90 KHz and a bandwidth of 19 KHz. This filter was designed built and tested on its own printed circuit board. A print of the masks for the PCB, and a photograph of the performance of the filter is included at the end of this section.

In general, high Q filters (Elliptic and Chebyshev) will have higher sensitivity to component and temperature variations and higher noise than low Q filters such as Butterworth and Bessel.

a) 8th Order Elliptic Bandpass with the following Filter characteristics:

Amax: 0.5 dB (peak to peak passband ripple)

Amin > 50 dB (stopband attenuation)

(f_1, f_2) Passband: 81,000 to 100,000 Hz (geometrically symmetric) $\Rightarrow f_c^2 = f_1 \times f_2$

(f_c) Center: 90,000 Hz

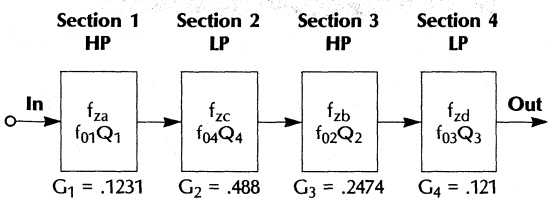
Stopband: 70.5 KHz to 115 KHz

b) Obtain:

Poles
- f_{01} = 80839 Hz, Q_1 = 30.2
- f_{02} = 85820 Hz, Q_2 = 10.86
- f_{03} = 94383 Hz, Q_3 = 10.86
- f_{04} = 100200 Hz, Q_4 = 30.2

Zeros
- f_{za} = 69185 Hz
- f_{zb} = 50082 Hz
- f_{zc} = 117080 Hz
- f_{zd} = 161733 Hz

c) After considering a few pole-zero pairing combinations the following (not necessarily optimum) combination was adopted.



Note: G_i are the high frequency gains. (= R_{10}/R_{17})

Because of difficulty in solving equations first order equation were calculated and final values found by using potentiometer.

d) Choose f_{CLK} = highest f_0 = 100200 @ 50:1 $\Rightarrow 50f_0$ = 5.01 MHz. Choose ~ 10% higher f_{CLK} = 5.5 MHz. It's better to choose a slightly larger f_{CLK} to be able to adjust R_5.

e) Design Procedure.

Section 1. *) Want a ratio = $\frac{5.5\ \text{MHz}}{80839\ \text{Hz}} \cong 68 = R_t$

in Mode 1c $R_t = 50 \times \sqrt{1 + \frac{R_5}{R_6}} \Rightarrow 1 + \frac{R_5}{R_6} = 1.8516$

Assume $R_5 + R_6 = 1000\ \Omega$

then $1 + \frac{R_5}{R_6} = \frac{1000}{R_6} = 1.8516$

$\Rightarrow R_6 \cong 540\Omega$ (fixed R)

$\Rightarrow [R_5 = R_6\ (1.8516 - 1) \cong 460\ \Omega]$ [1000 Ω trim pot]

*) Want Q = 30.2 use following approximation:

$$\frac{R_3}{R_2} \approx \frac{Q\sqrt{1 + \frac{R_5}{R_6}}}{1 + Q(f_0/f_X)} \text{ (Note)} \quad ; \text{ where } f_X = 2.4\ \text{MHz (internal pole)}$$

$\cong 20.4 \Rightarrow$ assume R_2 = 2000 Ω

and $R_3 \approx 40.7$ KΩ (100 K trim pot)

and initially assume $R_1 = R_3 = 40.7$ KΩ

*) Zero. Use the following approximation.

f_{za} = 69185 Hz

$$\frac{R_{17}}{R_{19}} \cong \frac{1 - (f_z/f_0)^2}{\frac{R_2}{R_1}\left(1 + \frac{R_5}{R_6}\right)} = \frac{1 - (69185/80839)^2}{1/20 \times 1.8516} = 2.89$$

Since R_{19} loads the LP output then assume $R_{19} > 5000\Omega$. Also since later we will fine tune the gains this relationship will slightly change. Thus, initially assume a higher R_{17} which can be change later if needed.

Choose $R_{17} \cong 30$ KΩ (fixed R)

and $R_{19} \approx 10$ KΩ (20 KΩ trim pot)

choose $R_{18} = R_{17}$ (initially)

and $R_{10} = R_{17} \times G_1 = 30K \times .123 = 3690\ \Omega$ (fixed R)

(Note: This is a first order approximation that underestimates the value of Q, whose final value will be tuned in later in the breadboard stage.)

f)
1. By looking at the bandpass output adjust R_5 until the peak frequency is f_0, in this case 80839 Hz
2. Then adjust R_3 until Q = 30.2
3. Then change R_1 until the peak of the bandpass or lowpass output (larger of the two) is about 0 dB. R_1 does not need to be a trim pot.
4. Now by looking at the output of the section adjust R_{19} to place the zero at the correct frequency (in this case 69185 Hz)

10

5. Adjust R_{18} to obtain a deeper notch. Sometimes R_{18} is not needed at all and can be removed from the circuit.
6. Check the high frequency gain so that it is G_1 = .1231
7. Design the rest of the sections the same way
8. Keep R_{10} of first section as a trim pot to slightly trim gain of the whole filter (if important in the application).

For this design these are the final values:

Section 1.

R_1 = 94.5 KΩ
R_2 = 2 KΩ
R_3 = 66.2 KΩ (100 K pot)
R_5 = 452 Ω (1 KΩ pot)
R_6 = 540 Ω
R_{10} = 3.83 KΩ
R_{17} = 32.4 KΩ
R_{18} = 15 KΩ
R_{19} = 4.65 KΩ
$H_{LP\ PEAK}$ = 1.1512 (+1.22 dB)
$H_{BP\ PEAK}$ = .846 (–1.45 dB)

Section 2.

R_1 = 65 KΩ
R_2 = 2 KΩ
R_3 = 47.4 KΩ (100 K pot)
R_5 = 170 Ω (500 Ω pot)
R_6 = 830 Ω
R_{10} = 14.34 KΩ
R_{17} = 28.7 KΩ
R_{18} = ∞
R_{19} = 2.9 KΩ
$H_{LP\ PEAK}$ = 1.12 (+.984 dB)
$H_{BP\ PEAK}$ = .972 (–.247 dB)

Section 3.

R_1 = 31.5 KΩ
R_2 = 2 KΩ
R_3 = 23.3 KΩ (50 K pot)
R_5 = 389 Ω (1 KΩ pot)
R_6 = 600 Ω
R_{10} = 9.05 KΩ
R_{17} = 40 KΩ
R_{18} = 16.86 KΩ
R_{19} = 6.35 KΩ
$H_{LP\ PEAK}$ = 1.074 (+.62 dB)
$H_{BP\ PEAK}$ = .834 (–1.58 dB)

Section 4.

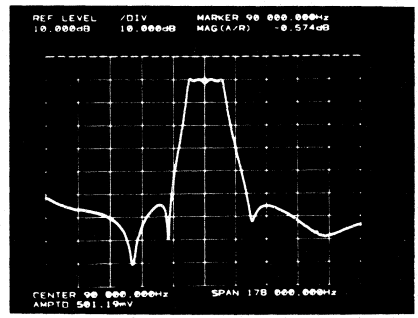
R_1 = 25 KΩ
R_2 = 2000 Ω
R_3 = 21.4 KΩ (50 K pot)
R_5 = 279 Ω (500 Ω pot)
R_6 = 732 Ω
R_{10} = 12 KΩ
R_{17} = 99.97 KΩ
R_{18} = ∞
R_{19} = 6 KΩ
$H_{LP\ PEAK}$ = 1.12 (+.924 dB)
$H_{BP\ PEAK}$ = .953 (–.418 dB)

Note: All R's are 1% metal film 1/4W
Trim pots are 25 turns. 1/2W

When placing resistors in and out of the ML2111 filter circuit, specifically R_3, the filter will oscillate at f_0 due to the Q going to infinity. Also when designing high frequency high Q filters, such as f_0 = 100 KHz and Q = 30 like pole #4, high voltage swings may cause nonlinear operation provoking oscillations. Changing f_{CLK} momentarily to a much lower value will restore the filter to a stable linear operation. Thus it is important for high frequency, high Q filters to limit the input signal swing to about 500-700 mV peak.

7.1 Performance Measurements, Schematics and PCB Layout

Figure 13: Frequency Response of Eighth Order Elliptic Filter.



The center frequency is at 90 KHz with the lower cutoff at 81 KHz and the upper cutoff at 100 KHz. The stopband is down –55 dB at 70.5 KHz and 115 KHz.

Figure 14: Passband of Filter Showing 0.5 dB Ripple.

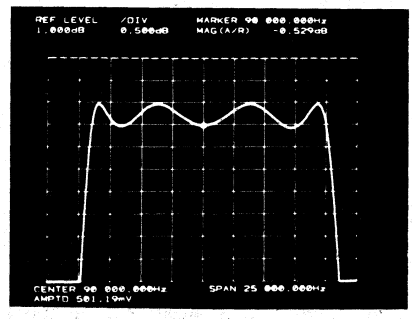
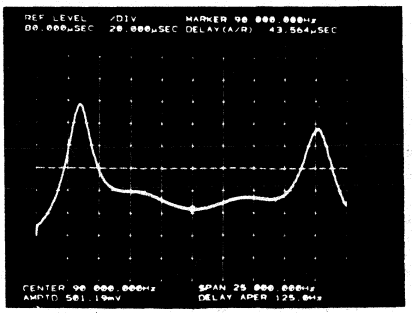
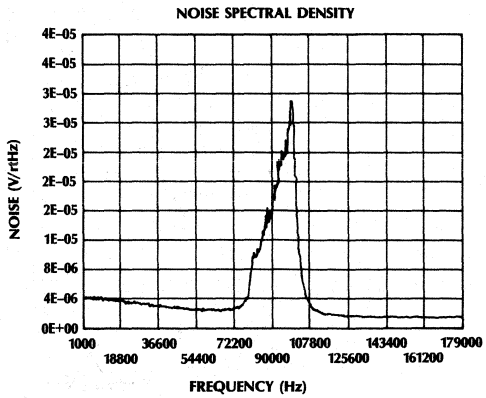


Figure 15: Group Delay.



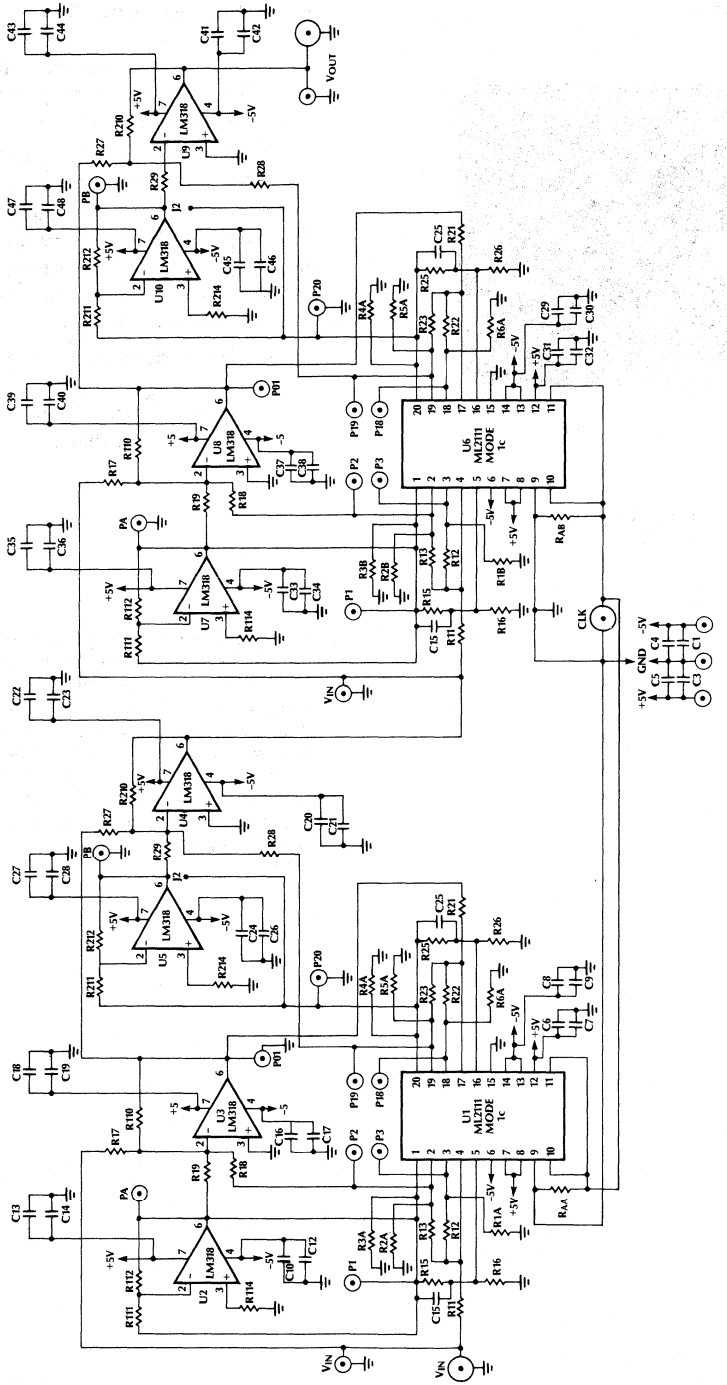
A constant group delay can be achieved by adding allpass equalizer sections to this filter.

Figure 16: Power Spectral Density of the Noise



This plot shows that the pole/zero pairing and order of the bi-quad sections chosen was not optimum as far as noise is concerned. The plot shows that the upper band edge of noise is higher than the lower band edge. A different combination of pole/zero pairing and order pairing would have yielded a flatter noise response and possibly a lower noise value; which would have then improved the S/N ratio. The current design yields S/N of about 40 dB assuming a noise bandwidth from 1 KHz to 179 KHz. Input voltage = 353 mV_{rms}, output noise voltage = 3.14 mV_{rms}.

Figure 17: Schematic Diagram of Printed Circuit Board



(Note that U2 and U7 are not used in this design. This is a general purpose development board and not a minimal component count design).

Figure 18a: PCB Layout Component Side

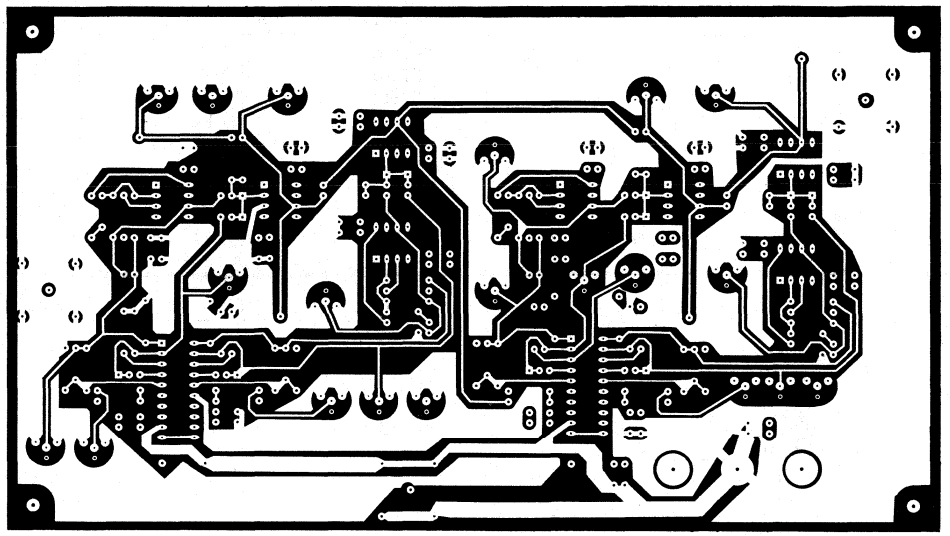
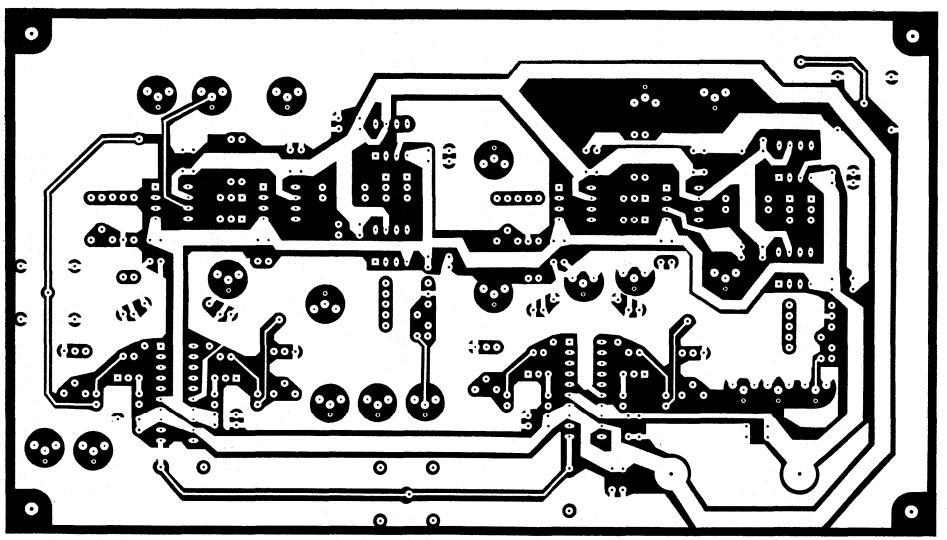


Figure 18b: PCB Layout Solder Side



ML2111 Application Board Parts List

Part #	Value	Note
Resistors		
R1A	1 KΩ	
R2A	500 Ω	
R3A	1 KΩ	
R4A	1 KΩ	
R5A	500 Ω	
R6A	1 KΩ	
R11A	94.5 KΩ	
R12A	2 KΩ	
R13A	66.2 KΩ	100 KΩ Pot
R15A	452 Ω	1 KΩ Pot **
R16A	540 Ω	
R17A	32.4 KΩ	
R18A	15 KΩ	
R19A	4.65 KΩ	10 KΩ Pot*
R110A	3.83 KΩ	10 KΩ Pot*
R111A	OPEN	
R112A	OPEN	
R114A	OPEN	
RAA	100 Ω	
RAB	100 Ω	
R210A	14.3 KΩ	
R211A	5 KΩ	
R212A	5 KΩ	
R214A	2.5 KΩ	
R21A	65 KΩ	
R22A	2 KΩ	
R23A	47.4 KΩ	100 KΩ Pot
R25A	170 Ω	500 Ω Pot**
R26A	830 Ω	
R27A	28.7 KΩ	
R28A	OPEN	
R29A	2.9 KΩ	10 KΩ Pot*
R1B	1 KΩ	
R2B	500 Ω	
R3B	1 KΩ	
R4B	1 KΩ	
R5B	500 Ω	
R6B	1 KΩ	
R110B	9.05 KΩ	
R111B	OPEN	
R112B	OPEN	
R114B	OPEN	
R11B	31.5 KΩ	
R12B	2 KΩ	
R13B	23.3 KΩ	50 KΩ Pot
R15B	389 Ω	1 KΩ Pot**
R16B	600 Ω	
R17B	40 KΩ	
R18B	16.86 KΩ	
R19B	6.35 KΩ	50 KΩ Pot*

Part #	Value	Note
Resistors (Continued)		
R210B	12 KΩ	
R211B	5 KΩ	
R212B	5 KΩ	
R214B	2.5 KΩ	
R21B	25 KΩ	
R22B	2 KΩ	
R23B	21.4 KΩ	50 KΩ Pot
R25B	279 Ω	500 Ω Pot**
R26B	732 Ω	
R27B	100 KΩ	
R28B	OPEN	
R29B	6 KΩ	100 K Pot*
Capacitors		
C15A	OPEN	
C25A	OPEN	
C15B	OPEN	
C25B	OPEN	
C1	100 µF	bypass
C3	100 µF	bypass
C4	0.1 µF	bypass
C5	0.1 µF	bypass
C6	0.1 µF	U1 bypass
C7	0.01 µF	U1 bypass
C8	0.1 µF	U1 bypass
C9	0.01 µF	U1 bypass
C10	OPEN	U2 bypass
C12	OPEN	U2 bypass
C13	OPEN	U2 bypass
C14	OPEN	U2 bypass
C16	0.1 µF	U3 bypass
C17	0.01 µF	U3 bypass
C18	0.1 µF	U3 bypass
C19	0.01 µF	U3 bypass
C20	0.1 µF	U4 bypass
C21	0.01 µF	U4 bypass
C22	0.1 µF	U4 bypass
C23	0.01 µF	U4 bypass
C24	0.1 µF	U5 bypass
C26	0.01 µF	U5 bypass
C27	0.1 µF	U5 bypass
C28	0.01 µF	U5 bypass
C29	0.1 µF	U6 bypass
C30	0.01 µF	U6 bypass
C31	0.1 µF	U6 bypass
C32	0.01 µF	U6 bypass
C33	OPEN	U7 bypass
C34	OPEN	U7 bypass
C35	OPEN	U7 bypass
C36	OPEN	U7 bypass
C37	0.1 µF	U8 bypass
C38	0.01µF	U8 bypass

ML2111 Application Board Parts List (Continued)

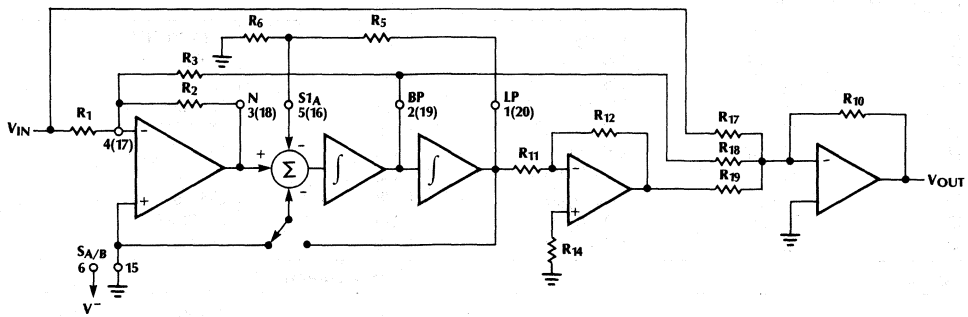
Part #	Value	Note
Capacitors (Continued)		
C39	0.1 μF	U8 bypass
C40	0.01 μF	U8 bypass
C41	0.1 μF	U9 bypass
C42	0.01 μF	U9 bypass
C43	0.1 μF	U9 bypass
C44	0.01 μF	U9 bypass
C45	0.1 μF	U10 bypass
C46	0.01 μF	U10 bypass
C47	0.1 μF	U10 bypass
C48	0.01 μF	U10 bypass
Jumpers		
J1A	IN	
J2A	OUT	
J1B	IN	
J2B	OUT	

Part #	Value	Note
ICs		
U1	ML2111CCP	
U2	OPEN	
U3	LM318H	
U4	LM318H	
U5	LM318H	
U6	ML2111CCP	
U7	OPEN	
U8	LM318H	
U9	LM318H	
U10	LM318H	
Miscellaneous		
20	scope probe sockets	
3	BNC connectors	
3	female banana plugs	
2	20 pin low profile sockets	

* Gain and zero frequency adjustment. May not be needed if application can tolerate slight variations in stop band.
** R5 - In most cases R5 can be replaced by a 1% resistor after trimming has been done.

Appendix A. Flexible Building Block Summary

Lowpass —



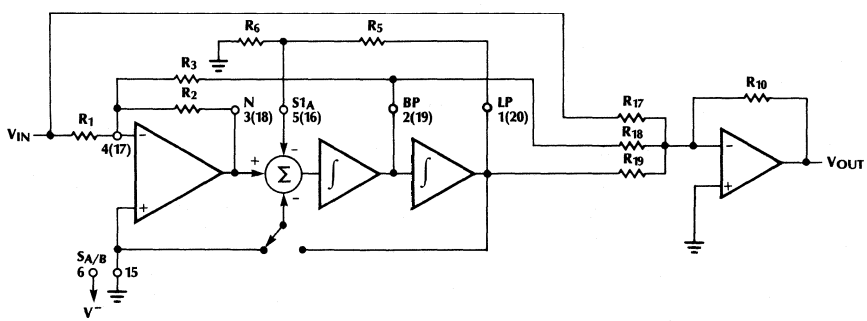
$$f_0 = \frac{f_{CLK}}{100(50)} \sqrt{\frac{R_6}{R_5 + R_6}} \; ; \; Q = \frac{R_3}{R_2} \sqrt{\frac{R_6}{R_5 + R_6}}$$

$$f_Z = f_0 \sqrt{1 + \frac{R_2 R_{12} R_{17}}{R_1 R_{11} R_{19}} \left(1 + \frac{R_5}{R_6}\right)} \; ;$$

$$H_{OLP} = \left(-\frac{R_{10}}{R_{17}}\right) \left(1 + \frac{R_2 R_{12} R_{17}}{R_1 R_{11} R_{19}} \left(1 + \frac{R_5}{R_6}\right)\right)$$

$$\frac{R_3}{R_1} = \frac{R_{18}}{R_{17}}$$

Highpass —

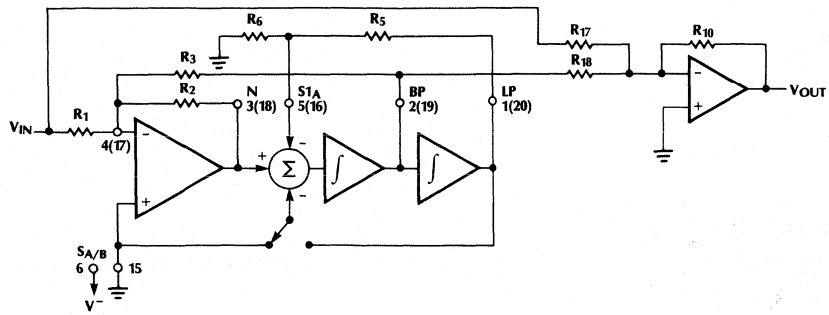


$$f_0 = \frac{f_{CLK}}{100(50)} \sqrt{\frac{R_6}{R_5 + R_6}} \; ; \; Q = \frac{R_3}{R_2} \sqrt{\frac{R_6}{R_5 + R_6}}$$

$$f_Z = f_0 \sqrt{1 - \frac{R_2 R_{12} R_{17}}{R_1 R_{11} R_{19}} \left(1 + \frac{R_5}{R_6}\right)} \; ; \; H_{OHP} = -\frac{R_{10}}{R_{17}}$$

$$\frac{R_3}{R_1} = \frac{R_{18}}{R_{17}}$$

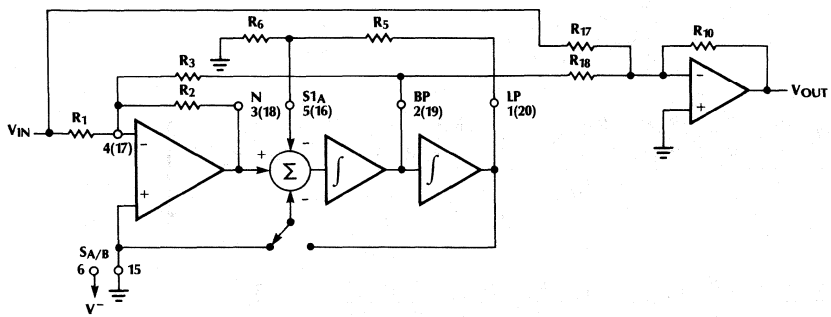
Allpass —



$$f_0 = f_z = \frac{f_{CLK}}{100(50)} \sqrt{\frac{R_6}{R_5 + R_6}} \; ; \; Q = \frac{R_3}{R_2} \sqrt{\frac{R_6}{R_5 + R_6}}$$

$$H_{OAP} = -\frac{R_{10}}{R_{17}} \; ; \; \frac{R_{17}R_3}{R_{18}R_1} = 2$$

Notch —



$$f_N = \frac{f_{CLK}}{100(50)} \sqrt{\frac{R_6}{R_5 + R_6}} \; ; \; Q = \frac{R_3}{R_2} \sqrt{\frac{R_6}{R_5 + R_6}}$$

$$H_{ON1} \; (f \rightarrow 0) = H_{ON2} \; (f \rightarrow f_{CLK}/2) = -\frac{R_{10}}{R_{17}} \; ; \; \frac{R_3}{R_1} = \frac{R_{18}}{R_{17}}$$

Appendix B. Derivation of Flexible Building Block Transfer Function

$$V_N = -\frac{R_2}{R_1} V_{IN} - \frac{R_2}{R_3} V_{BP}$$

$$V_{BP} = \frac{\left(V_N - \frac{R_6}{R_5 + R_6} V_{LP}\right)}{s} \omega_1$$

$$V_{LP} = \frac{V_{BP}\, \omega_1}{s}$$

$$\frac{s\, V_{BP}}{\omega_1} = -\frac{R_2}{R_1} V_{IN} - \frac{R_2}{R_3} V_{BP} - \frac{R_6}{R_5 + R_6} \frac{V_{BP}\, \omega_1}{s}$$

$$V_{BP}\left[\frac{s}{\omega_1} + \frac{R_2}{R_3} + \frac{R_6}{R_5 + R_6} \frac{\omega_1}{s}\right] = -\frac{R_2}{R_1} V_{IN}$$

$$\frac{V_{BP}}{V_{IN}} = \left(-\frac{R_3}{R_1}\right) \frac{\frac{R_2}{R_3} s\omega_1}{s^2 + \frac{R_2}{R_3} s\omega_1 + \frac{R_6}{R_5 + R_6} \omega_1^2}$$

$$V_O = -\frac{R_{10}}{R_{17}} V_{IN} - \frac{R_{10}}{R_{18}} V_{BP} + \frac{R_{12}}{R_{11}} \frac{R_{10}}{R_{19}} V_{LP}$$

$$f_1 = \frac{f_{CLK}\, 2\pi}{50} \qquad H_{OBP} = -\frac{R_3}{R_1}$$

$$f_0 = \sqrt{\frac{R_6}{R_5 + R_6}} \frac{f_{CLK}\, 2\pi}{50} \qquad Q = \frac{R_2}{R_3} \sqrt{\frac{R_6}{R_5 + R_6}}$$

$$\omega = 2\pi f$$

$$V_O = -\frac{R_{10}}{R_{17}} V_{IN} - \frac{R_{10}}{R_{18}}\left(-\frac{R_2}{R_1}\right) \frac{s\omega_1\, V_{IN}}{s^2 + \frac{R_2}{R_3} s\omega_1 + \frac{R_6}{R_5 + R_6} \omega_1^2} + \frac{R_{12} R_{10}}{R_{11} R_{19}}\left(-\frac{R_2}{R_1}\right) \frac{\omega_1^2\, V_{IN}}{s^2 + \frac{R_2}{R_3} s\omega_1 + \frac{R_6}{R_5 + R_6} \omega_1^2}$$

$$V_O = \left(-\frac{R_{10}}{R_{17}}\right)\left[\frac{s^2 + \frac{R_2}{R_3} s\omega_1 + \frac{R_6}{R_5 + R_6} \omega_1^2 - \frac{R_{10} R_2 R_{17}}{R_{18} R_1 R_{10}} s\omega_1 + \frac{R_{12} R_2 R_{17}}{R_{11} R_1 R_{19}} \omega_1^2}{s^2 + \frac{R_2}{R_3} s\omega_1 + \frac{R_6}{R_5 + R_6} \omega_1^2}\right]$$

$$\frac{V_O}{V_{IN}} = \left(-\frac{R_{10}}{R_{17}}\right)\left[\frac{s^2 + \frac{R_2}{R_3}\left(-\frac{R_{10}}{R_{17}}\right)\left[\frac{R_{10} R_3}{R_{18} R_1} - \frac{R_{10}}{R_{17}}\right] s\omega_1 + \left[1 + \frac{R_2 R_{12} R_{17}}{R_1 R_{11} R_{19}}\left(1 + \frac{R_5}{R_6}\right)\right] \frac{R_6}{R_5 + R_6} \omega_1^2}{s^2 + \frac{R_2}{R_3} s\omega_1 + \frac{R_6}{R_5 + R_6} \omega_1^2}\right]$$

$$\frac{V_O}{V_{IN}} = \left(-\frac{R_{10}}{R_{17}}\right)\left[\frac{s^2 + \frac{R_2}{R_3}\left[1 - \frac{R_{17}}{R_{18}} \frac{R_3}{R_1}\right] s\omega_1 + \left[1 + \frac{R_2 R_{12} R_{17}}{R_1 R_{11} R_{19}}\left(1 + \frac{R_5}{R_6}\right)\right] \frac{R_6}{R_5 + R_6} \omega_1^2}{s^2 + \frac{R_2}{R_3} s\omega_1 + \frac{R_6}{R_5 + R_6} \omega_1^2}\right]$$

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Application Note 5

ML2200, ML2208 Software Driver

1.0 Introduction

This application note presents a very simple software driver for the ML2200/ML2208 Data Acquisition Peripheral. As mentioned in the data sheet, under section 6.0 "Methods of Data Transfer to the Microprocessor", there are several ways to handle the A/D converted data output from the ML2200/ML2208; 1) Data on Demand, 2) Polling; 3) Interrupt, or 4) DMA. This application note presents a driver for Data on Demand.

An application using Data on Demand requires the A/D converted data at arbitrary times, as opposed to the other three methods of data transfer which requires the microprocessor to periodically read the data. The ML2200/ML2208 operating in a Data on Demand mode is not running continuously. Data on Demand would be more characteristic of a data acquisition application rather than a signal processing application which would need to sample a signal periodically in order to be able to reconstruct it.

The driver is written in pseudo code, which is no particular language but should be easily translatable to any computer language. It is a step-by-step process of reading and writing values to ML2200/ML2208 registers.

Four modules are covered: Initialization, Activate Conversion and Read Data, Self Test Diagnostic, Self Calibration Diagnostic, Power Down and Power Up Modules. Initialization covers power-up procedures and optionally may call Self Test and Self Calibration Diagnostic modules. Activate Conversion is the steady state module that is called each time the A/D data is desired. Power Down and Power Up are used only if this capability is desired.

Initialization Mode (Power-On Initialization)

1)	Power on	
2)	Write (40H) to Control Register	; Reset
3)	Write (80H) to Control Register	; Set Calibration
4)	Wait 16,520 external clocks	
5)	Read Status Register	
6)	Is CLCP = 1, Yes: continue, No: go back to step 5	
7)	Write (40H) to Interrupt Acknowledge Register	; CLCPAK
–)	Call (Self Calibration Diagnostic Module)	; OPTIONAL
		; Use Program shown on last page figure 1
8)	Write (88H) to Index Register	; Point to first
9)	Write (08H) Window High Reg	; instruction RAM use
10)	Write (26H) Window Low Reg	; auto increment
11)	Write (01H) Window High Reg	
12)	Write (26H) Window Low Reg	
13)	Write (02H) Window High Reg	
14)	Write (26H) Window Low Reg	
15)	Write (03H) Window High Reg	
16)	Write (26H) Window Low Reg	
17)	Write (04H) Window High Reg	
18)	Write (26H) Window Low Reg	
19)	Write (05H) Window High Reg	
20)	Write (26H) Window Low Reg	
21)	Write (06H) Window High Reg	
22)	Write (26H) Window Low Reg	
23)	Write (87H) Window High Reg	
24)	Write (26H) Window Low Reg	

10

25) Write (0AH) to Control Reg ; set MSTR bit so
; that pulse goes out
; each conversion and
; put in DMA mode to
; facilitate reading
; data.
26) Write (0BH) to Control Reg ; Set Run bit
27) Call (Self Test Diagnostic Module) ; OPTIONAL

; end of initialization module.

Activate Conversion and Read Data Module

(Called each time A/D converted data is desired)

1) Read status register
2) Is ISQ = 1? Yes: continue, No: go back to step 1
3) Write (10H) to Interrupt Acknowledge Reg ; acknowledge ISQ
4) Wait (8 × 31.4 μs = 251.2 μs)
5) Read status register
6) DBR = 1? Yes: continue; No: go back to step 5
7) Read Window Low Register save as High Byte ; DMA mode allows
Read Window Low Register save as Low Byte ; μP to read High and
8) Go back to step 7 seven more times ; Low bytes at same
9) Return ; address

Self Test Diagnostic Module

(Assumes the program in figure 1 is already loaded in the Instruction RAM as performed in the initialization module. When the SLFT bit is set, the diagnostic program is the same one as shown on page 22 of the data sheet. This module sets the SLFT bit, starts a conversion, then checks the data for the results.)

1) Read Control Register
2) Or (20H) ; Set SLFTST in
; Control Register
3) And (7FH) ; don't set CAL bit
4) Write back into control register
5) Call (ACTIVATE CONVERSION AND READ DATA MODULE)
6) Check selftest data ; Data 0 = 0
; Data 1 = +1
; Data 2 = –1
; Data 3 = 0

(Note: these values may not be exact due to the potential noise in the system)

7) Read Control Register
8) And (5FH) ; clear SLFT bit
9) Write back into control register
10) Return

Self Calibration Diagnostic Module

(This can be used to verify that the part is properly calibrated. It should be called between steps 7 and 8 in the initialization module. This test is not necessary since each production part is fully tested before it is shipped.)

1) Write (08H) to Index Register ; Point to the first
2) Write (88H) to Window High Register ; Instruction
3) Write (60H) to Window Low Register ; Load with RDCAL
4) Write (01H) to Control Register ; Set RUN bit
5) Read Status Register ; Wait for ISQ
6) Is ISQ = 1? Yes: continue, No: go back to step 5
7) Write (10H) to Interrupt Acknowledge Register ; Start Program
8) Read Status Register
9) Is DBR = 1? Yes: continue, No: go back to step 8 ; Wait for Data
10) Write (00H) to Index Register ; Point to Data
11) Read Window Low Register
12) Is Data = 0FFH? Yes: Failed Calibration, No: continue
13) Write (00H) to Control Register ; Take out of Run Mode
14) Return

Power Down Module

1) Read Control Register ; Clear the Run Bit
2) And with (7EH)
3) Write Control Register
4) Read Status Register and Process any conditions
5) Write (0FFH) to Interrupt Acknowledge Register ; Clear all Interrupt
6) POWER DOWN (PDN pin goes low) ; Conditions
7) Return

Power Up Module (Coming from a Power Down State)

1) POWER UP (PDN pin goes high)
2) Wait (10 msec)
3) Read Control Register ; Set the Run Bit
4) Or with (01H)
5) And with (7FH)
6) Write to Control Register
7) Return

	Last	ALRMEN	Mode	CHAN	Cycle	Gain	REF
SEQ0	0	0	Intra Sequence Pause	CH0	13	1	Internal
SEQ1	0	0	Immed Execute	CH1	13	1	Internal
SEQ2	0	0	Immed Execute	CH2	13	1	Internal
SEQ3	0	0	Immed Execute	CH3	13	1	Internal
SEQ4	0	0	Immed Execute	CH4	13	1	Internal
SEQ5	0	0	Immed Execute	CH5	13	1	Internal
SEQ6	0	0	Immed Execute	CH6	13	1	Internal
SEQ7	1	0	Immed Execute	CH7	13	1	Internal

Figure 1. ML2208 Program Used in Driver

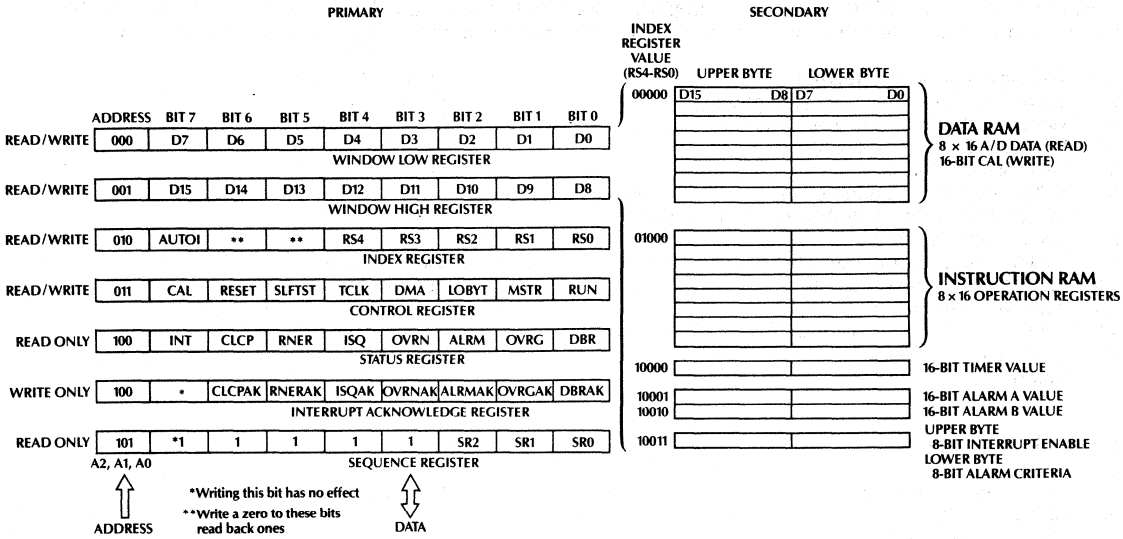

Figure 2. ML2200/ML2208 Registers

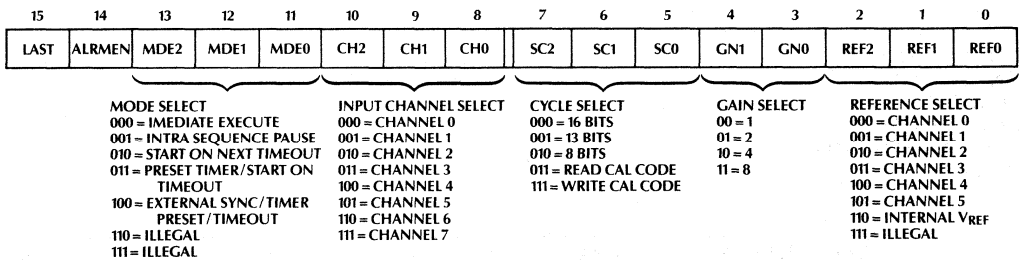

Figure 3. ML2208 Bit Map of Instruction RAM

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Application Note 6

Vince Cardinale

Fiberoptics

Introduction

Although fiberoptic technology has been around for some time, its cost and the lack of standardization has hindered its widespread application, until recently. The introduction of new integrated circuits developed specifically for fiberoptic systems has lowered the costs, making fiberoptic links more competitive. Applications in Telephony, LANs, WANs, and point to point high speed interfaces, have helped make fiberoptics one of the fastest growing segments in the electronics market.

Micro Linear's fiberoptic products can be used to implement a range of different fiberoptic interfaces. Data rates up to 100 Megabaud which are compatible with ECL or TTL are achievable using a single 5 volt supply. Most of the applications for these products require bandwidths above 1MHz, where the quality of the interface can be compromised with a poor implementation. With this in mind, having a thorough understanding of fiberoptics will significantly contribute to the success of a circuit design. This application note will address the transmit and receive circuits, some important PC board layout techniques, and will conclude with a sample circuit and board layout.

Fiberoptics

Fiberoptic systems have several key advantages over their wire equivalents, which account for the continued effort to make them practical in more applications. The most significant advantage is the low level of attenuation seen with high frequency signals. This feature allows a higher degree of multiplexing than is achievable using wire. This is exactly what is needed for long distance telephone lines and computer networks. Other attractive features include a lack of RFI radiation and a low sensitivity to EMI noise. These characteristics make it easier to meet FCC regulations and increase the security of data transmissions.

In a fiberoptic system (figure 1) digital data is coded into a serial bit stream represented by bursts of light from a laser diode or LED. This light is channeled by the fiber to a PIN photodiode at the receiver which is sensitive to the frequency of the light transmitted. Because light effects the reverse current flow through a PIN photodiode, a transimpedance amplifier is required to convert this current to a voltage and boost the low level signal to something usable. A quantizing circuit usually follows because variable fiber lengths and conditions will distort the signal. The Quantizer squares the signal and conforms to standard interface levels (ECL or TTL).

Fiberoptics is not a perfect interface, though. The signal level can be attenuated by insertion loss at the transmitter and receiver, connector loss, and transmission loss. These losses limit the maximum length of the fiber and affect the requirements of the transmitter and receiver. In order to accommodate a worst case situation, a flux budget should be developed so that minimum circuit performance levels can be ascertained.

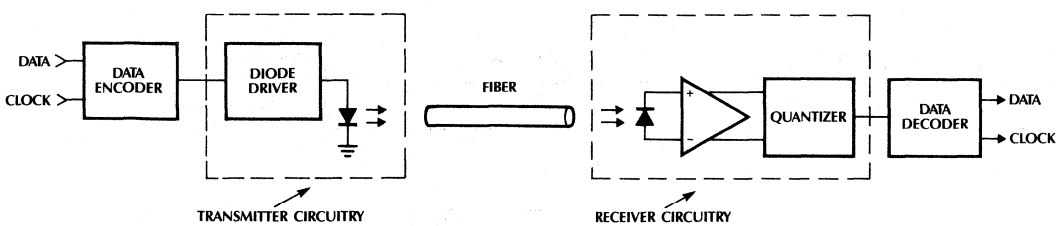


Figure 1.

Defining a Flux Budget

$$10 \log \left(\frac{\phi_T}{\phi_R}\right) = \alpha_O L + \alpha_{TC} + \alpha_{CR} + n\alpha_{CC} + \alpha_M$$

A flux budget is a mathematical representation of the optical power in a fiberoptic system. It accounts for connector losses, attenuation due to fiber length, and a safety margin defined by the designer. Defining this budget is one of the first things that should be done when designing a fiberoptic link.

Each of the terms is defined as follows:

ϕ_T is the flux (μW) available from the transmitter
ϕ_R is the flux (μW) required by the receiver
α_O is the fiber attenuation constant (dB/km)
L is the fiber length (km)
α_{TC} is the transmitter-to-fiber coupling loss (dB)
α_{CC} is the fiber-to-fiber loss (dB) for in-line connectors
n is the number of in-line connectors
α_{CR} is the fiber-to-receiver coupling loss (dB)
α_M is the safety margin (dB)

A graphical representation of the flux budget is shown in figure 2. Option (a) depicts the use of in-line connectors. Option (b) is without them.

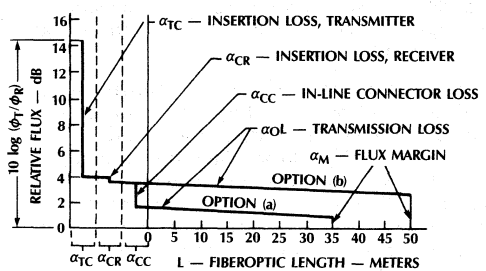


Figure 2.

To keep power consumption at a minimum, the appropriate starting point is the minimum acceptable signal level at the receiver. This minimum received power level, summed with several interface losses gives the minimum output power of the LED. If the fiber length can vary in a given system then the dynamic range of the receiver is important and the maximum received power must also be calculated.

Dynamic Range

The dynamic range of the receiver must be large enough to accommodate all the variables a system may present. Figure 3 shows an example dynamic range calculation for transmission distances ranging from 10 meters to 1000 meters with 12.5dB/km cable, and up to two in-line connectors.

α_{LED} = LED output variation	=	7.0dB
α_{LDC} = LED driver variation	=	2.2dB
$\alpha_O L$ = 1km × 12.5dB/km	=	12.5dB
$n\alpha_{CC}$ = 2 × 2dB	=	4.0dB
α_M	=	3.0dB
Thermal Variations	=	1.0dB
Dynamic Range		29.7dB

Figure 3.

The Circuit Design

The combination of low receiver input sensitivity with significant dynamic range requires the receiver to have two important features: amplitude control and AC coupling.

An offset voltage in the receiver will reduce its sensitivity by not allowing low level signals to trigger the digital output circuit. The circuit in figure 4 contains both AC coupling between the transimpedance and limiting amplifiers, and a DC restoration loop around the limiting amplifiers. These two features keep the offset voltage through the receiver to an absolute minimum, thus maximizing sensitivity.

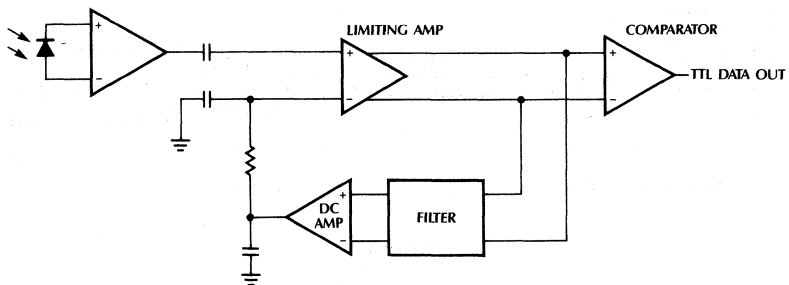


Figure 4.

In order to handle a wide dynamic range, like 50dB, special attention must be given to the receiver circuit design. Applying a large input signal to a typical amplifier can cause the transistors in the signal path to saturate resulting in pulse width distortion and reduced bandwidth. Some technique of controlling the amplitude must be incorporated in order to protect the signal integrity.

Amplitude control can be achieved with either an AGC circuit or with the use of limiting amplifiers. An AGC circuit keeps the transistors out of saturation by reducing the gain of the circuit as the signal amplitude increases. A limiting amplifier simply limits the signal amplitude to a point before saturation. This technique results in a simpler, higher bandwidth design and so was chosen by Micro Linear.

Data Format

The data format is important since it affects the bandwidth and duty cycle which the interface must accomodate. There are many ways to code data in a serial format. Some codes allow unlimited consecutive symbols while others do not. Those that do not are called Run-Length-Limited (RLL) codes. A fiberoptic interface which incorporates AC coupling to increase sensitivity can only pass RLL type codes. The particular run-length-limited code chosen must be considered carefully since it will affect the bandwidth of the system.

Manchester code is popular in AC coupled systems because it has a 50% duty cycle and can be encoded and decoded with relatively simple circuits. In Manchester code two symbols are used for each bit transmitted. This doubles the fundamental frequency which the interface must handle. A more efficient RLL code is 4B5B. This code uses 5 symbols to send 4 bits. This represents an increase in efficiency from 50% (Manchester) to 80% (4B5B). A fiberoptic interface which will transmit 40 Megabits per second using 4B5B coding must accomodate 50 Megabaud (symbols per second). Since there are always 2 symbols per cycle the minimum system bandwidth is 25 Megahertz. If Manchester code was used to transmit 40 Megabits per second the interface would have to handle 80 Megabaud or a minium bandwidth of 40 Megahertz.

Bandwidth

From the example just described you can see how the code chosen effects the minimum bandwidth of the fiberoptic interface to be designed. The optimum system bandwidth is actually somewhat higher though due to four conflicting concerns: noise, intersymbol interference, power, and bit error rate.

If an interface were designed with a 3dB bandwidth equal to the minimum bandwidth as described above, level transitions would be smooth, like a sine wave. This is not desirable for a digital signal. Also, smooth rise and fall times will cause interference between adjacent symbols resulting in a distortion of the output signal. This is known as intersymbol interference. A fiberoptic interface with a higher bandwidth will have faster rise and fall times and less intersymbol interference. On the other hand, a higher bandwidth will increase the noise on the output signal. When you combine these two opposing effects with the desire for low power and a low BER (Bit Error Rate) (which also conflict), an optimum bandwidth can be derived. The curve in figure 5 indicates the optimum bandwidth is about 50% higher than the minimum bandwidth.

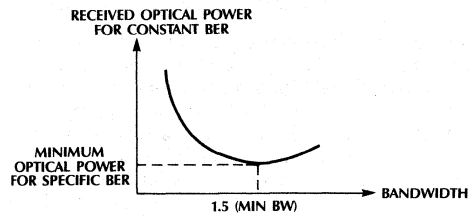


Figure 5.

Transmitter Design

The light source can be either a laser diode or an LED. Because a laser diode has such a narrow spectrum of radiant light it is called a Single Mode light emitter. Multi Mode light emitters radiate a wider spectrum of light. LEDs are Multi Mode and as such suffer from a higher level of chromatic dispersion, caused by different propagation velocities for light of different wavelengths. This is the dominant bandwidth limiting factor for LED driven fiberoptic links. Light emitting diodes have an emission spectrum on the order of 40 to 60nm full width at half maximum amplitude centered at 820nm. On the other hand, LEDs are much cheaper than laser diodes and can be modulated in the 100MHz range, making them suitable for short to medium distance communications such as LANs and point-to-point computer interfaces.

LEDs are current driven devices so a current modulation circuit is needed to use the LED as a data transmitter. In applications where the data rate is less than 10MHz a circuit similar to figure 6 will be adequate to drive the LED without a significant amount of pulse width distortion. Unfortunately, LEDs do not turn on or off linearly nor are their rise and fall times equal. For data rates above 10MHz these characteristics need to be considered in order to get the best possible performance.

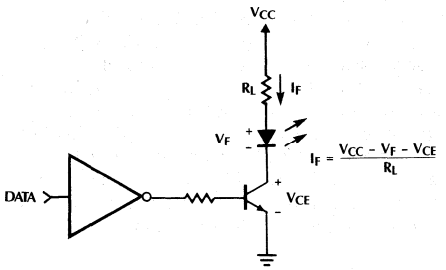
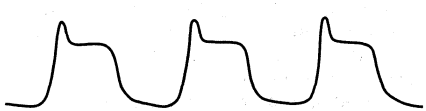


Figure 6.

Two techniques which can be used to improve the turn-on time of an LED are "pre-bias" and "drive current peaking". Pre-bias is a small forward voltage applied to the LED in the "off" state. This voltage prevents the junction and parasitic capacitances from discharging completely when the LED is in the "off" state, thus reducing the amount of charge that the driver must transfer to turn the emitter back on. Drive current peaking is a momentary increase in LED forward current that is provided by the driver during the rising and falling edges of the current pulses that are used to modulate the emitter. The time constant of this peaking circuit needs to be equal to the minority carrier lifetime of the emitter so that the rise and fall times will be improved without causing excessive overshoot of the optical pulses. Figure 7 shows the problems which can result from excessive peaking.



OPTICAL OVERSHOOT DUE TO EXCESSIVE PEAKING OF THE LED DRIVE CURRENT

Figure 7.

The circuit in figure 8 implements both the pre-bias and peaking techniques described above. When the DATA signal is low the voltage divider created by R_1 and R_2 can be set-up so the voltage between R_1 and R_2 is slightly less than the LED turn-on voltage. This pre-bias voltage prevents the LED capacitance from discharging completely which allows the LED to turn on faster because less time is required to completely charge the junction capacitance. The time to completely charge the LED can be reduced further by increasing the amount of current flowing in the LED duirng turn-on. The capacitor in this circuit has the effect of connecting R_3 in parallel with R_2 for a short time during level transitions. This momentary condition allows additional current to flow through R_3 and the LED. By matching the R_3C time constant to the minority carrier lifetime of the LED, *peak* performance is achieved.

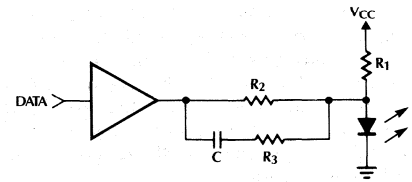


Figure 8.

LEDs are characteristically harder to turn off than to turn on. This phenomenon is commonly refered to as the long-tailed response, and is depicted in figure 9 as it relates to transmitted optical power. Circuits such as the one in figure 6 exhibit this problem because there is no low impedance path to dissipate the stored charge in the LED when turning off. In order to compensate for this an active pull down configuration should be used. For the circuit in figure 8, this can be achieved by using an input buffer with a totem pole output structure. When the DATA signal is low, the lower transistor of the totem pole is active. Acting as a current sink, this device provides a low impedance path for the charge stored in the LED junction, reducing pulse-width distortion and the magnitude of the long tail.

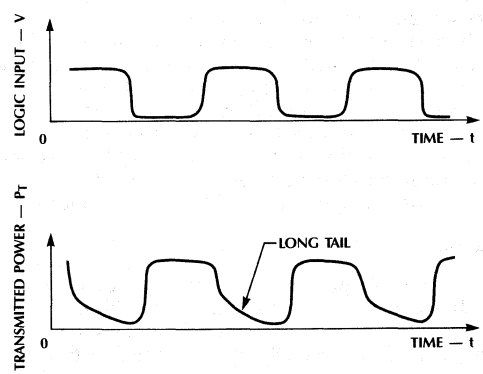


Figure 9.

The ML4631 LED Driver

The ML4631 (figure 10) uses a circuit topology similar to figure 8. With no external components this circuit will provide 60mA DC forward current to the LED during the "on" state and maintains a pre-bias voltage of about 1.1V during the "off" state. By adding a small external capacitor, the peaking effect described earlier can be induced. A proprietary high speed driver, utilizing schottky devices and a clamped internal supply, is used to drive the RC network. An enable pin is provided for gating the DATA signal. The output of the Driver is capable of sinking or sourcing 100mA at 100MBd.

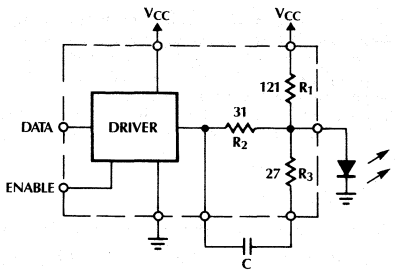


Figure 10.

Because all the nodes around the resistors are available to the user, the LED forward current can easily be modified using the following equations

$$R_1 = \frac{V_{CC} - 4.7V_F + 10.73}{I_F} \quad (1)$$

$$R_2 = \frac{R_1}{3.7} - 2 \quad (2)$$

$$R_3 = R_2 - 4 \quad (3)$$

$$C = \frac{2ns}{R_2 + R_3} \quad (4)$$

In equation 1, V_F is the forward voltage drop of the LED when a forward current of I_F is passed through it. The values for R_1, R_2, and R_3 were chosen for the ML4631 by setting I_F to 60mA, V_F to 1.8V and solving the above equations. Since the forward voltage drop of an LED is related to the forward current, a graph of their relationship is usually provided in the LED data sheet. The graph of I_F vs V_F for the Hewlett Packard HFBR-1414 is shown in figure 11. If a different forward current is desired, the corresponding forward voltage drop should be used in equation 1.

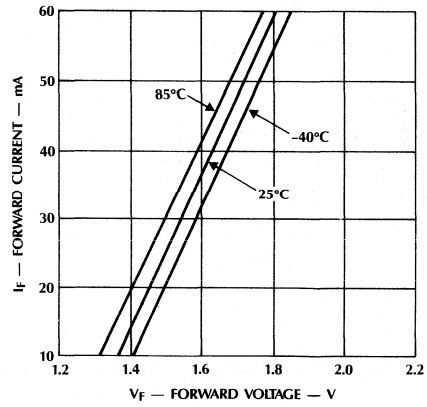


Figure 11.

Different configurations can be used to set the DC current up to approximately 100mA. Since the forward current supplied to the LED comes not only from the Driver output but also from V_{CC} through R_1, it would appear the maximum I_F achievable is more than the 100mA output spec of the Driver. However, because of the additional peaking current and the tolerance on the output drive current, the practical design limit is typically about 100mA.

Operating the ML4631 as shown in figure 10 will produce an LED forward current of about 60mA ± 35%. This range is mainly due to the 20% tolerance of the resistors in the output stage. Using one or two 1% external resistors will substantially improve the accuracy of I_F. Figure 12 shows several configurations with various I_F levels and accuracies. Each of these examples uses at least one on-chip resistor, usually configured as the R_3 in figure 8. Since R_3 affects only the peaking current, its accuracy is less critical and does not affect the steady state forward current at all. For complete flexibility, the high speed Driver output is available to drive an external RC network.

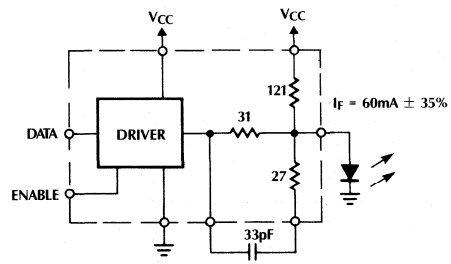


Figure 12a.

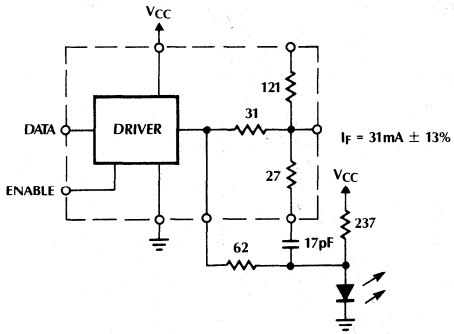


Figure 12b.

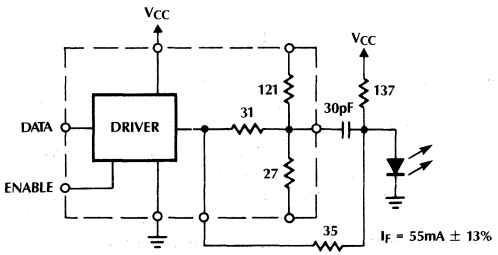


Figure 12c.

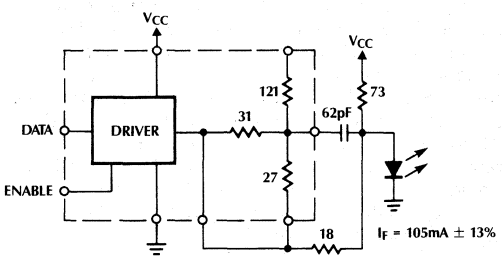


Figure 12d.

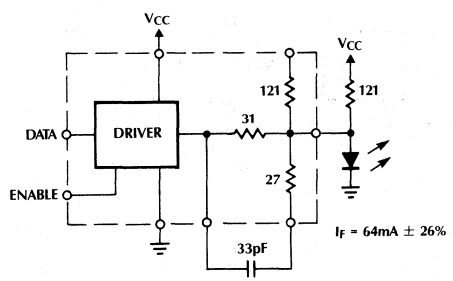


Figure 12e.

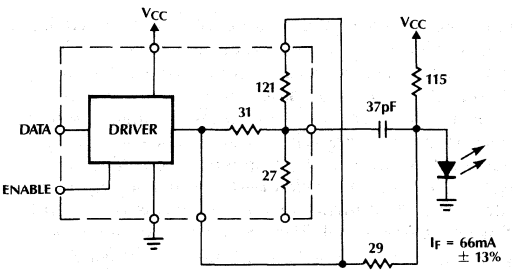


Figure 12f.

Note: Tolerance calculations were made with the following assumptions:
1) On-chip resistor tolerance is ±35% to account for process and temperature variations over 0–70°C.
2) Off-chip resistor tolerance is ±1%.
3) Power supply is 5.0V ± 10%. A 5V ± 5% supply will improve the I_F tolerance values shown above by ±3%.
4) V_F = 1.8V.

Receiver Design

For optimum performance the receiver needs to combine a wide dynamic range (about 50dB), high sensitivity (down to 1μW), high bandwidth (50MHz) and compatibility with standard digital interfaces (ECL or TTL). Another feature which is required in some fiberoptic systems is a Link Monitor. This circuit monitors the input level and sets a flag and/or disables the digital output when the input falls below a predetermined point.

The four major functional blocks of a receiver are the optical to current conversion, the current to voltage conversion, the analog to digital conversion, and the Link Monitor. A PIN photodiode and a transimpedance amplifier can be used to perform the first two functions while the third and fourth require several discrete standard devices and a significant amount of design effort or one of Micro Linear's Quantizer products.

There are several manufacturers of discrete PIN photodiodes and transimpedance amplifiers which are suitable for this application. Some of these manufacturers offer both functions in a single module compatible with fiberoptic connectors. These modules, like the Hewlett Packard HFBR-24X6, isolate the most noise sensitive section of the receiver, the PIN photodiode to transimpedance amplifier connection, and protect it from outside influences. In addition, they are relatively low cost, and eliminate the need to design the fiberoptic connector hardware.

The output of these receiver modules is a low level analog voltage which is directly proportional to the incident optical power. This signal needs to be amplified, squared-off, and appropriately level shifted (for ECL or TTL outputs). As described earlier, a limiting amplifier can be used in this application to accomodate a wide input dynamic range while maintaining a high bandwidth.

Building a high speed analog to digital conversion circuit which must perform over a wide dynamic range with low offsets using off-the-shelf components is difficult. Furthermore, a worst case analysis may be impossible because some of the parameters critical to a fiberoptic receiver design, such as input offset and input referred noise are not always included in the discrete component specifications. The typical bandwidth of these devices may be known but the minimum is not always guaranteed, yet this is required for a worst case analysis.

The ML4621, ML4622, and ML4623 Quantizers

The ML4621, ML4622, and ML4623 Quantizers eliminate these problems by providing a monolithic solution. All three products include a limiting amplifier front end, a comparator output section and a Link Monitor. The ML4621 is the most flexible circuit. The differential data path between the amplifier section and the comparator section is available to the user for filtering or wave shaping. In addition, both ECL and TTL outputs are available, and the Link Monitor peak detector can be controlled with an external current source or the value of the peak detector capacitor.

The ML4622 and ML4623 are more application specific. The ML4622 has an ECL output while the ML4623 has a TTL output. In both products the node between the amplifier and comparator is not brought out to the user, and the Link Monitor peak detector can be controlled only by the value of the peak capacitor. Like the ML4621, the ML4622 (ECL output) was optimized for speed (65MHz typical) while the ML4623 (TTL output) was optimized for low power (40mA typical). Both fit in a 16 pin SOIC package.

Input Amplifier Section

All of the Quantizer products have a two stage limiting amplifier with a DC restoration feedback loop. Figure 13 shows this input circuitry in detail. The two input coupling capacitors C_1 and C_2 perform two important functions. First they eliminate any offset voltage created by the transimpedance amplifier, and in addition they create a high pass filter at the input of the Quantizer. This filter establishes the low corner frequency, f_L, of the Quantizer's 3dB bandwidth.

$$f_L = \frac{1}{2\pi\ 8000\ C} \qquad (C = C_1 = C_2) \qquad (5)$$

8000 represents the parallel combination of the DC bias setting resistors 10K and 35K. Using a 0.1μF capacitor for C_1 and C_2 establishes a corner frequency at about 200Hz. C_4 and C_5 control the high corner frequency, f_H.

$$f_H = \frac{1}{2\pi\ 425\ C} \qquad (C = C_4 = C_5) \qquad (6)$$

425 represents the internal impedance at nodes CF1 and CF2. Using a 20pF capacitor for C_4 and C_5 establishes a corner frequency at about 19MHz. If CF1 and CF2 are left open the high corner frequency will be >50MHz for the ML4621 and ML4622, or >40MHz for the ML4623.

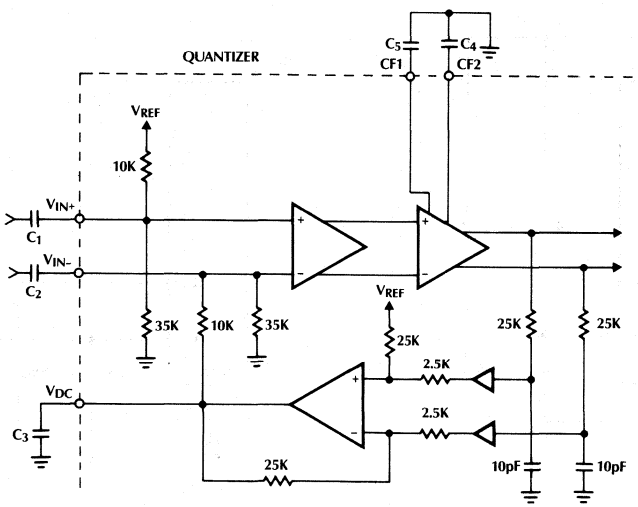


Figure 13.

The bandwidth of the receiver, as defined by $f_H - f_L$, can be adjusted to the particular needs of different systems. The high pass filter not only eliminates DC offsets but also reduces any low frequency power supply noise picked-up in the transimpedance amplifier and associated traces. The low pass filter reduces high frequency noise which directly effects the signal to noise ratio and thus the sensitivity of the receiver. Since these circuits were designed for maximum bandwidth, some band limiting should be used as indicated in figure 5 to maximize sensitivity.

Although the input is AC coupled, the offset voltage *within* the limiting amplifiers will be present at V_{OUT+} and V_{OUT-}. This is represented by V_{OS} in figure 14. In order to reduce this error a DC feedback loop is incorporated. First, the DC component of V_{OUT+} and V_{OUT-} is developed through an RC filter of 25K and 10pF. Then a difference amplifier circuit with a gain of 10 is used to provide a single ended signal, stored in C_3, which can be fed back into the inverting input terminal. This negative feedback loop nulls the offset voltage, forcing V_{OS} to be zero.

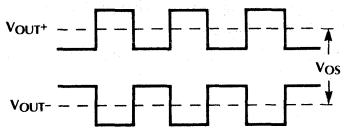


Figure 14.

Although the value of C_3 is non-critical, the pole it creates can effect the stability of the feedback loop. In order to avoid any stability problems the value of C_3 should be at least 100 times smaller than C_1 and C_2. In some systems C_3 can actually be eliminated due to the dominant effect C_1 and C_2 have on the loop.

The limiting amplifiers have a maximum output voltage swing of about $700mV_{P-P}$. Since the gain of the amplifiers is 75, input signals greater 9mV will be clipped at about 2.7V and 3.4V. Typically this signal is connected directly to the comparator inputs, as in the ML4622 and ML4623. If some filtering or wave shaping is desired between the amplifier output and the comparator input, the ML4621 should be used since these nodes are brought out to pins. If AC coupling is involved, the DC bias must be reestablished between (GND + 2V) and (V_{CC} - 1V). Also, the loading on V_{OUT+} and V_{OUT-} should be kept below 3mA, and be aware that CMP+ and CMP– will sink about 25μA.

Output Comparator Section

The ML4621 has both ECL and TTL outputs. If the ECL output is to be used, the power to the TTL output section can be removed by connecting V_{CC} TTL and GND TTL to V_{CC}. This will reduce the V_{CC} supply current by 5 to 10mA. The Quantizer can be powered by –5.2V (V_{CC} = 0V and GND = –5.2V), which produces standard ECL output levels, or +5V (V_{CC} = +5V and GND = 0V), providing raised ECL levels. The ECL outputs on the ML4621 can source up to 10mA, so a 200Ω load tied to –2V (below V_{CC}) can be accommodated. If a –2V supply is not available, connecting the ECL output to GND through a 510Ω resistor, and to V_{CC} through a 330Ω resistor will provide the same voltage swing as 200Ω tied to –2V (see figure 15). If the standard ECL load of 50Ω tied to –2V is required the ML4622 can be used.

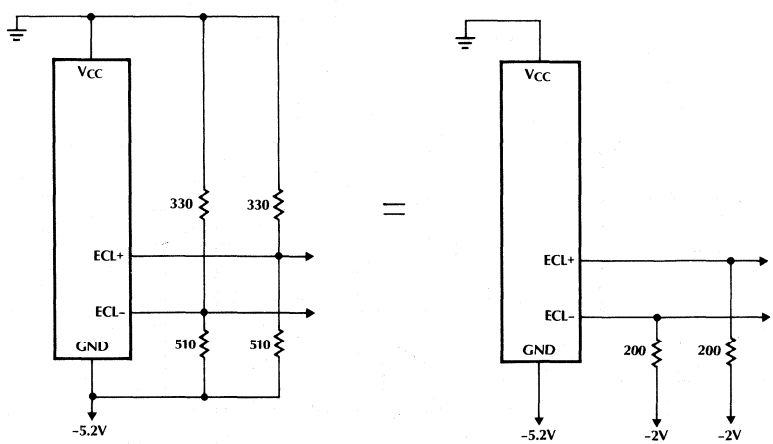


Figure 15.

The output comparator is gated with the $\overline{\text{CMP ENABLE}}$ pin which is active low. When $\overline{\text{CMP ENABLE}}$ is high, ECL+ is held high, ECL– is held low, and TTL OUT is held high. If the Quantizer is powered by +5V and ground then any external TTL compatible signal can be used to control this pin. If a –5.2V supply is used, the signal should be appropriately level shifted. In either case, the $\overline{\text{TTL LINK MON}}$ pin can be used to drive the $\overline{\text{CMP ENABLE}}$ pin directly. The $\overline{\text{TTL LINK MON}}$ is an output signal from the Minimum Signal Discriminator circuit providing the Link Monitor function.

Link Monitor Section

The $\overline{\text{TTL LINK MON}}$ and $\overline{\text{ECL LINK MON}}$ pins both provide an output signal indicating when the input data signal is below a user defined acceptable level. Under normal operating conditions this output will be low, indicating the data is of acceptable amplitude. The voltage levels on the $\overline{\text{TTL LINK MON}}$ pin are TTL compatible if the power supply is +5V. With a –5.2V supply the $\overline{\text{ECL LINK MON}}$ output pin will provide single ended ECL levels. The $\overline{\text{TTL LINK MON}}$ pin can also be used to drive an LED, providing a visible link status indicator. This pin can sink up to 10mA.

The Minimum Signal Discriminator circuit contains a peak detector, a comparator, and output level shift circuitry (figure 16). The droop rate of the peak detector is:

$$\frac{dV}{dt} = \frac{I_{ISET}}{C_6} \qquad (7)$$

The peak detector droop rate can be controlled adjusting either the value of C_6 at the C_{PEAK} pin or I_{ISET} at the I_{SET} pin. If I_{NOM} is connected to I_{SET}, I_{ISET} will be 125μA. The ML4622 and ML4623 make this connection internally so I_{NOM} and I_{SET} are not available to the user. The droop rate for these products can be adjusted with C_6. The ML4621 has these extra pins, which allows the user to set I_{ISET} with an external resistor, R_{EXT}, tied between I_{SET} and V_{CC}. I_{ISET} would then be:

$$I_{ISET} = \frac{V_{CC} - 0.7}{R_{EXT} + 1700} \qquad (8)$$

The output of the peak detector is a DC voltage proportional to half the peak-to-peak voltage between V_{OUT+} and V_{OUT-}. If this signal is larger than the voltage provided by the Threshold Generator circuitry the $\overline{\text{TTL LINK MON}}$ and $\overline{\text{ECL LINK MON}}$ pins will both be low.

The Threshold Generator level shifts the reference voltage at $V_{TH}ADJ$ through a circuit which has a temperature coefficient matching that of the limiting amplifiers. This improves the accuracy of the Link Monitor over temperature. The relationship between $V_{TH}ADJ$ and V_{TH} (the minimum voltage at the input which will trigger the Link Monitor) is:

ML4621: $V_{TH}ADJ = 600V_{TH} + 0.7$ (9)

ML4622 & ML4623: $V_{TH}ADJ = 375V_{TH}$ (10)

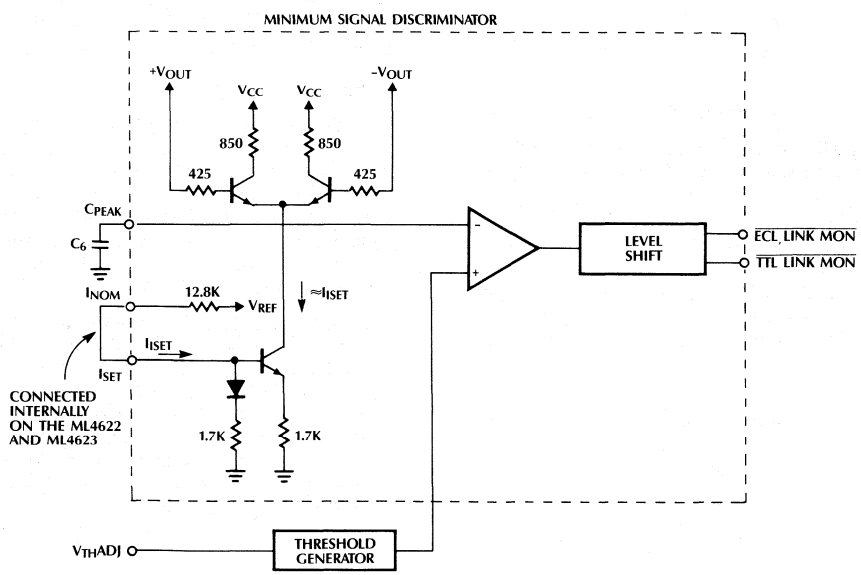


Figure 16.

In these equations V_{TH} is the *peak* value of the input signal. The operating range over which these equations apply is indicated by the graphs in figure 17. The on-chip reference voltage, V_{REF}, can be tied directly to

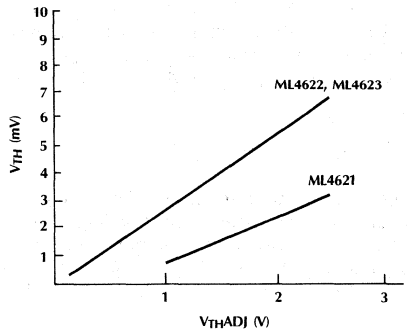


Figure 17.

V_{TH}ADJ to set the threshold level. This 2.5V low impedance source will set the threshold at its maximum allowable level as indicated in the graph. A lower threshold level can be set by dividing down V_{REF} with a resistor string, as in figure 18. On the ML4622 and

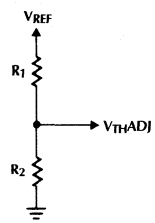


Figure 18.

ML4623, V_{TH}ADJ is a high impedance node so the equation for the resultant V_{TH}ADJ voltage is simply:

$$\text{ML4622 \& ML4623: } V_{TH}ADJ = V_{REF}\frac{R_2}{R_1 + R_2} \quad (11)$$

Figure 19 shows the input circuitry at V_{TH}ADJ on the ML4621. This circuit has a relatively low input impedance of 6.8K and is offset by one diode drop. A

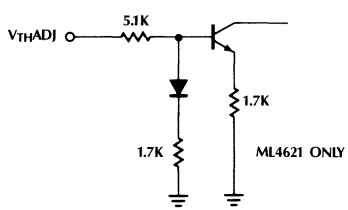


Figure 19.

resistor divider can still be used to drive this point but a different equation, which accounts for the load and offset, must be used:

$$\text{ML4621: } V_{TH}ADJ = \frac{R_2(6800V_{REF} + 0.7R_1)}{6800(R_1 + R_2) + R_1R_2} \quad (12)$$

If, for example, you were using the ML4621 and you wanted the Link Monitor to trigger when the received optical power went below 1μW (–30dBm), you first need to calculate the resultant voltage at V_{IN+} and V_{IN-}. If you were using the HFBR-24X6 Fiberoptic Receiver with a responsivity of 8mV/μW, the peak-to-peak voltage would be:

$$1\mu W \times 8mV/\mu W = 8mV_{P-P} \quad (13)$$

So the Link Monitor should trigger at some point slightly lower than 4mV peak, say 3mV. The reference voltage at V_{TH}ADJ should then be:

$$V_{TH}ADJ = 600(.003) + 0.7 = 2.5V \quad (14)$$

This is a convenient value since the reference voltage supplied by the Quantizer, V_{REF}, is 2.5V. Thus, shorting V_{REF} to V_{TH}ADJ on the ML4621 will set the minimum input signal level at about 3mV. On the other Quantizers this will set the level at about 6.5mV (equivalent to 1.6μW input power).

The Link Monitor has about 0.4mV (peak) hysteresis built-in. V_{TH}ADJ in equations 9 and 10 is the *high* threshold level (the trigger point when the input voltage is rising). The *low* threshold level (the trigger point when the input voltage is falling) is about 0.4mV less than the levels given in these equations. More hysteresis can be induced by connecting a resistor between $\overline{\text{TTL LINK MON}}$ and V_{TH}ADJ creating a positive feedback loop.

A Sample Circuit

The circuit in this section (figure 20) is a point-to-point fiberoptic interface designed to pass 20MBd data over 1 kilometer of 62.5/125μm fiber cable. The main components are the ML4631 LED driver, the HFBR-1414 LED, the HFBR-2416 Receiver, and the ML4621 Quantizer. Choosing –30dBm for the minimum received optical power makes equations 13 and 14 applicable and allows V_{REF} to be used to set the Link Monitor.

Applying figure 5 to the 20MBd data rate yields an optimal bandwidth of about 15MHz. Using equation 6, the value for C_4 and C_5 is derived by setting f_H equal to 15MHz and solving for C. The lower corner frequency, f_L, should be chosen so that, at least, any 60Hz line noise is filtered out. Choosing 0.1μF for C_1 and C_2 will set the lower corner at 200Hz (equation 5). C_3 should be at least 100 times smaller than C_1 and C_2 so .001μF is a good choice.

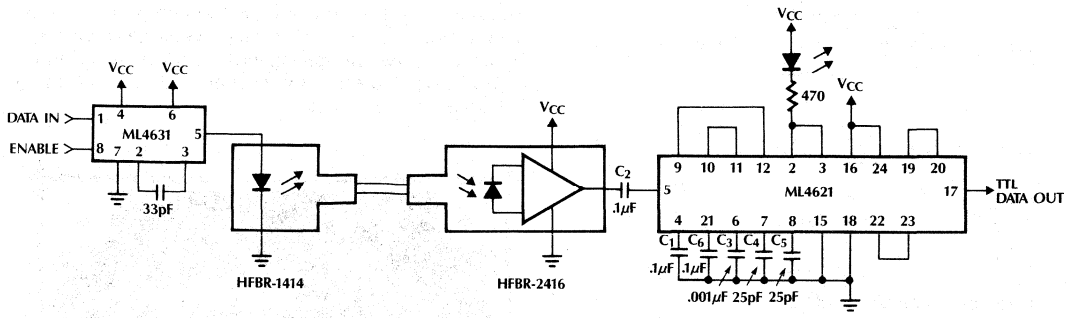


Figure 20.

The only external component left to calculate is C_6. Since the baud rate is 20MBd, the time between peaks in the Link Monitor's peak detector is 50ns. If no more than 0.1% droop is acceptable under the worst case conditions (when the input signal is the smallest), and the internal current source I_{ISET} is used, then C_6 is calculated as follows:

Smallest input signal = 3mV

Gain through amplifiers = 75

Smallest voltage at V_{OUT+} and V_{OUT-} = 3mV × 75 = 225mV

Smallest acceptable droop voltage = 0.1% × 225mV = 225μV

$$\text{Slowest acceptable droop rate} = \frac{225\mu V}{50ns} = 4.5V/\mu s$$

$$\text{Smallest } C_6 = \frac{125\mu A}{4.5V/\mu s} = .028\mu F$$

A 0.1μF capacitor is a convenient acceptable value for this application.

Now that the minimum received power is known, a flux budget can be developed for the interface, and the required optical power from the LED can be derived. Since the output power of the HFBR-1414 is specified out of a short length of fiber attached to the LED unit, no α_{TC} term is required in the flux budget. If no in-line connectors are used and the remaining terms are:

ϕ_R = 1μW
α_O = 10dB/km
L = 1km
α_{CR} = 0.2dB
α_M = 3.0dB

solving the flux budget equation for ϕ_T yields:

$$10 \log \frac{\phi_T}{\phi_R} = \alpha_O L + \alpha_{CR} + \alpha_M \quad (15)$$

$$10 \log \frac{\phi_T}{1\mu W} = 10(1) + 0.2 + 3 = 13.2dB$$

$$\log \phi_T - \log 1\mu W = 1.32$$

$$\log \phi_T + 6 = 1.32$$

$$\log \phi_T = -4.68$$

ϕ_T = 20.9μW (–16.8dBm)

The HFBR-1414 has a minimum Peak Output Optical Power of 31.6μW (–15dBm) when coupled to a 62.5/125μm fiber cable, and when a forward current (I_F) of 60mA is applied. Since the optical output power vs. forward current relationship of the LED is approximately linear, the forward current required to get the minimum output power, 31.6μW, can be calculated as follows:

$$\frac{20.9\mu W}{31.6\mu W} \times 60mA = 40mA \quad (16)$$

The ML4631 is preconfigured to output a minimum of 44mA (60mA typical, 80mA max) so no external components are required in this application. Of course, as mentioned earlier, an external peaking capacitor can be added to improve the rise and fall times.

Now, to make sure there is no chance of saturating the receiver with too much power, a dynamic range calculation is in order. Since there are no in-line connectors and the cable length is fixed, the only dynamic range components are the thermal variations (α_T), the user defined system margin (α_M), the LED output power tolerance (α_{LED}), and the LED drive circuit tolerance (α_{LDC}):

10

$$\alpha_{LDC} = 10 \log \frac{\frac{80}{602}(-12dBm)}{\frac{44}{60}(-12dBm)} = 2.6dB \quad (17)$$

$$\alpha_{LED} = 10 \log \frac{-9dBm}{-16dBm} = 7.0dB \quad (18)$$

α_{LDC}	= 2.6dB
α_{LED}	= 7.0dB
α_M	= 3.0dB
α_T	= 1.0dB
Dynamic Range:	13.6dB

So the maximum input power (ϕ_{TMAX}) the HFBR-2416 Receiver will see is:

$$10 \log \frac{\phi_{TMAX}}{1\mu W} = 13.6dB \quad (19)$$

$$\phi_{TMAX} = 22.9\mu W$$

This is well below the 150μW maximum spec for the HFBR-2416, and the resultant output voltage is

$$22.9\mu W \times 8mV/\mu W = 183.2mV_{P-P} \quad (20)$$

This is well below the 1.4V maximum input voltage of the ML4621.

The Board Layout

It's important to use good layout techniques when creating the PC board for this, or any, high speed circuit. In addition to speed, the receiver in this circuit handles low level signals, making it especially sensitive to noise, ground loops and parasitic feedback paths. All Micro Linear Quantizers employ a fully differential data path which helps reduce the sensitivity to noise in the system. Because this is a high gain circuit, parasitic feedback from the high-level logic-compatible output must be kept to a minimum in order to prevent undesired oscillations. This is accomplished with layouts which physically separate the receiver inputs and outputs. Power supply filtering should be used to ensure the power busses don't provide a feedback path that will degrade the stability of the receiver. Also, a ground plane is strongly recommended to minimize the inductance of the supply return paths.

The effect of the ground plane is maximized by locating it on the same side as the components, and maintaining a ground path between all adjacent pins. Figure 21 shows the foil pattern used on an ML4621 demo board. Note the full ground plan and the paths between pins on the IC.

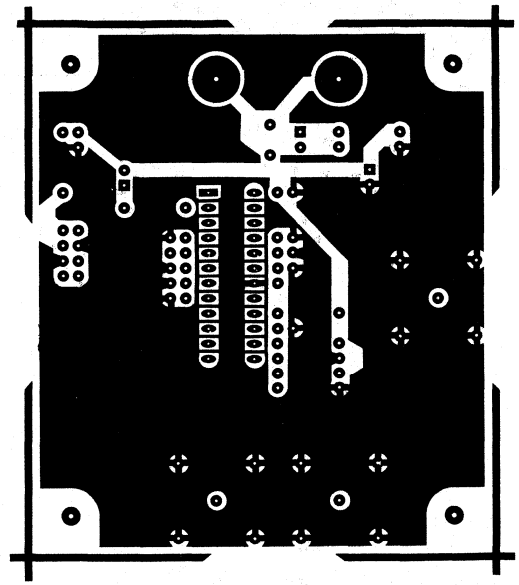


Figure 21.

The importance of good construction and layout techniques cannot be over-stressed. Layout designs that result in excessive parasitic inductance and capacitance will degrade the stability and bandwidth of the receiver. Although the receiver is generally considered to be the most critical portion of the fiberoptic link electronics, careful attention should also be paid to the transmitter. Several traces in this circuit will pass large currents at high speeds. In order to minimize the effect of trace inductance, these lines should be kept as short as possible.

When good layout practices are employed, a 100MBd fiberoptic interface can be constructed using the components described here.

Micro Linear

Application Note 7

Expanding the ML2200 Input Multiplexer

Harlan Ohara & Vince Cardinale

1.0 Introduction

If the four channel differential input multiplexer on the ML2200 is insufficient for your application, it can be expanded using one of three methods described in this document. An expanded input multiplexer will greatly enhance the processing power of the ML2200 but will restrict some of its flexibility. The limitations of each circuit are discussed at the end of this application note.

The first circuit controls up to 64 differential inputs but restricts the ML2200 to always run eight operations. The second circuit controls up to 128 single ended inputs and again restricts the ML2200 to always run eight operations. The third circuit is limited to eight differential inputs but is fully programmable in the number of operations. Each circuit is fully synchronized with the ML2200 and can be built with off-the-shelf components.

Although this application note discusses only the ML2200, the ML2208 can be used as well. Only minor operational issues within the ML2208 are affected.

2.0 General Theory of Operation

An external counter (74LS163) is used to control the additional multiplexer devices (DG506 or DG507). The counter is incremented by the SYNC pin of the ML2200, which must be programmed as an output. The SYNC pin is suitable for this purpose since it always signifies the start of a new operation.

Synchronization with the ML2200 is achieved by utilizing the DBR pin to load input channel #1 into the counter. Since the DBR signal comes out after the sequence of operations are complete and the next sequence is started, it is too late to correctly synchronize the counter prior to the beginning of the next sequence. Synchronizing on the "1" count, however, will always reset the counter to the proper value if synchronization is ever lost.

Due to the above described behavior, a "boundry" problem exists in the very first sequence of operations *and* the first operation of the second sequence after the chip is started. In order to get out of this problem, the RUN bit of the control register is decoded and duplicated in these circuits. The RESET signal is also brought in. These signals force the counter to predetermined states and relieves the "boundry" problem.

3.0 A 64-Channel Differential Input Circuit

This circuit, shown in figure 1, provides up to 64 additional input channels. Two 74LS163 counters, U5 and U6, are used to develop the address for each channel. Only 6 of the 8 available counter bits are needed to control the channel selection. The 3 LSBs are used to drive the multiplexer (DG507) address bus and the 3 MSBs are decoded and used to drive each multiplexer's enable pin. A 74LS138 (U7) is used to decode the MSBs, providing control for 8 multiplexer chips. The 2 unused counter bits could be used to address additional multiplexers, providing control for up to 256 channels.

A D-type flip-flop (U4A, 74LS74) is used to reset both counters whenever the ML2200 is reset or not in RUN mode. This is accomplished by presenting an active low signal at the synchronous clear inputs of the counters whenever either the RESET or HALT condition exists. When the ML2200 is placed in RUN mode, the first SYNC pulse resets the counters to zero instead of incrementing them. At the same time, the first SYNC pulse clears the resetting condition by clearing the flip-flop.

The other flip-flop in this circuit, U4B, is used to trap the 0 to 1 transition of the DBR signal. This transition causes the output of U4B to go low, which sets up the counters for a load cycle. The next SYNC pulse (which should correspond to the first operation of the ML2200) will then load the counter with a "1", forcing the counters to be synchronized to the sequence. As before, the same pulse that performs the load operation also clears the load operation.

U1 (74LS138) and U2 (74LS379) form the logic that decodes the RUN bit from the microprocessor bus to develop one of the conditions that resets the counters. U1 simply decodes the address of the control register within the ML2200 and U2 latches the status of the RUN bit.

This circuit requires operations to be done in groups of eight and each operation within the group must have the same characteristics.

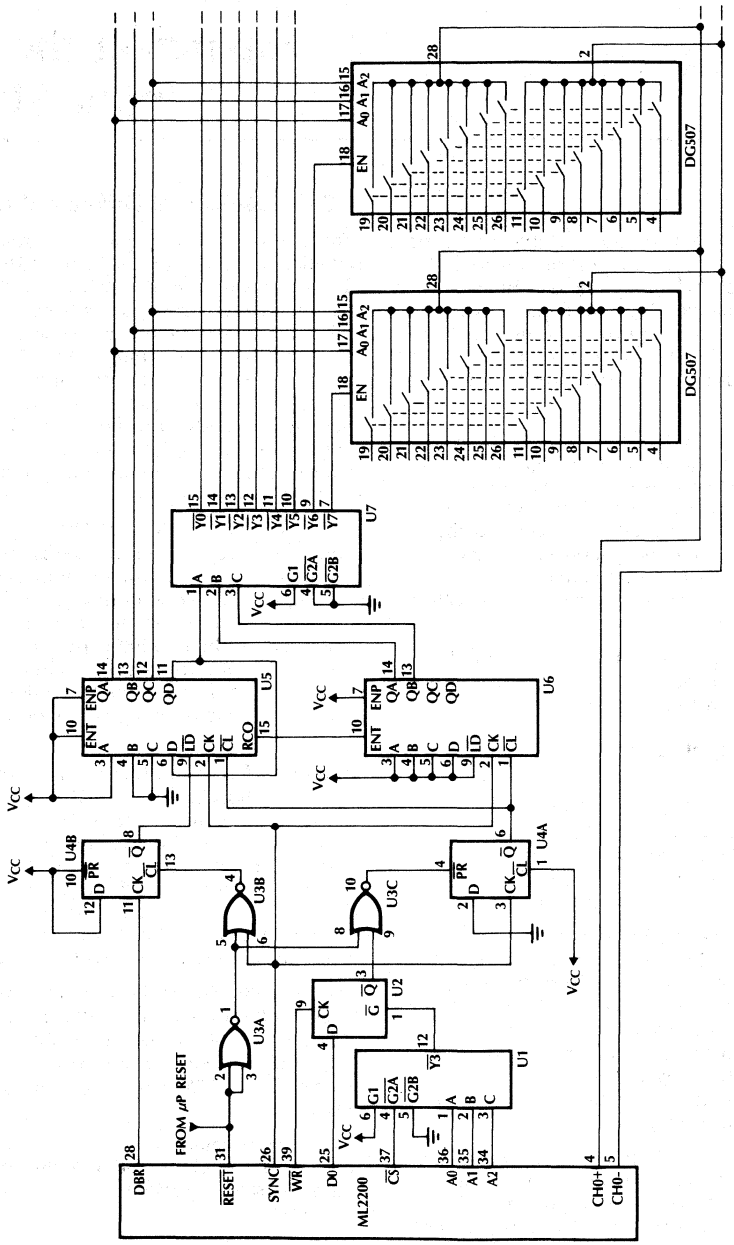

DG507
DG507
U7
U5
U6
U4B
U4A
U3B
U3C
U3A
U2
U1
VCC
FROM μP RESET
ML2200
DBR
RESET
SYNC
WR
D0
CS
A0
A1
A2
CH0+
CH0-

Figure 1.

4.0 A 128-Channel Single Ended Input Circuit

This circuit, shown in figure 2, is identical to the differential circuit with three exceptions:

1. Four address bits are used to drive each multiplexer, since each multiplexer chip now contains 16 channels instead of 8.
2. The decoder chip (U7) is shifted one bit up on the counter output. This makes room for the extra bit needed for multiplexer addressing.
3. DG506 multiplexers are used because this is a single ended application.

This circuit requires operations to be done in groups of eight and each operation within the group must have the same characteristics.

5.0 An 8-Channel Diferrential Input Circuit

This circuit, shown in figure 3, is very similar to the two previous circuits. It still uses two D-type flip-flops to load and reset the counters. The difference here is that register U7 (74LS379) is provided at address location 6 within the 8 byte ML2200 address space and is used to store a count equal to the number of operations programmed by the microprocessor in the ML2200.

Address location 6 and 7 are spare locations within the ML2200 address space. A 74LS85 (U8) four bit comparator is used to reset the counter to zero when the maximum count is reached. A single DG507 provides the eight input channels.

This circuit is not restricted to performing operations in groups of eight. Each channel can be programmed and initiated individually. This flexibility is maintained at the expense of limiting the number of differential inputs to eight.

6.0 Circuit Limitations

In order to maintain synchronization with the ML2200, these circuits contain several inherent limitations which are described below:

1. The SYNC pin is limited to use as an output.
2. These designs allow less settling time for external input circuits, such as instrumentation amplifiers, than otherwise would be possible.
3. The capability to do random reference selection is lost.
4. The capability to do random input channel selection is lost. Input channels must be scanned sequentially.

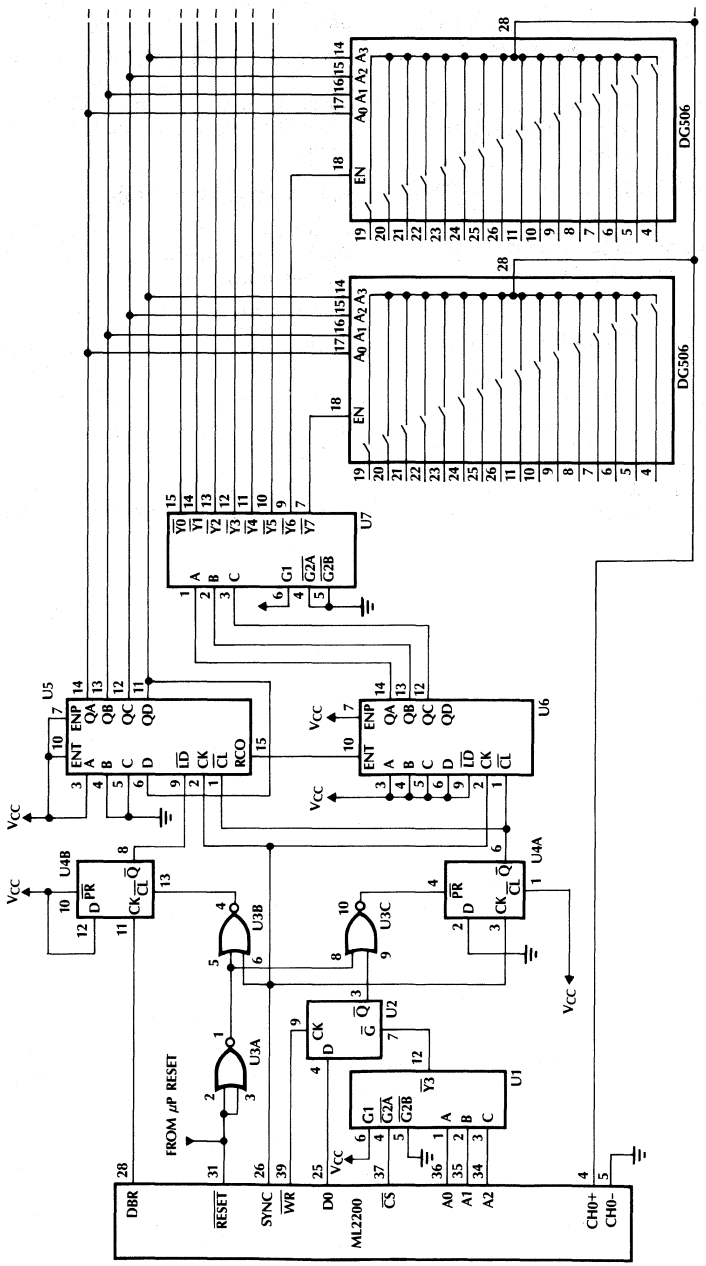

DG506
DG506
U7
U5
U6
U4B
U4A
U3B
U3C
U3A
U2
U1
VCC
FROM μP RESET
ML2200
DBR
RESET
SYNC
WR
D0
CS
A0
A1
A2
CH0+
CH0–

Figure 2.

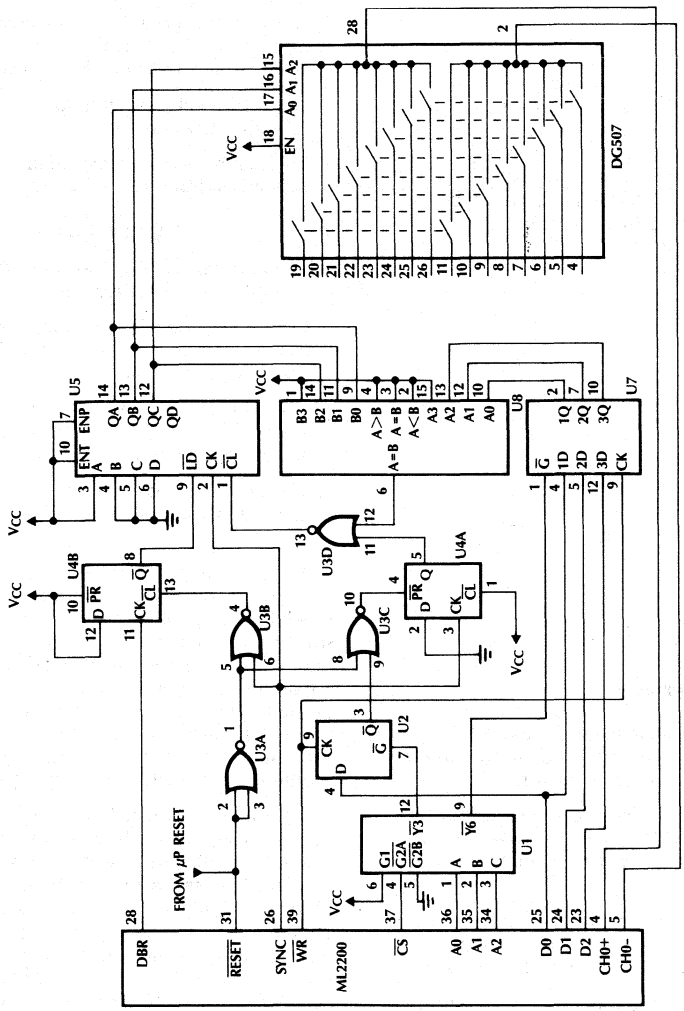

DG507
U5
U7
U8
U4A
U4B
U3A
U3B
U3C
U3D
U2
U1
VCC
FROM μP RESET
ML2200
DBR
RESET
SYNC
WR
CS
A0
A1
A2
D0
D1
D2
CH0+
CH0-

Figure 3.

Micro Linear

Application Note 8

Harlan Ohara

One Pin Crystal Oscillators

1.0 Introduction

Micro Linear has frequently used a one pin oscillator design in its CMOS chips. The concept of a one pin oscillator may seem peculiar to some at first, but the design topology has been around for many years, dating back to vacuum tube days. This topology is shown in Figure 1 and is commonly known as the Colpitts oscillator. The only difference compared to previous implementations is that an MOS transistor is used as the active element.

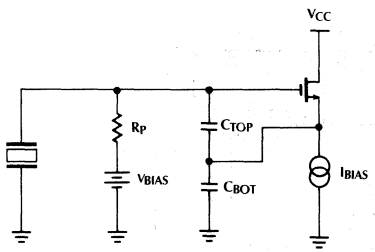


Figure 1.

There are two important advantages to using this particular topology versus the more common two pin design (which is called a Pierce oscillator):

1. Only one pin is required, leaving the extra pin for maximum functionality. This is increasingly important as chips become more complex in function.
2. No external components are usually required except for the crystal. If extremely high frequency accuracy is required, then an external capacitor in parallel with the crystal can be used to trim the frequency.

All is not free, however, there are some disadvantages:

1. This design is less tolerant of external parasitics to ground than the two pin design. This is not usually a problem since the designs used in Micro Linear's circuits have been provided with sufficient margin to handle typical printed circuit board parasitics.
2. Flexibility in terms of user adjustment of design parameters is less in this design. Again, this is not seen to be a problem for two reasons:
   a) Board level designers rarely adjust the two pin design parameters.
   b) Enough margin is provided so that adjustment is not needed.

2.0 Theory of Operation

Exact circuit analysis of the oscillator is a complex procedure for several reasons:

1. In a practical design situation, the system equations are a minimum of 5th order. Exact hand calculations are difficult at best.
2. Final oscillation conditions are not only based on small signal analysis, but very dependent on large signal non-linear situations.
3. The crystal model is generally a simple case in small signal analysis but element parameters can change with excitation level.

In this section, no attempt is made to provide a complete exact analysis. An alternate approach is taken in which hand calculations can closely approximate the small signal solution. This approach is also much more heuristically satisfying in that effects of design parameter changes can be seen without applying a lot of math. This also serves to provide the user with a way to calculate an approximate frequency of oscillation if more exact frequency tolerances are required other than just plugging the crystal in.

For the more technically inclined, an exact small signal sample design procedure is presented in Appendix A using the MathCAD™ program on an IBM-compatible PC. This is possible due to the presence of a root solver capability in MathCAD. Users of HP calculators or numerical analysis computer programs can also perform this analysis. Appendix B contains an example procedure to estimate final oscillation amplitude while Appendix C goes through the procedure to calculate the closed loop root locus plot which is then used to estimate oscillator startup time.

2.1 Crystal Model

The typical crystal model is shown below:

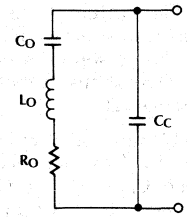


Figure 2.

Typical values for the 12.352 megahertz crystal used in some of Micro Linear's telecom chips are:

$L_O := 8.005814 \cdot 10^{-3}$ henries
$C_C := 5.10 \cdot 10^{-12}$ farad
$C_O := 20.7558 \cdot 10^{-15}$ farad
$R_O := 15$ ohms

The admittance of the crystal is:

$$Y_{XTL}(s) := C_C \cdot s + \frac{1}{L_O \cdot s + \frac{1}{C_O \cdot s} + R_O}$$

Plot 50 points versus frequency:

$x := 1 \ldots 50$

Define radian frequency values:

$\omega_x := 12.346 \cdot 10^6 \cdot 2 \cdot \pi + x \cdot 120$

Plot real (resistive) part:

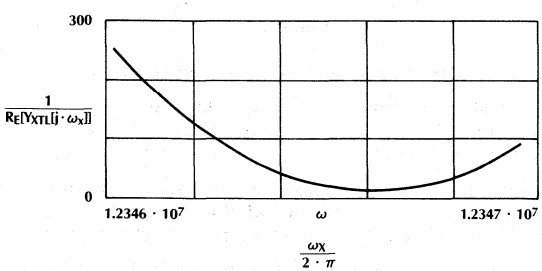


Figure 3.

Plot susceptance:

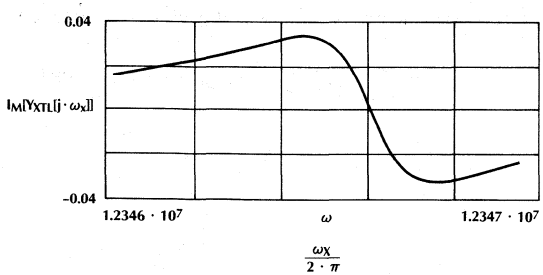


Figure 4.

Note that at the series resonance frequency of:

$$\frac{1}{2 \cdot \pi \cdot \sqrt{L_O \cdot C_O}} = 1.2346608 \cdot 10^7 \text{Hz}$$

the susceptance is zero and the resistance is: $R_O = 15$.

Oscillators that operate the crystal in the series mode use this characteristic as part of a feedback loop in which the loop gain is maximum at this frequency. Above this frequency the susceptance is inductive. Oscillators such as this one-pin design (and the two-pin Pierce) operate the crystal in the parallel mode, "using it as an inductor."

2.2 Simplified Hand Calculation of Loop Gain:

In this section, a simplified (but approximate) method of calculating the loop gain is shown. This method also demonstrates in a more heuristic way how loading affects the oscillator and how one may choose the crystal characteristics, especially the series resistance R_O. The calculation for the approximate frequency of oscillation is also shown. This calculation is quite accurate.

Before we proceed with the calculations. two general principles will be presented that are used to make the calculations. Derivations of these principles can be found in reference [1]:

1. In Figure 5, it is seen that an RLC circuit with series loss can be represented by a circuit with parallel loss (resistance). This applies when the circuit Q is high (>10).

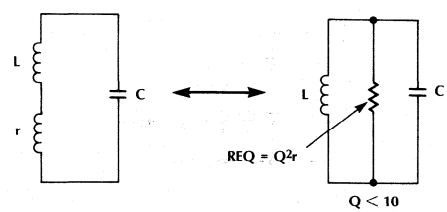


Figure 5.

2. In Figure 6, an RLC circuit with series capacitors can be classified as a "parallel resonant transformer" circuit. Again, this is accurate only when the Q is high (this is easily satisfied with crystal circuits, with Q's in the ten to hundreds of thousands). In this case, the two capacitors act like a transformer with a turns ratio of:

$$n := \frac{C_1}{C_1 + C_2}$$

Hence any resistance can be reflected by the square of the turns ratio.

10

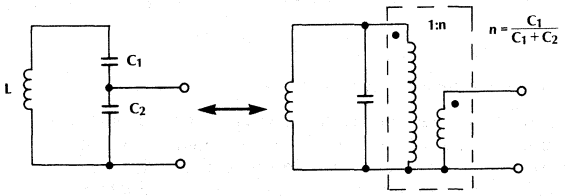


Figure 6.

Using principle 1) from above, we can construct a crystal model which has a parallel loss element:

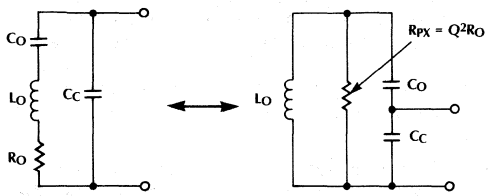


Figure 7.

Using principle 2) from above, we can now reflect the loss element to the crystal terminals by the "turns ratio."

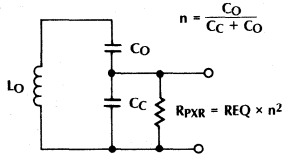


Figure 8.

At this point, we should develop the small signal equivalent of the oscillator circuit:

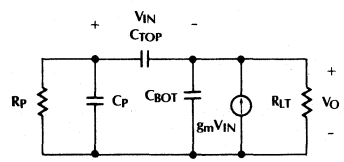


Figure 9.

In Figure 9 the MOS transistor has now been replaced by its small signal equivalent circuit. In this instance, g_m is the small signal transconductance of the transistor and is set by the DC bias current. R_{LT} is the parallel combination of the drain to source conductance and the "body bias factor" (if the source is not at the same potential as the bulk). Derivations of these parameters can be found in reference [2].

C_P is the parallel combination of all circuit reactive parasitics found at the oscillator pin, including the crystal case capacitance, C_C. C_{TOP} and C_{BOT} are on-chip capacitors with sizes chosen for a particular design range.

R_P is the resistance of an on-chip DC bias resistor for the gate of the MOS device *plus* any dissipative loss present at the oscillator pin to ground. This is any lossy effects due to circuit board or socket dissipation factors at the frequency of oscillation.

We now connect the crystal to the oscillator circuit. Note that the reflection and transformer calculations above must be done with all circuit capacitances taken into account:

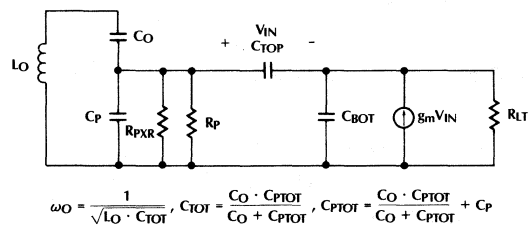


Figure 10.

Let us assign some typical values to the components:

$R_{LT} := 80 \cdot 10^3$ ohms $g_m := 1.6 \cdot 10^{-3}$ Amps/Volt
$C_P := 10 \cdot 10^{-12}$ farad $C_{TOP} := 16 \cdot 10^{-12}$ farad
$R_P := 100 \cdot 10^3$ ohms $C_{BOT} := 16 \cdot 10^{-12}$ farad

We will use the crystal values defined above with the exception that C_C is now included in C_P, which represents all capacitive parasitics present at the pin.

The total capacitance present at the pin including C_{TOP} and C_{BOT} is:

$$C_{PTOT} := \frac{C_{TOP} \cdot C_{BOT}}{C_{TOP} + C_{BOT}} + C_P \qquad C_{PTOT} = 1.8 \cdot 10^{-11}$$

The total capacitance seen across the crystal inductance is:

$$C_{TOT} := \frac{C_O \cdot C_{PTOT}}{C_O + C_{PTOT}} \qquad C_{TOT} = 2.073 \cdot 10^{-14}$$

This capacitance in parallel with the crystal inductance just so happens to produce a resonant frequency which is very close to the frequency of oscillation:

$$\omega_O := \frac{1}{\sqrt{L_O \cdot C_{TOT}}} \qquad \omega_O = 7.762 \cdot 10^7$$

$$\frac{\omega_O}{2 \cdot \pi} = 1.2353724 \cdot 10^7$$

Note that this frequency is .014% higher than the specified 12.352 Megahertz. This is because this crystal was ground with a specified capacitive load of 18pF across its terminals. In our case, we only have about 13pF.

The circuit Q is now calculated:

$$Q := \frac{1}{\omega_O \cdot R_O \cdot C_{TOT}} \qquad Q = 4.143 \cdot 10^4$$

The equivalent parallel resistance across the crystal inductance is now calculated using principle 1) above:

$$R_{PX} := Q^2 \cdot R_O \qquad R_{PX} = 2.574 \cdot 10^{10}$$

This is now reflected to the oscillator pin using principle 2) above:

$$R_{PXR} := R_{PX} \cdot \left[\frac{C_O}{C_O + C_{PTOT}}\right]^2 \qquad R_{PXR} = 3.415 \cdot 10^4$$

This is now combined with the parallel resistance present at the oscillator pin:

$$R_{PTOT} := \frac{R_{PXR} \cdot R_P}{R_{PXR} + R_P} \qquad R_{PTOT} = 2.546 \cdot 10^4$$

Note that this can be reflected again through the "capacitive transformer" of C_{TOP} and C_{BOT}:

$$R_{PTOTR} := R_{PTOT} \cdot \left[\frac{C_{TOP}}{C_{TOP} + C_{BOT}}\right]^2$$

$$R_{PTOTR} = 6.364 \cdot 10^3$$

We now combine this with the resistance present at the transistor source:

$$R_L := \frac{R_{LT} \cdot R_{PTOTR}}{R_{LT} + R_{PTOTR}} \qquad R_L = 5.895 \cdot 10^3$$

This is the load resistance. This multiplied by the transconductance will give us our gain up to the source of the transistor from the input.

$$g_m R_L = 9.433$$

Note that the input to our circuit is the voltage applied across the gate to source of the MOS transistor, or in other words, the voltage across C_{TOP}. Using the "capacitive transformer principle" we can determine that the loop gain is:

$$A_L := \frac{C_{BOT}}{C_{TOP}} \cdot g_m \cdot R_L \qquad A_L = 9.433$$

This gives us our loop gain, which hopefully is more than 1 to allow oscillations. Note that this compares favorably with the exact analysis given in Appendix A of 9.41.

This is a good time to pause and reflect on what the above analysis tells us:

1. It is seen that the oscillation frequency depends on the total capacitance at the oscillator pin in series with the crystal capacitor C_O. Since C_O is very small (typically 10's of femto-farads) external capacitance has a small effect on the oscillation frequency. This provides a means of "tweaking" the frequency to an exact value with a trimmer capacitor placed from the oscillator pin to ground.
2. Using the "capacitive transformer" principle, it is seen that large values of capaitance at the oscillator pin reduces the loop gain since the crystal resistance is now reflected into a smaller value and hence the product $g_m \cdot R_l$ is smaller. Oscilloscope probes can contribute a significant amount of parasitic and should be used carefully when debugging this circuit. If frequency trimming is employed by placing a parallel adjustment capacitor to ground, it must be done carefully so that the loop gain is not made too small.
3. Lossy components at the oscillator pin also reduces the product $g_m \cdot R_L$. This is especially important at higher crystal frequencies, where printed circuit board material or socket material becomes more and more lossy. The value of the on-chip bias resistor varies with frequency from about 1MΩ to about 100kΩ (over a 1 to 20 MHz range). Note that this is a fairly high impedance which is easily affected by external parasitics. Oscilloscope probes can be particularly lossy at these frequencies.

2.3 Three More Important Criteria for Consideration:

Three more important items need to be covered. These items may or may not be OK even if the loop gain calculation is adequate (more than 1):

1. Oscillator phase margin.
2. Nyquist criterion.
3. Final oscillation amplitude

The theory for the above criteria is too lengthy to cover in an application note; only a brief qualitative explanation will be given. The reader is encouraged to consult references [3], [4], and [5]. The exact analysis given in Appendix A will cover the phase margin and Nyquist criterion.

Oscillator Phase Margin:

Figures 11A through 11D in Appendix A show the open loop transfer characteristics of the oscillator. 11A shows the overall magnitude over a wide range of frequencies.

The crystal characteristic is not visible since it occurs over a very narrow range. 11B shows the phase characteristic.

These curves show that the circuit produces a single pole rolloff of 6dB per decade and a final phase shift of 90 degress. Examining the circuit in Figure 10, we see that the loop transfer function starts out at 180 degrees out of phase. This is because the output is developed across C_{BOT} and the input is taken across C_{TOP}. At DC, the voltage across C_{TOP} is of opposite phase to that of C_{BOT}, since the top side of C_{TOP} has a DC path to ground. The single pole rolloff is primarily due to (but not exactly) the combination of R_{LT} and the total capacitance seen at the source of the MOS transistor to ground. The crystal inductance combined with the circuit capacitances can almost provide another 180 degrees of phase shift. This, combined with the 180 degrees from the active element will provide ALMOST, but not quite the 360 degrees needed for oscillation. This is where the single pole rolloff comes in. Examining 11C shows that the loop gain peaks first then dips. This is due to primarily a complex pole pair and a complex zero pair. The peak is a result of the crystal resonating with all circuit capacitances:

$$\omega_P := \frac{1}{\sqrt{L_O \cdot C_{TOT}}} \qquad \omega_P = 7.7620737 \cdot 10^7$$

The complex zero pair comes about when the crystal resonates with all capacitances except for the C_{TOP} and C_{BOT} combination:

$$\omega_Z := \sqrt{\frac{1}{L_O \cdot \left[\frac{C_P \cdot C_O}{C_P + C_O}\right]}} \qquad \omega_Z = 7.7656489 \cdot 10^7$$

The phase shift at the complex pole pair passes through zero and the amplitude peaks to provide the oscillation point. The phase then goes past the point needed for oscillation and then passes through zero again at the complex zero location, returning to the 90 degree point where it started. The amount that the phase shift passes the point necessary for oscillation is called the phase margin. This depends on:

1. The proximity of the complex zero and pole pair, which is determined by the difference in value of the C_{TOP} and C_{BOT} combination relative to the external circuit capacitances. Large parasitics decrease the distance between the pole and zero pair, degrading the phase margin.
2. The circuit "Q," which is a function of the reflected crystal resistances. Applying the reflection algorithm described above shows that large capacitive parasitic values produce a lower "reflected" crystal resistance and thus a lower "Q." Additionally low values of parasitic loss resistances present at the oscillator pin will have the same effect.

If both of the above situations exist, the phase may not cross the zero point at all and oscillations will not start. The exact analysis procedure in Appendix A gives a quantitative description of this situation.

Nyquist Criterion:

In Figures 11C and 11D in Appendix A, note that the loop gain falls to below unity at the complex zero point. A situation can exist where perhaps, if g_M is large, the loop gain will remain above unity, even at the complex zero frequency. This represents a violation of the Nyquist criterion for oscillation in that the Nyquist plot never encircles the –1,0 point. This can happen with crystals at the lower frequencies around 1MHz or so. Appendix A gives a quantitative analysis of this situation, and reference [5] goes in detail for the theory.

Final Oscillation Amplitude:

This section outlines a qualitative explanation of the final oscillation amplitude. For a complete analysis, refer to references [1] and [4]. Appendix B gives an example analysis using the numerical methods of the MathCAD software on an IBM PC. If the user is interested at a higher level, please contact Micro Linear for design parameters.

Given the loop gain at the frequency where the phase shift crosses zero, oscillations start and then increase in amplitude. The waveforms across C_{TOP} and C_{BOT} in Figure 10 are close to sinusoidal due to the high Q of the circuit. The drain current of the MOS transistor, however, is a square law version of the gate to source voltage. Thus, at large signals, the effective g_M of the transistor is reduced by a factor which is related to only the first harmonic of the drain current. This is the only component which is fed back around the loop due to the high Q. For a given small signal loop gain, the amount of oscillation amplitude necessary to maintain the large signal loop gain at one will determine the final oscillation amplitude. For a typical Micro Linear design, this usually falls within the power supplies. Occasionally, then the loop gain is high, the amplitude may exceed the power supplies but is "clamped" by the input static protection diodes present on the oscillator pin. This forward biases the substrate, but the input protection structure of the oscillator pin prevents any harmful effects from this phenomenon.

3.0 Design Parameters

The following section outlines some parameters necessary to perform the hand calculation analysis described above and the exact analysis in Appendix A for various Micro Linear chips at the time of this application note:

ML2200, ML2208, ML2230, ML2233, ML2221:
These designs are restricted to 3–7MHz only; no frequency trim. Provide minimum parasitic from pin to ground possible.

C_{TOP}: 10pF
C_{BOT}: 12pF
Typical g_m: 500μA/V
Typical R_{LT}: 8kΩ
R_P at 3MHz: 240kΩ (see Appendix D)
R_P at 7MHz: 140kΩ

ML2031, ML2032:
These designs are restricted to 3–15MHz only; frequency trimming with capacitor allowed if desired.

C_{TOP}: 16pF
C_{BOT}: 16pF
Typical g_m: 1.6mA/V
Typical R_{LT}: 80kΩ
R_P at 3MHz: 220kΩ (see Appendix D)
R_P at 15MHz: 100kΩ

ML2035, ML2036:
These designs are restricted to 2–18MHz only; frequency trimming with capacitor allowed if desired.

C_{TOP}: 18pF
C_{BOT}: 18pF
Typical g_m: 1.6mA/V
Typical R_{LT}: 80kΩ
R_P at 2MHz: 290kΩ (see Appendix D)
R_P at 15MHz: 100kΩ

In addition, the package pin capacitance is needed along with any stray capacitance due to the bond wire, etc. These values vary from device to device, but an approximate value would be about 1–3pF.

4.0 Crystal Specifications

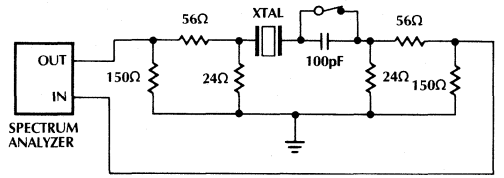
For most situations, standard microprocessor type crystals will work fine in these circuits. If more precise frequency tolerance or unusual frequencies are desired, a special grind will have to be orderd from a crystal manufacturer.

1. Calculate what capacitance will be seen by the crystal in your board, then specify this to the crystal manufacturer.
2. An approximation of the series resistance tolerable can be made using the above analysis or the exact analysis in Appendix A. One fact which is rarely known is that crystal resistances on startup can be much higher than when the crystal is being excited. Specify both a low level maximum series resistance and an operating level series resistance (e.g., 10nW to 1μW startup level and 1μW to 200μW operating level). An equation to calculate crystal dissipation is given in Appendix A.
3. Frequency tolerances of about .005% are common, tighter tolerances are available.
4. Frequency stability over temperature (0–70°C) of about .005% are common; special order for extended temperature range or tighter tolerance.
5. Frequency stability is typically dominated by the crystal itself. Temperature coefficients of the parasitic capacitances come into play and can be calculated using the equations described above. Variation of the oscillator g_m and internal capacitance values versus temperature has a very minor role in stability (1–5ppm or so over 0–70°C).

5.0 Board Level Design Verification

Some simple tests can be performed during the debugging process to verify that the crystal being used and the parasitics present are acceptable for manufacture:

1. Measure the crystal parameters. A procedure to do this is described below. This is a procedure described in reference [6].



1. MEASURE PEAK AMPLITUDE AND FREQUENCY: PEAK AMPLITUDE GIVES R_O VALUE.
2. OPEN SWITCH, MEASURE PEAK FREQUENCY (THIS SHIFTS UP) $\Delta f = \frac{1}{8\pi^2 f_S C_T L_O}$ $C_T = 100pF + C_C$ (CASE CAPACITANCE) SOLVE FOR L_O.
3. $f_S = \frac{1}{2\pi\sqrt{L_O C_O}}$, SOLVE FOR C_O

2. Observe crystal startup at the high temperature/low power supply specification of your system. Crystal startup is the most stringent test of the design. Often times the series resistance of the crystal at low levels is many times that at operation. Do this over a wide sample range of the intended crystal to be used.

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3. Be sure that the oscillator amplitude is at least 2 volts peak to peak at the high temperature/low supply case. This is to insure that the buffer that squares the sine wave up remains operational. If less than 2 volts, consider using a crystal with a lower series resistance or decrease parasitic capacitance on the oscillator pin. Do not use long lead lengths or traces from the oscillator pin to the crystal.
4. Observe crystal startup times. This is a good indication of available loop gain. Crystal startup time is a function of the real part of the closed loop transfer function. Appendix C provides a sample of how to calculate a root locus plot versus varying g_m's.
5. When observing the oscillator pin, use a FET probe or use a standard probe in series with a 1pF capacitor to prevent loading the pin with excessive parasitic. When observing frequency stability, use a spectrum analyzer with an antenna wire pickup to minimize parasitic effects. Alternately, if a buffered output of the oscillator is available, measure the frequency at this point.

6.0 References

[1] Clarke-Hess, "Communications Circuits: Analysis and Design," Addison-Wesley Publishing Company, 1971.

[2] P.R. Gray and R.G. Meyer, "Analysis and Design of Analog Integrated Circuits," Second Edition, John Wiley and Sons, 1984.

[3] J.T. Santos and R.G. Meyer, "A One Pin Crystal Oscillator for VLSI Circuits," *IEEE Journal of Solid State Circuits*, Vol SC-19 No. 2, April 1984.

[4] R.G. Meyer and D.C.F. Soo, "MOS Crystal Oscillator Design," *IEEE Journal of Solid State Circuits*, Vol SC-15, No. 2, April 1980.

[5] M.A. Unkrich and R.G. Meyer, "Conditions for Start-Up in Crystal Oscillators,"*IEEE Journal of Solid State Circuits*, Vol SC-17, No. 1, February, 1982.

[6] N.J. Watson, "Crystal Testing Using Spectrum Analyser TF 2370," Application Note No. 14, Marconi Instruments.

APPENDIX A

ONE PIN OSCILLATOR DESIGN

This document is an exact small signal analysis of the one pin oscillator using the MathCAD software package.

******define units first:

$rad \equiv 1$ $\quad deg \equiv \pi \cdot \frac{rad}{180}$ $\quad TOL \equiv 10^{-6}$ sets MathCAD tolerance

******Define Parameters:

$Ctop \equiv 16 \cdot 10^{-12}$ $\quad Cbot \equiv 16 \cdot 10^{-12}$ $\quad Cc \equiv 5 \cdot 10^{-12}$ (xtal case cap)

$Ro \equiv 15$ $\quad Lo \equiv 8.005813989 \cdot 10^{-3}$ $\quad Co \equiv 20.7558457 \cdot 10^{-15}$

****Serial Resonant Frequency $\omega s := \frac{1}{\sqrt{Lo \cdot Co}}$ $\quad \frac{\omega s}{2 \cdot \pi} = 1.2346594 \cdot 10^{7}$

****Crystal Q: $Qxtal := \frac{1}{\omega s \cdot Ro \cdot Co}$ $\quad Qxtal = 4.14 \cdot 10^{4}$

****CAPACITOR DIVIDER:

****Equivalent C of Capacitor Divider: $Ceq := Ctop \cdot \frac{Cbot}{Ctop + Cbot}$

$Ceq = 8 \cdot 10^{-12}$

****Transformer Ratio for Capacitive Divider: $n := \frac{Ctop}{Ctop + Cbot}$

$n = 0.5$

****Impedance Reflection Ratio for Capacitive Divider:

$zc := n^{2}$ $\quad zc = 0.25$

****Transistor Characteristics:

$gm := 1.6 \cdot 10^{-3}$ $\quad Rlt := 80 \cdot 10^{3}$

****Pin Characteristics:

**External pin parasitics--this is the real and imaginary parts of any external parasitic at the oscillation frequency):

$Rext := 100 \cdot 10^{3}$ $\quad Cext := 5 \cdot 10^{-12}$

****Total Parallel Capacitance:

$Cptot := Cc + Cext + Ceq$

$Cptot = 1.8 \cdot 10^{-11}$ $\quad Cpt := Cptot - Ceq$

$Cpt = 1 \cdot 10^{-11}$

****Equivalent Capacitance for Pole Pair:

$Cpol := Co \cdot \frac{Cptot}{Co + Cptot}$ $\quad Cpol = 2.073 \cdot 10^{-14}$

****Approximate Frequency of Oscillation:

$Wpol := \frac{1}{\sqrt{Lo \cdot Cpol}}$ $\quad Fpol := \frac{Wpol}{2 \cdot \pi}$ $\quad Fpol = 1.235371 \cdot 10^{7}$

****Ratio of the Capacitive Divider Between Crystal and Oscillator:

$nx := \frac{Co}{Co + Cptot}$ $\quad nx = 0.001$

****Impedance Reflection Ratio:

$zx := nx^{2}$ $\quad zx = 1.327 \cdot 10^{-6}$

****Q with Cload: $Q := \frac{Wpol \cdot Lo}{Ro}$ $\quad Q = 4.143 \cdot 10^{4}$

****Equivalent Parallel R for Crystal Only:

$Rpx := Q^{2} \cdot Ro$ $\quad Rpx = 2.574 \cdot 10^{10}$

****Reflected Value of the Crystal Resistance at the Oscillator:

$Rxtal := Rpx \cdot zx$ $\quad Rxtal = 3.415 \cdot 10^{4}$

Total parallel resistance at the oscillator pin:

$Gsum := \frac{1}{Rext} + \frac{1}{Rxtal}$ $\quad Rsum := \frac{1}{Gsum}$ $\quad Rsum = 2.546 \cdot 10^{4}$

****Reflected Parallel R at Oscillator to Transistor Source:

$Rref := Rsum \cdot zc$ $\quad Rref = 6.364 \cdot 10^{3}$

****Total Load Seen at Transistor Source:

$Rl := Rref \cdot \frac{Rlt}{Rref + Rlt}$ $\quad Rl = 5.895 \cdot 10^{3}$

****Loop Gain Calculated with Reflection Method:

$Al := gm \cdot Rl \cdot \frac{Cbot}{Ctop}$ $\quad Al = 9.433$

**in dB: $\quad 20 \cdot \log(Al) = 19.493$

**********EXACT CALCULATIONS:**********

**Polynomial Coefficients for Zeros:

$n0 := 1$

$n1 := (Co \cdot Ro + Co \cdot Rext + Cpt \cdot Rext)$

$n2 := (Co \cdot Lo + Co \cdot Cpt \cdot Ro \cdot Rext)$

$n3 := (Co \cdot Cpt \cdot Lo \cdot Rext)$

guess first zero location:

$\omega := \frac{-1}{Rext \cdot (Cpt + Co)}$ $\quad \omega = -9.9792871 \cdot 10^{5}$

$s := \omega$

$z1 := root\left[n3 \cdot s^{3} + n2 \cdot s^{2} + n1 \cdot s + n0, s\right]$

$z1 = -9.9792906 \cdot 10^{5}$

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guess complex zero pair location:

$$\omega := \sqrt{\frac{1}{Lo \cdot \frac{Co \cdot Cpt}{Co + Cpt}}} \qquad \omega = 7.7656404 \cdot 10^{7}$$

$s := \omega \cdot i$

$z2 := root\left[n3 \cdot s^{3} + n2 \cdot s^{2} + n1 \cdot s + n0, s\right]$

$z2 = -1.9722866 \cdot 10^{3} + 7.7656391 \cdot 10^{7}\, i$

***** Zeros:

$z1 = -9.9792906 \cdot 10^{5}$

$z2 = -1.9722866 \cdot 10^{3} + 7.7656391 \cdot 10^{7}\, i$

**********Poles:

**Coefficients for Poles:

$d0 := 1$

$d1 := (Co \cdot Ro + Co \cdot Rext + Ctop \cdot Rlt + Ctop \cdot Rext + Cbot \cdot Rlt + Cpt \cdot Rext)$

$$d2 := \begin{bmatrix} Co \cdot Lo + Co \cdot Ctop \cdot Ro \cdot Rlt + Co \cdot Ctop \cdot Ro \cdot Rext + Co \cdot Ctop \cdot Rlt \cdot Rext \ \ldots \\ + Co \cdot Cbot \cdot Ro \cdot Rlt + Co \cdot Cbot \cdot Rlt \cdot Rext + Co \cdot Cpt \cdot Ro \cdot Rext \qquad \ldots \\ + Ctop \cdot Cbot \cdot Rlt \cdot Rext + Ctop \cdot Cpt \cdot Rlt \cdot Rext + Cbot \cdot Cpt \cdot Rlt \cdot Rext \end{bmatrix}$$

$d3 := Co \cdot Ctop \cdot Lo \cdot Rlt + Co \cdot Ctop \cdot Lo \cdot Rext + Co \cdot Cbot \cdot Lo \cdot Rlt + Co \cdot Cpt \cdot Lo \cdot Rext \ \ldots$

$+ Co \cdot Ctop \cdot Cbot \cdot Ro \cdot Rlt \cdot Rext + Co \cdot Ctop \cdot Cpt \cdot Ro \cdot Rlt \cdot Rext \qquad \ldots$

$+ Co \cdot Cbot \cdot Cpt \cdot Ro \cdot Rlt \cdot Rext$

$d4 := Co \cdot Ctop \cdot Cbot \cdot Lo \cdot Rlt \cdot Rext + Co \cdot Ctop \cdot Cpt \cdot Lo \cdot Rlt \cdot Rext \ \ldots$

$+ Co \cdot Cbot \cdot Cpt \cdot Lo \cdot Rlt \cdot Rext$

guess first pole location:

$$\omega := \frac{-1}{(Rext)\cdot(Ctop + Cbot + Cpt)} \qquad \omega = -2.3809524\cdot 10^{5}$$

$s := \omega$

$$p1 := root\left[d4\cdot s^{4} + d3\cdot s^{3} + d2\cdot s^{2} + d1\cdot s + d0, s\right]$$

$p1 = -2.492\cdot 10^{5}$

guess second pole location (this is dominant pole)

$$\omega := \frac{-1}{Rlt\cdot\left[Cbot + \frac{Ctop\cdot Cpt}{Ctop + Cpt}\right]} \qquad \omega = -5.6423611\cdot 10^{5}$$

$s := \omega$

$$p2 := root\left[d4\cdot s^{4} + d3\cdot s^{3} + d2\cdot s^{2} + d1\cdot s + d0, s\right]$$

$p2 = -8.6971683\cdot 10^{5}$

guess complex pole pair location:

$$\omega := \frac{-1}{\sqrt{Lo\cdot\frac{Co\cdot(Cpt + Ceq)}{Co + Cpt + Ceq}}} \qquad \omega = -7.7620652\cdot 10^{7}$$

$s := i\cdot\omega$

$$p3 := root\left[d4\cdot s^{4} + d3\cdot s^{3} + d2\cdot s^{2} + d1\cdot s + d0, s\right]$$

$p3 = -1.3566881\cdot 10^{3} - 7.7620647\cdot 10^{7}\, i$

**********Summary:**********

$tp := 2\cdot\pi$

$z1 = -9.9792906\cdot 10^{5}$ $\qquad \frac{z1}{tp} = -1.5882534\cdot 10^{5}$

$z2 = -1.9722866\cdot 10^{3} + 7.7656391\cdot 10^{7}\, i$ $\qquad \frac{z2}{tp} = -313.899161 + 1.2359398\cdot 10^{7}\, i$

10

$p1 = -2.492351 \cdot 10^{5}$

$p2 = -8.6971683 \cdot 10^{5}$

$p3 = -1.3566881 \cdot 10^{3} - 7.7620647 \cdot 10^{7}\, i$

$\frac{p1}{tp} = -3.9666998 \cdot 10^{4}$

$\frac{p2}{tp} = -1.3841973 \cdot 10^{5}$

$\frac{p3}{tp} = -215.9236169 - 1.235371 \cdot 10^{7}\, i$

**********System Function:**********

$$H(s) := \frac{gm \cdot Rlt \cdot \left[n3 \cdot s^{3} + n2 \cdot s^{2} + n1 \cdot s + n0\right]}{d4 \cdot s^{4} + d3 \cdot s^{3} + d2 \cdot s^{2} + d1 \cdot s + d0}$$

**********Plot System Function**********

$x := 1 \,..80$

$l_x := \frac{x}{10}$

$\omega x := \sqrt{\left[tp \cdot 10^{l}\right]}$

$20 \cdot \log\left[\left|\left[H\left[i \cdot \omega x_x\right]\right]\right|\right]$

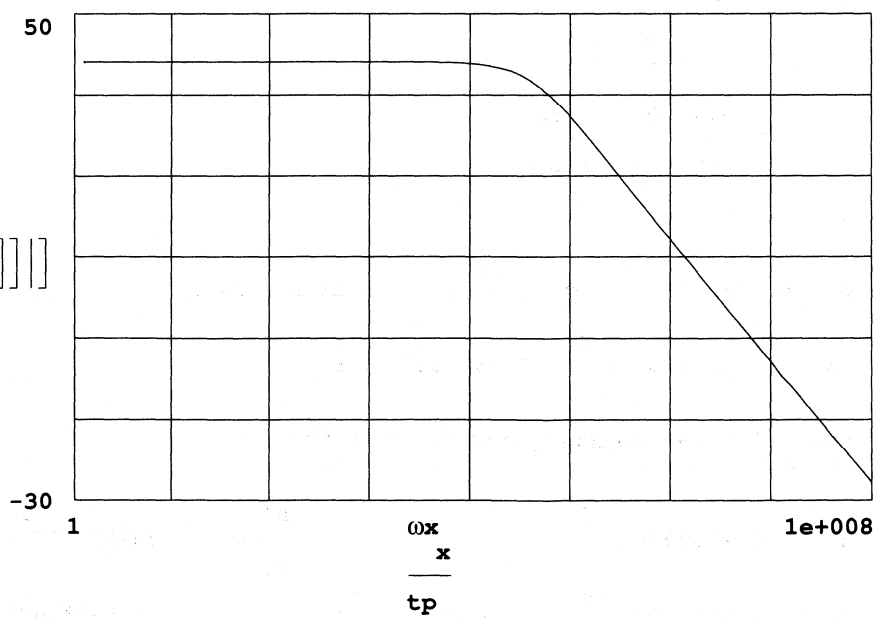


Figure 11A

plot phase:

$$Ph := \left[\arg(H(i \cdot \omega x)) \cdot \frac{180}{\pi} \right]$$

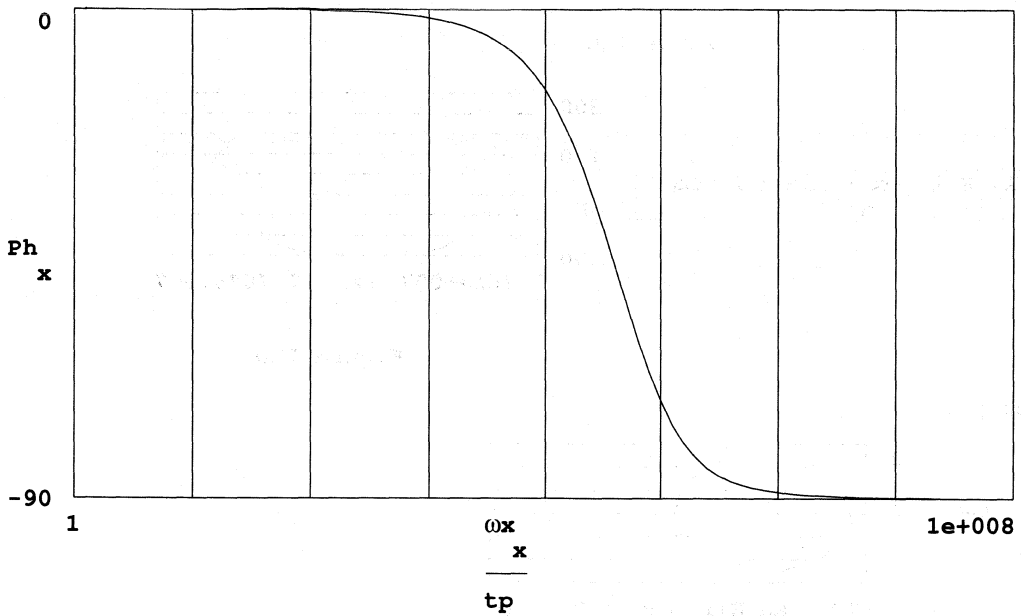


Figure 11B

plot an expanded area around the complex pole/zero pair:

$n := 0 \ldots 100$

$range := (|Im(z2)| - |Im(p3)|) \quad range := range \cdot .2$

$lo := |Im(p3)| - range$

$hi := |Im(z2)| + range$

$$\omega x_n := \left[(hi - lo) \cdot \frac{n}{100} + lo \right]$$

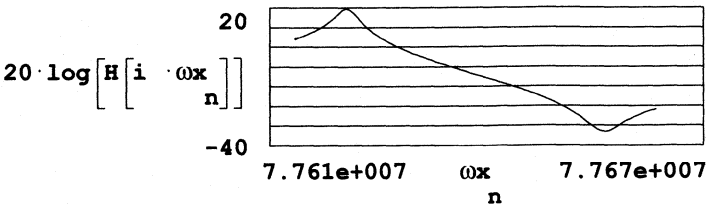


Figure 11C

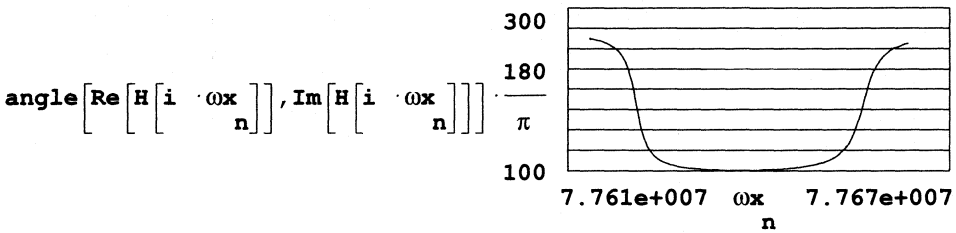


Figure 11D

Nyquist plot:

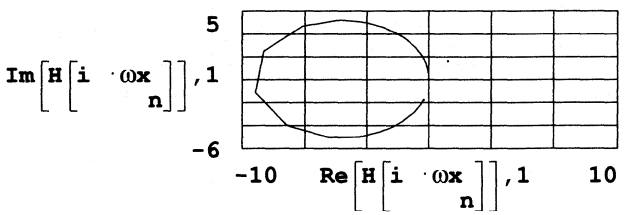


Figure 11E

$\omega g := i \cdot (Im(p3) + 10)$ $\qquad \frac{\omega g}{tp} = -1.2353708 \cdot 10^{7}\, i$

Find exact frequency of phase zero crossing due to complex pole pair:

$\omega osc := root(Im(H(\omega g)), \omega g)$

check:
$arg(H(\omega osc)) = 180 \cdot deg$

Exact zero phase frequency and amplitude:

$\frac{\omega osc}{tp} = -1.2353722 \cdot 10^{7}\, i$ $\qquad |H(\omega osc)| = 9.41$

Find exact zero phase and amplitude due to complex zero pair:

guess first:

$\omega g := i \cdot (Im(z2) - 100)$

$\frac{\omega g}{tp} = 1.2359383 \cdot 10^{7} i$

$\omega zer := root(Im(H(\omega g)), \omega g)$

check:

$arg(H(\omega zer)) = -179.999 \cdot deg$ $\quad |H(\omega zer)| = 0.02$ amplitude

$\frac{\omega zer}{tp} = 1.2359386 \cdot 10^{7} i$ frequency

Find phase margin for oscillator (maximum phase between complex pole and zero pair):

$\omega x_n := -\left[(|\omega zer| - |\omega osc|) \cdot \frac{n}{105} + |\omega osc| + 100 \right]$

$\pi - \max\left[\overrightarrow{angle(Re(H(i \cdot \omega x)), Im(H(i \cdot \omega x)))}\right] = -79.361 \cdot deg$

10

APPENDIX B

This goes through an example calculation of the reduction in small signal gm due to a certain amplitude across Ctop or the gate of the MOS device. The analysis can be carried out in a more general manner and graphs can be plotted out for the purpose of providing a graphical solution to ascertain the final oscillation amplitude given an initial set of bias conditions. The procedure is for example purposes only. If the reader requires more specific information, please contact Micro Linear directly.

This analysis was carried out in MathCAD.

define some numbers:

MOS transistor threshold voltage: $vt := .926$

MOS transistor k factor: $\beta := \frac{700}{4.2} \cdot 47 \cdot 10^{-6}$

$\omega := 1$ here, frequency doesn't matter, so make it 1

$vbq := 1.158$ dc bias value of gate to source

simple MOS equation for drain current

$$id(vgs) := if\left[vgs > vt, \left[\frac{1}{2} \cdot \beta \cdot (vgs - vt)^2\right], 0\right]$$

$idq := id(vbq)$ calculate dc bias current

$idq := 2.112 \cdot 10^{-4}$

$vin(t,vb) := vb + a \cdot \cos(\omega \cdot t)$ define the gate to source excitation

$gmq := \sqrt{2 \cdot \beta \cdot id(vbq)}$ small signal gm at dc bias

$gmq = 0.0018173$

Find the average bias voltage of vgs which MUST equal the dc bias current:

$TOL := 10^{-8}$ guess $vb := vbq - .2$

Given

$$\frac{1}{2 \cdot \pi} \cdot \int_0^{2 \cdot \pi} id(vin(t,vb))\, dt \approx idq$$

$newvb := Find(vb)$

$newvb = 0.898$ $vbq = 1.158$ compare to new bias

check:

$$\left[\frac{1}{2\cdot\pi}\cdot\int_0^{2\cdot\pi} id(vin(t,newvb))\ dt\right] = 2.112\cdot 10^{-4}$$

This represents a shift of:

vbq - newvb = 0.26 volts in vgs bias

for a sine wave amplitude of:

a ≡ .5 volts peak of vgs (note: this is NOT the output voltage!)

This gives a steady state vgs of:

vg(t) := vin(t,newvb)

The first harmonic of the drain current is:

$$id1 := \frac{1}{\pi}\cdot\int_0^{2\cdot\pi} id(vg(t))\cdot\cos(\omega\cdot t)\ dt$$

$id1 = 3.624\cdot 10^{-4}$ The large signal gm, or GM is now calculated:

$$GM := \frac{id1}{a} \qquad GM = 7.247\cdot 10^{-4}$$

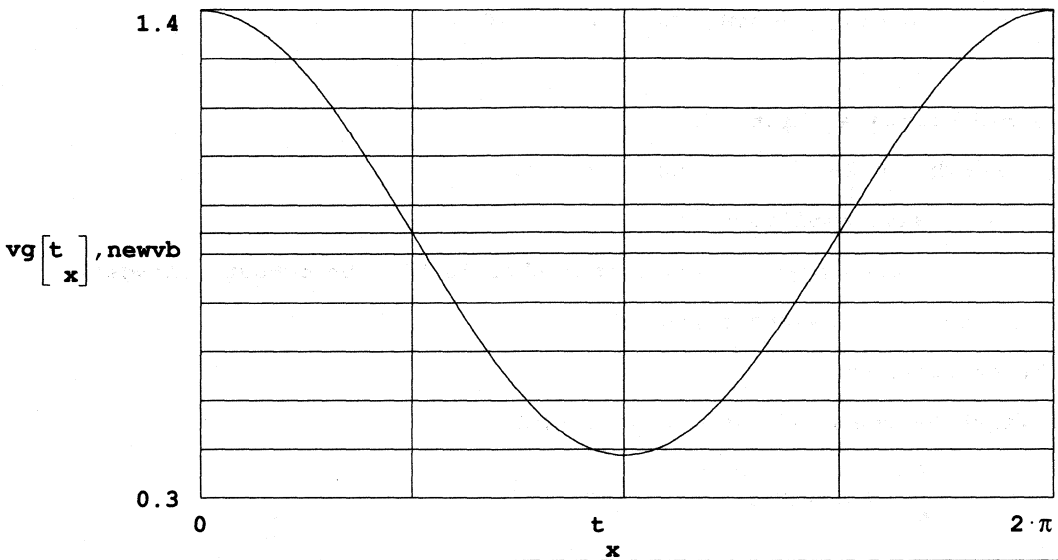
The normalization of GM/gm is now shown:

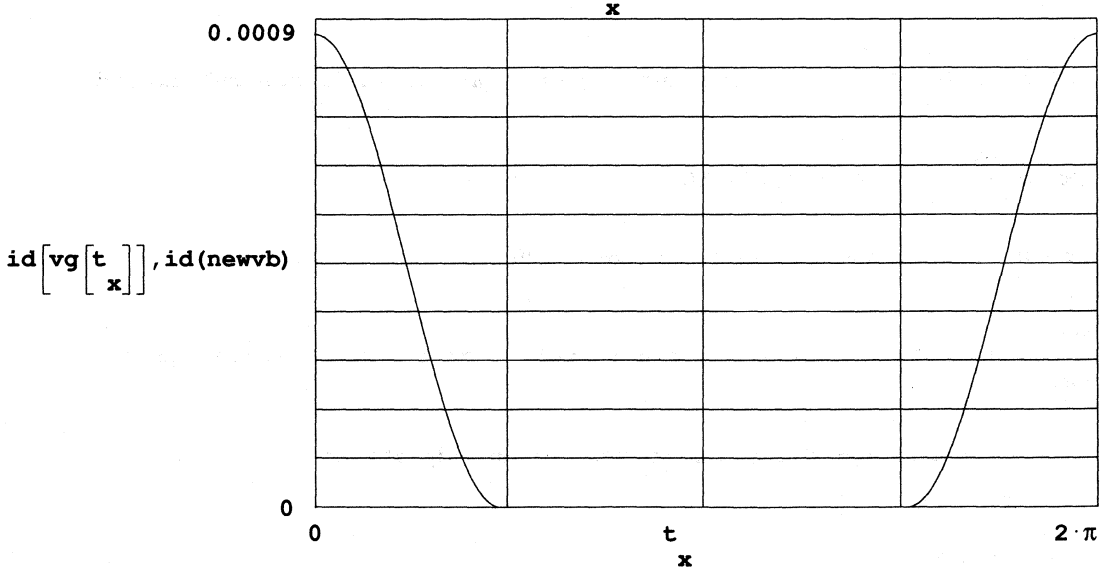
$\frac{GM}{gmq} = 0.399$ This shows a reduction of the small signal gm.

Plot gate voltage and drain current in steady state:

x := 0 ..255

$$t_x := \frac{2\cdot\pi\cdot x}{255}$$


1.4
vg[t, x], newvb
0.3
0
t
x
2·π


0.0009
id[vg[t, x]], id(newvb)
0
0
t
x
2·π

APPENDIX C

Oscillator Root Locus Calculation

This calculates the real and imaginary parts of the closed loop transfer function. The real part is the time constant of the initial exponential startup transient.

define a range of gm values to calculate over:

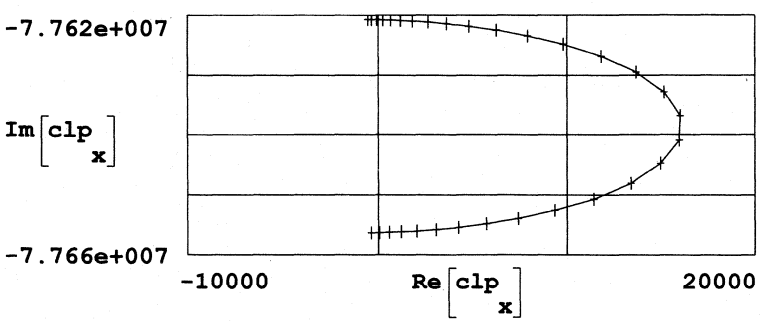
$x := 40 \,..10$

$$gm_x := 10^{-\left[\frac{x}{10}\right]} \qquad TOL \equiv 10^{-6}$$

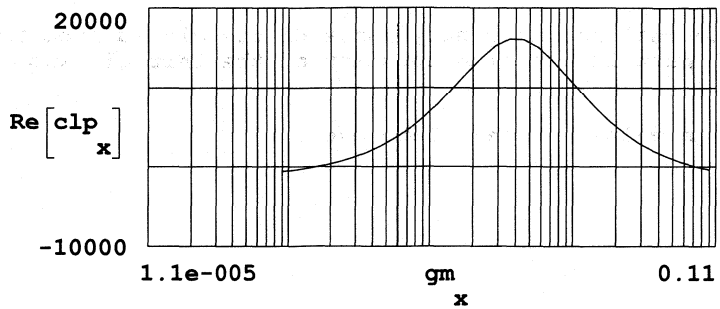
Calculate root locus for gm. These are the roots of the characteristic equation of the closed loop transfer function. See Appendix A for the definitions of the coefficients shown below:

$$clp_x := root\left[\left[\begin{array}{l} d4 \cdot s^4 + \left[d3 + n3 \cdot gm_x \cdot rmb\right] \cdot s^3 + \left[d2 + n2 \cdot gm_x \cdot rmb\right] \cdot s^2 \ldots \\ + \left[d1 + n1 \cdot gm_x \cdot rmb\right] \cdot s + d0 + n0 \cdot gm_x \cdot rmb \end{array}\right], s\right]$$

Root Locus Plot:



Real part of closed loop transfer function versus gm:



Note in the above plot that there is a limited range of gm's for which the poles of the closed loop transfer function remain in the right half plane. In other words, too low a gm creates too low a gain. However, too high gm values also violate the Nyquist Criterion.

APPENDIX D

This shows how to calculate the real part of the on chip bias resistor Rp for inclusion in the loop gain calculations. This was done on MathCAD.

This is a calculation of the Real part of a distributed RC network with one end shorted to ground. A parallel R part is calculated.

ORIGIN := 1 $\qquad$ $m := 1 \,..3$

Following DC resistance values are for the ML2031, ML2035, and ML2200. The total capacitance is also calculated for the network.

$$r0 := \begin{bmatrix} 3 \\ 240 \cdot 10 \\ 3 \\ 640 \cdot 10 \\ 6 \\ 10 \end{bmatrix} \qquad c0_m := r0_m \cdot 100 \cdot .08 \cdot \frac{10^{-15}}{4 \cdot 10^{3}}$$

Define a range of frequencies to use: $n := 1 \,..40$

$$f_n := n \cdot \frac{10^{6}}{2} \qquad \omega := (f \cdot 2 \cdot \pi)$$

Calculate the admittance of the distributed network:

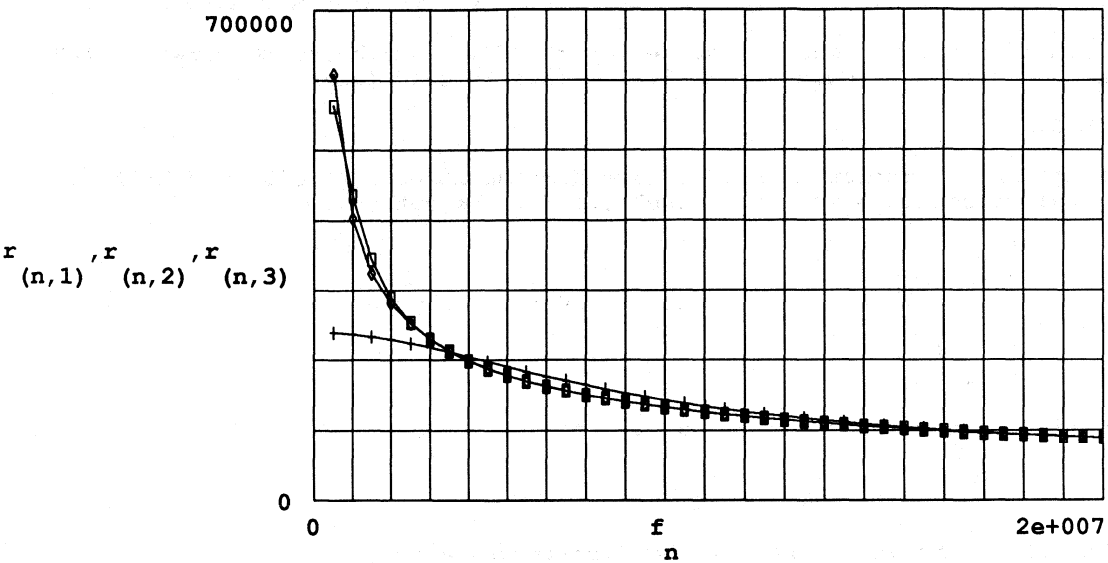
$$\Gamma_{n,m} := \sqrt{i \cdot \omega_n \cdot c0_m \cdot r0_m} \qquad Z0_{n,m} := \sqrt{\frac{r0_m}{i \cdot \omega_n \cdot c0_m}} \qquad y1 := \left[\frac{1}{Z0 \cdot \tanh(\Gamma)}\right]$$

Extract the real part and invert to get resistance:

$$r := \left[\frac{1}{Re(y1)}\right]$$

10

Plot the real part versus frequency:



diamonds=ML2200, boxes=ML2035, pluses=ML2031

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Application Note 10

An Improved Method of Load Fault Detection

High frequency supply designs pose unique problems in fault detection. A typical method of output fault detection in most standard controllers is to provide a cycle-by-cycle current limit (V_{TH1}) to limit the peak current in the output switch. In addition, these controllers have a second current limit (V_{TH2}), which is typically set 40% higher than the cycle by cycle limit. Crossing V_{TH2} on the I_{SENSE} input resets the Soft Start circuit and allows current in the output to decay before re-starting the system.

In theory, by the time the power output stage can begin to turn off from having crossed V_{TH1}, the output current will have exceeded V_{TH2} and a soft start reset wil be performed. This technique works well if leakage inductance is low and turn-off delay is high enough to cause enough energy to transfer to the output inductor, causing the current to build up in subsequent cycles (figure 2a). This current build up takes place when the output is short circuited because the output inductor has almost no voltage across it and therefore a very shallow discharge slope. If, however, energy transfer is low due to fast turn-off of the outputs (which is desirable to minimize switching losses) energy transfer to the output inductor will be minimized, resulting in the supply continually running at the cycle by cycle current limit to a short circuit with no reset occurring (figure 2b).

High frequency controllers are designed to minimize T_{PD} and turn off the output MOSFET gates quickly. This implies that the event which triggers soft start reset will not persist for very long if it is detected at all. The short persistence of the triggering event requires that Q1 discharge C1 in a very short time, typically resulting in a partial discharge and an inadequate reset. A solution to this problem (figure 3) is implemented in all of Micro Linear's PWM IC's. Flip-flop (F2) and comparator (A4) are added to the circuit, to ensure a full reset. If desired, a delay (as implemented in the ML4809 and ML4811) can also be added before restart, which lowers the system's effective duty cycle allowing the supply to cool down.

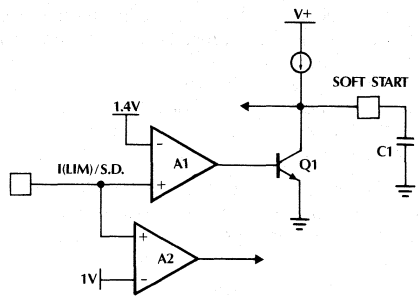

Figure 1. Typical Two Threshold Current Limit/Fault Detect

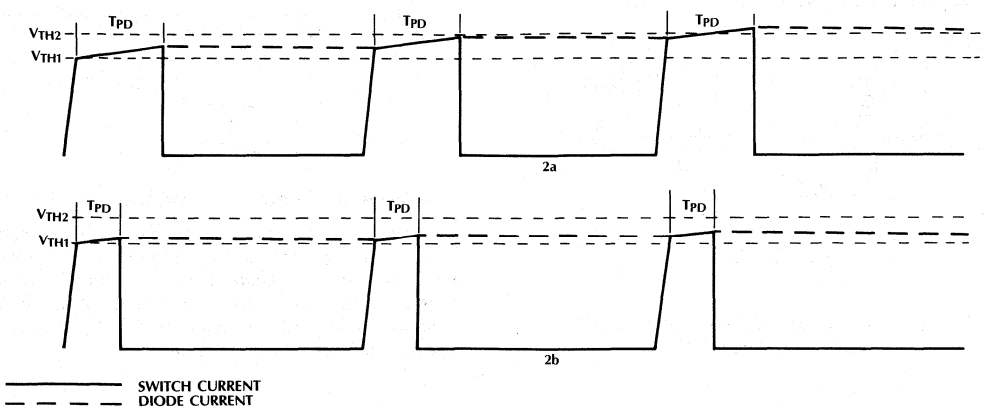

Figure 2. Current Waveforms During Output Short Circuit Slow Output Turn-Off (2a) and Fast Turn-Off (2b)

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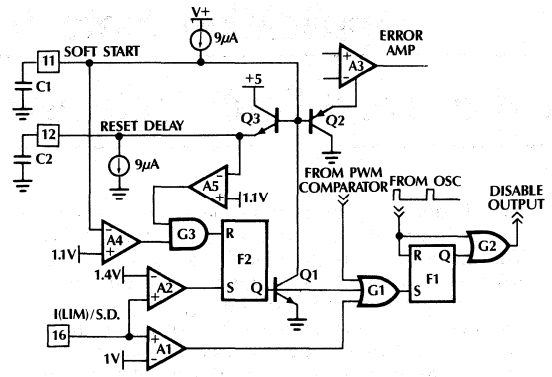

Figure 3. Improved Soft Start Reset with Delay — ML4809

Integrating Fault Detection

The "two threshold" detection technique described above limits the system designer's freedom to optimize his magnetics and minimize switching time. Since detecting the fault relies on building inductor current up on successive cycles, propagation delay cannot be minimized (as shown in figure 2) for this technique to work. Since these two parameters are important terms in high frequency supply efficiency, the need to compromise due to inadequacies in fault detection presents a problem.

A method of circumventing this problem involves "counting" the number of times the controller terminates the PWM cycle due to the cycle by cycle current limit.

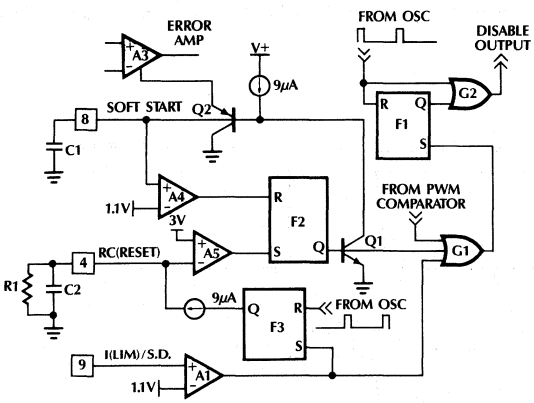

Figure 4. Integrating Soft Start Reset Circuit with Delay (ML4811)

Figure 4 shows the Integrating Fault Detect circuit. When the I_{LIM} signal (switch current) crosses the 1.1V threshold A1 signals the F1 to terminate the cycle and sets F3, which is reset at the beginning of each PWM cycle. The output of F3 turns on a current source to charge C2. When, after several cycles, C2 has charged to 3V, A5 turns on F2 to discharge soft start capacitor C1. Charge is continually bled from C2 by R1. If a current surge is short lived (for instance a disk drive start-up or a board being plugged in to a live rack) the control can "ride out" the surge (figure 5a) with the switch protected by the cycle by cycle limit. R1 and C1 can be selected to track diode heating, or to ride out various system surge requirements as required.

If the high current demanded is caused by a short circuit (figure 5b), the duty cycle will be short and the output diodes will carry the current for the majority of the PWM cycle. C2 charges fastest for low duty cycles (since F3 will be on for a longer time) providing for quicker shutdown during short-circuit when the output diodes are being maximally stressed.

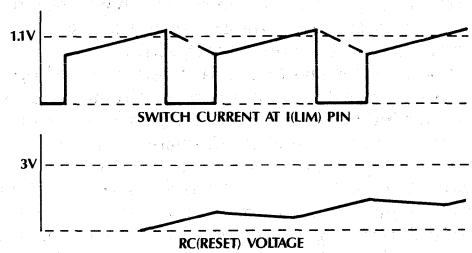

Figure 5a. Integrating Fault Detection Response to Load Surge

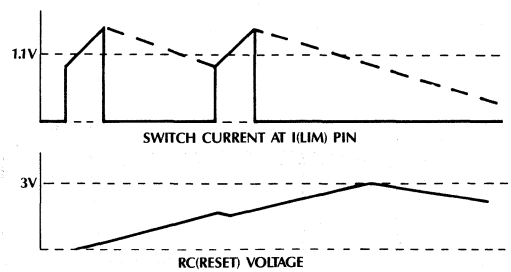

Figure 5b. Response to Load Fault (Short Circuit)

The Integrating Fault Detection circuit allows reliable detection of output faults independent of supply magnetics and propagation delays. Additionally, this method of fault detection is inherently noise immune, programmable, and can distinguish between load surges and load faults (short circuits).

Micro Linear

Application Note 11

Mehmet K. Nalbant

Power Factor Enhancement Circuit

A simple enhancement circuit for the ML4812 is described. The circuit which will be called the power factor enhancement circuit greatly improves the power factor while reducing the total harmonic distortion of the current waveform.

The circuit details for implementing the power factor enhancement circuit are given below. Figure 1 shows the schematic diagram of the circuit. The circuit operates by generating a small DC current bias and injecting it into the I_{SINE} (pin 6) input of the ML4812. This current injection has the net effect of improving the zero current crossover distortion. It does this by lifting the shoulders of the current waveform around the zero crossover areas.

The circuit in the dotted lines in Figure 2, shows the details of the implementation. The circuit automatically adjusts the amount of the injected DC bias as a function of the line voltage. The reason behind the variable amount of DC current injection is that at lower input voltages, the amount of DC bias that is required is less.

Based on experience, the amount of bias required at 220 VAC is approximately four times higher than at 120 VAC. The proper scaling can be adjusted by choosing appropriate values for the various resistors used and the zener diode voltage. The amount of bias that is required is a function of the boost inductor value and the ramp compensation. For best performance the value of the inductor should be chosen as high as possible which in turn will necessitate a small amount of ramp compensation.

One way to find the required bias currents is summarized below: the first step is to find the optimum bias at the nominal operating point, for example, at 120 VAC. This is done by connecting a variable resistor to the reference output of the IC. The initial value of the resistor is selected such that, the bias current equals the peak to peak ramp compensation voltage when the duty cycle is at its maximum. After the optimum value at the nominal operating conditions is found the input voltage is increased to 220 VAC and the same procedure above is repeated to find the optimum value of the resistor at the 220 VAC nominal operating conditions. The bias currents corresponding to the two resistor values above can be used to calculate the values of the components in the enhancement circuit. The formulas for calculating the various components are given below:

$$V_{C3\ (VIN)} = \frac{0.9V_{IN(RMS)}\ R6}{R1 + R2 + R6} \quad (1)$$

$$I_{ISINE(VIN)} = \frac{V_{C3} - V_{BE} - V_Z - V_{ISINE}}{R7} \quad (2)$$

$$r = \frac{I_{ISINE(220\ VAC)}}{I_{ISINE(120\ VAC)}} \quad (3)$$

$$r = \frac{V_{C3(220\ VAC)} - V_{BE} - V_Z - V_{ISINE}}{V_{C3(120\ VAC)} - V_{BE} - V_Z - V_{ISINE}} \quad (4)$$

Where:

$I_{ISINE(VIN)}$ = Bias current into the I_{SINE} input as function of the input voltage.

V_{BE} = Base emitter voltage of Q3 (0.7V nominal).

V_{ISINE} = Voltage at I_{SINE} input, typically 0.7V.

r = Ratio of bias current at 220 VAC input to the bias current at 120 VAC input.

By chosing a value for $V_{C3(220\ VAC)}$ the value of $V_{C3(120\ VAC)}$ is also found. These two values can be substituted to the equation above to calculate the required value for V_Z. The value of R7 can be found by using (2). The values of the remaining components can be calculated by using (1).

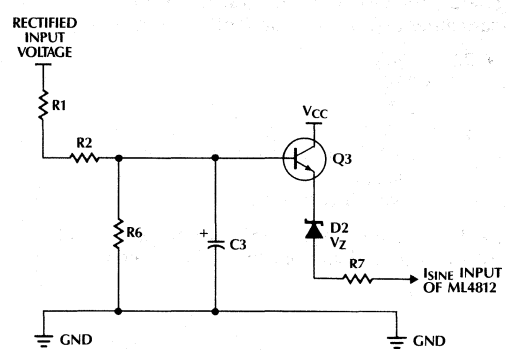

Figure 1. The Enhancement Circuit

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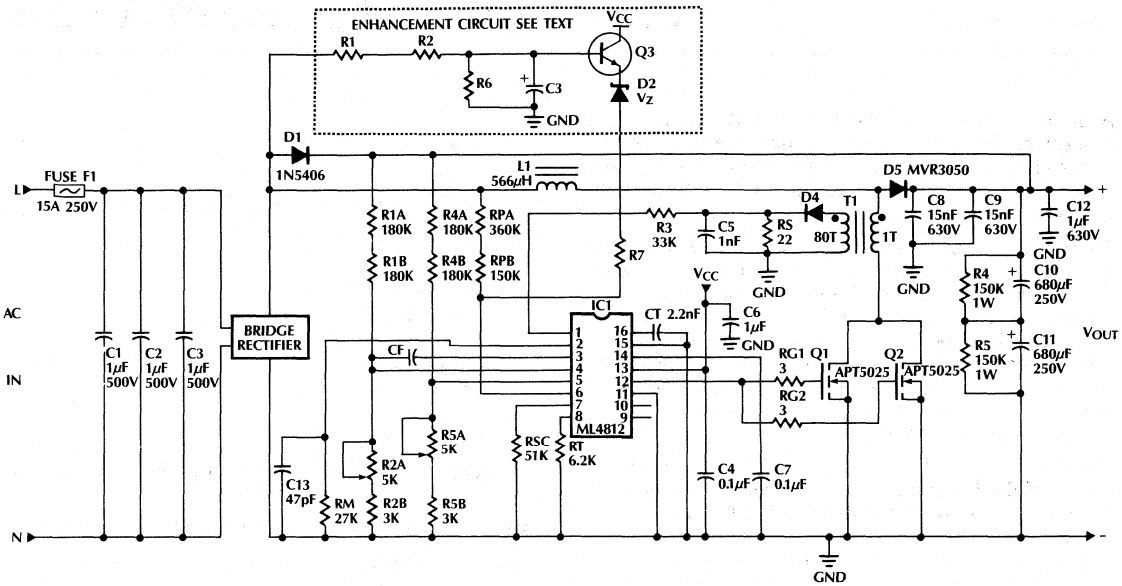


Figure 2. 1KW Enhanced Power Factor Correction Circuit

The circuit of Figure 2, is a 1KW input, power factor regulator. For this circuit the values of the enhancement circuit components were as follows:

R1 + R2 = 330K
R6 = 22K
R7 = 22K
D2, V_Z = 3.5V
Q3 = 2N2222 or any equivalent small signal transistor.
C3 = 10μF electrolytic cap

Table 1 shows the performance of the power factor regulator with and without the enhancement circuit.

Table 1. Effect of Enhancement Circuit on Power Factor

Input Voltage (VAC)	Input Power (W)	Power Factor	
		With Enhancement	Without Enhancement
120	742	.998	.991
	365	.994	.976
220	706	.996	.976
	352	.969	.940

Micro Linear

Application Note 12

Generating Phase Controlled Sinewaves with the ML2036

Vince Cardinale

Introduction

The 16-bit resolution of the ML2036 combined with its Inhibit feature makes it a powerful tool for generating precision sinewaves. It can produce frequencies from DC to 50kHz in 1Hz increments with –40dB harmonic distortion *and* has the control to stop the output at any given time or at the next zero crossing, *with no external components.*

Precise phase control can also be obtained with the addition of a few external devices. With the addition of phase control two or more ML2036 sinewave generators can be synchronized at any angle from 0 to 360 with better than 1 degree resolution.

Inhibit Mode

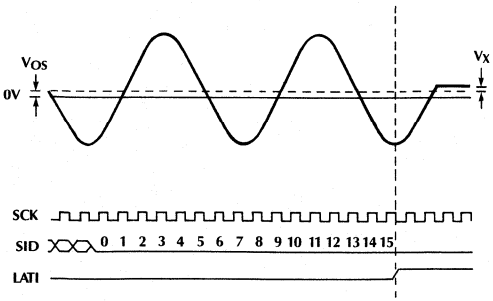
In order to place the ML2036 in Inhibit mode three conditions must occur simultaneously. The three-level P_{DN}–INH input pin must be at the V_{SS} voltage (–5V), the shift register must be loaded with all zeros, and the LATI pin must be a logic "1" (+5V). Once these three conditions are met the output continues to operate until it reaches $V_{OS} + |V_X|$ if the next zero crossing is positive going, or $V_{OS} - |V_X|$ if the next zero crossing is negative going, and then holds this level (see figure 1). The output will stay at this voltage until a new frequency is loaded into the data latch, at which point the output will continue where it left off. If the output stopped at zero after approaching from below 0V then it will start-up going positive. If it stopped after approaching from above 0V then it will start-up going negative.

Initialization

In order to synchronize the ML2036 you must first initialize it so it will start up at a known point in the sinewave. By using the Inhibit mode you can stop the part at 0V but you can't be sure from which direction it approached zero, or more importantly which direction it will start-up. If you can guarantee that it stopped while approaching from below 0V then you can be sure it will start-up going positive. This can be done if the LATI pin is not allowed to be high when the output is above ground. The circuit in figure 2 and the following procedure demonstrate how this can be implemented.

Initialization Procedure

1) Power up
2) Set LAT high
3) Set INH low
4) Load MSB: **0001 0000 0000 0000** :LSB
5) Set LAT low
6) Wait at least 1 output cycle time
7) Load all 0s
8) Set INH high (INH must go high before LAT by at least a NAND gate delay)
9) Set LAT high
10) Wait at least 1.5 output cycle times
    Output stops at 0V going high
11) Load desired frequency
12) Set LAT low
    Output begins at 0V going high
13) Set INH low



$$|V_X| = \frac{V_{PEAK}}{256} \text{ ; For } f_{OUT} \leq \frac{f_{CLK}}{2048}$$

$$|V_X| \leq \frac{V_{PEAK}}{256} + V_{PEAK} \text{ Sine} \left(\frac{8\pi f_{OUT}}{f_{CLK}} + \frac{\pi}{512} \right)$$

$$\text{For } f_{OUT} > \frac{f_{CLK}}{2048}$$

Figure 1. Inhibit Mode

10

Synchronization

At the completion of step 10 the part is initialized. Its output is stable at about 0V and will start up going positive. If you want to synchronize the output with some external event you can load the shift register with the desired frequency (step 11) and then set LAT low (step 12) synchronously with the external event. If you want to synchronize two ML2036 sinewave generators together initialize them both as described, and then set LAT low (step 12) on both circuits simultaneously.

Precise phase control between two parts can be achieved by initializing both parts, starting one and then waiting a known time before starting the other. For example, to produce two 5kHz sinewaves with 90° phase shift you should wait 50μs between starting each circuit. Since the ML2036 uses a 3MHz reference clock to update the output (assuming a 12MHz clock is used to drive CLK_{IN}) the phase resolution will be 0.6°. This resolution will vary from 0.0012° for two 10Hz signals to 6° for two 50kHz signals.

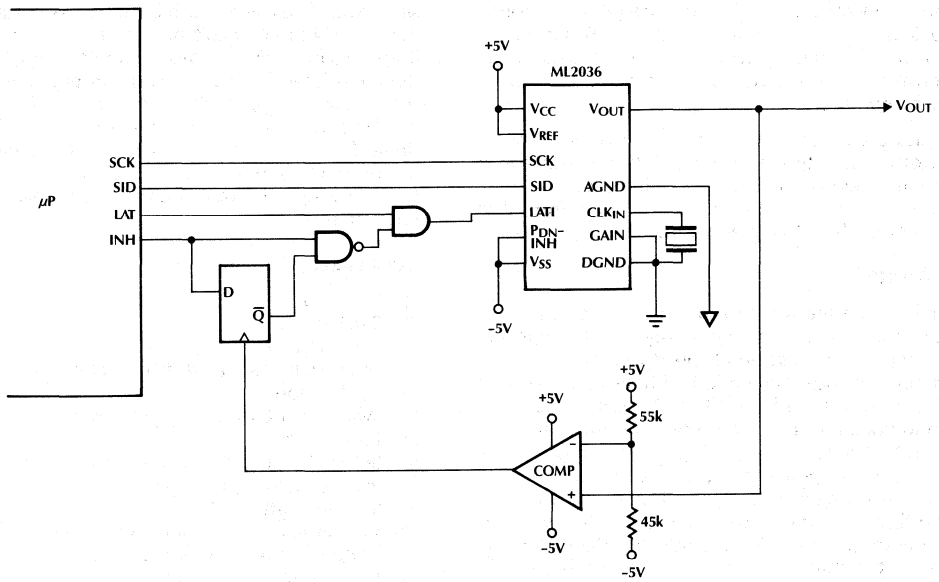


Figure 2.

Micro Linear

Application Note 13

William Cho

Designing with 10Base-T Transceivers

Micro Linear's family of 10Base-T transceivers offer highly integrated solutions for internal and external MAUs (Media Attachment Units) as well as HUB MAUs. These chips offer a high performance current drive transmitter with very low jitter and RFI noise. The ML4651, ML4652, ML4657, and ML4658 are 10Base-T transceivers that provide an AU interface for internal and external DTE MAUs while ML4654 and ML4655 provide TTL and ECL interfaces suited for Multiport Repeaters.

The following application note will cover some of the design issues that arise when designing either type of Media Attachment Units for Local Area Networks based on 10Base-T.

Internal (Embedded) MAUs with Shared AUI Port

Figure 1 shows a detailed schematic for an internal MAU design with a shared AUI (Attachment Unit Interface) port. The optional port requires additional circuitry as defined in the IEEE 802.3 specifications for proper termination and protection at the serial interface chip (or Manchester Encoder/Decoder) and the 10Base-T transceiver chip connected to an AUI port.

An AUI connection requires termination impedance of 78Ω on the receive end of the transmission lines (DI and CI). As such R1 and R2 in parallel with R3 and R4 provide the proper termination. This also applies to the receive output pins 4 and 5 of the transceiver chip. The 357Ω resistors for R3 and R4 was chosen to properly bias the driver circuitry (see section on AUI driver output). The 2kΩ values for R7 and R8 were chosen to provide the BIAS voltage for Tx+ and Tx– inputs. This also will not load down the 78Ω transmission line when the AUI port is connected and the transceiver chip is tri-stated. The output AUI drivers of the transceiver chip must be tri-stated to not load down the transmission lines when the AUI port is connected and the twisted pair port is disconnected. Powering down the chip will tri-state the outputs.

The transceiver can be powered down by switching V_{CC} to GND as shown or by switching the ground connection to open condition. A logic level MOSFET with an "on" resistance (R_{DSON}) of 0.5Ω or less can be used by connecting to the ground pin of the chip to power down the chip. When switching the ground off one must also include the ground connections of the driver resistors of COL and Rx outputs (R3, R4, R11, and R12). Another method of powering down the transceiver is to use an external mechanical switch as shown.

The isolation transformer is required for protection of the transceiver chip from 16V with respect to the system ground at the AUI interface during a fault condition as specified in 7.4.1.6. and 7.4.2.6 sections of the IEEE 802.3 standards for both the driver and the receiver.

If a shared AUI port is not required, then the design becomes simpler. Figure 13 of the datasheet shows AC coupling between the serial interface and the transceiver. This is to block DC bias voltage of the serial interface chip that may not match that of the transceiver. Micro Linear's transceivers require the input bias to be between 2.5V and 4.5V for CI and DI. If the two chips are compatible one can eliminate the AC coupling capacitors and bias resistors. By using a DC coupled interface, biasing the driver outputs is all that is needed for proper operation (Figure 2).

Twisted Pair Interface

The twisted pair connection to 10Base-T requires additional filtering and isolation components. The output structure of the twisted pair drivers are of the current drive type. This poses several very significant advantages when driving the twisted pair medium. Because the drivers are current driven, the differential outputs are well matched for a balanced signal transmission. Balanced transmission is crucial for meeting tight regulations on signal shapes. Also current driven outputs produce lower common-mode voltages for a lower EMI radiation. This can be a very significant issue when facing FCC regulations. Another advantage to current mode is that output drive, can be easily adjusted to compensate for losses in the transformer or output filter. RTSET will set the level of output drive current by the relationship:

$$RTSET = (RL/100) * 220$$

where RL is the characteristic impedance of the twisted pair cable.

The twisted pair differential output will see an effective resistance of 50Ω from the parallel combination of the two 200Ω resistors and reflected secondary AC line impedance of 100Ω for unshielded twisted pair. By driving 42mA to the 50Ω complex load, the differential signal voltage will swing ±2.5V peak around the 5V bias point when taking transients into consideration.

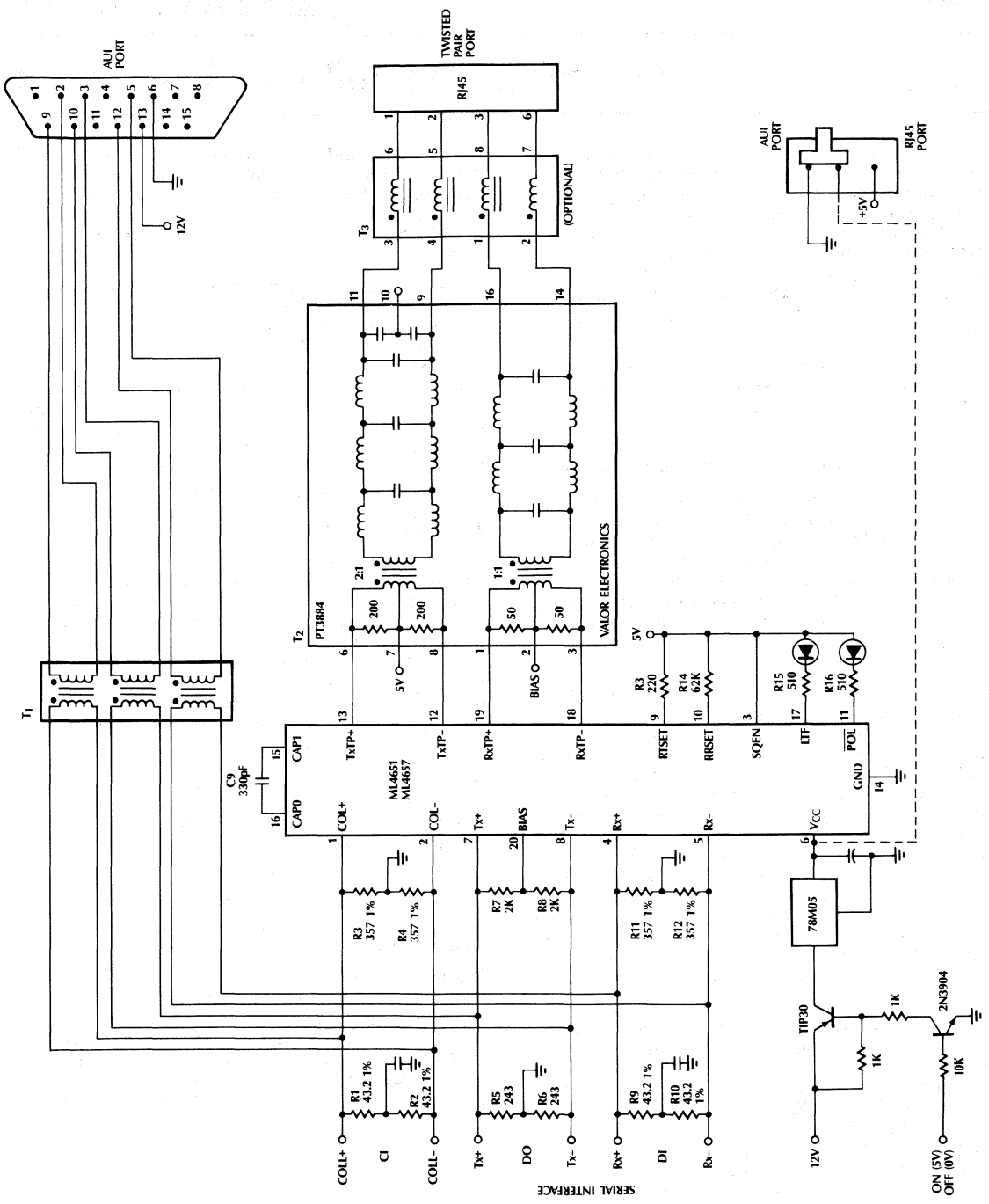


Figure 1. Internal MAU with Shared AUI Port

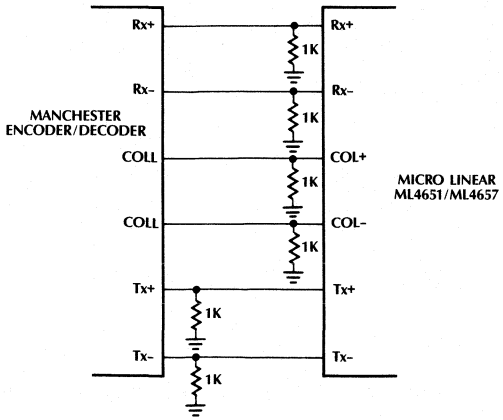
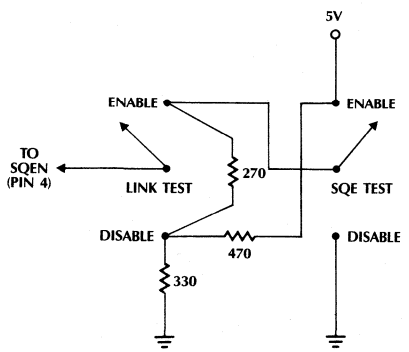


Figure 2. DC Coupled Interface for DTE Card Application

The isolation and filter components for both transmit and receive lines can all be integrated into one dip package style module. One such product can be obtained from Valor Electronics in San Diego. There are several other manufacturers who have these products available (refer to Figure 13 in the datasheet).

The output chokes shown in Figure 1 will pass any differential signal but block common mode voltages. Because Micro Linear's 10Base-T transceivers have very low common mode output voltage, this extra filtering choke may not be needed. Good board layout will also help.



SQE Test	Link Test	SQEN Pin 4
Enable	Enable	5V
Enable	Disable	3.3V
Disable	Enable	0V
Disable	Disable	1.2V

Figure 3. Mode Selection Circuit

External MAU

An external MAU design typically adds more LED outputs for status indication and adds circuitry for configuring the chip for SQE and Link Test options (See Figure 12 of datasheet). The selection of SQE and Link Test circuitry can be implemented in various ways. One such option is to use two SPDT switches to produce the proper voltage levels (Figure 3). The selected voltage to the SQEN input pin (pin #4 for ML4652 and ML4658) will internally configure the chip for the option to activate SQE test or Link test.

AUI Driver Output

The output structure of the driver stage connecting to the AUI is an open emitter type. The output is biased at typically 4.2V when high and 3.6V when low. That is a differential voltage of about ±0.6V across a 78Ω load which calculates to about 7.7mA output current during transmission. A 360Ω resistor at the output pin sets its current at 11.7mA when high and 10mA when low. In the case when the positive output is high, the current (I_O) flowing out of its drive transistor is the sum of 7.7mA and 11.7mA (Figure 4). That means the current flowing out of the negative output is 10mA minus 7.7mA. It then becomes apparent that the termination resistance must be low enough as to not shut off either of the output drive transistors but not too low as to saturate the transistor and dissipate excessive power.

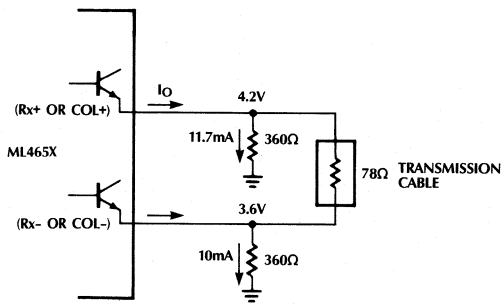


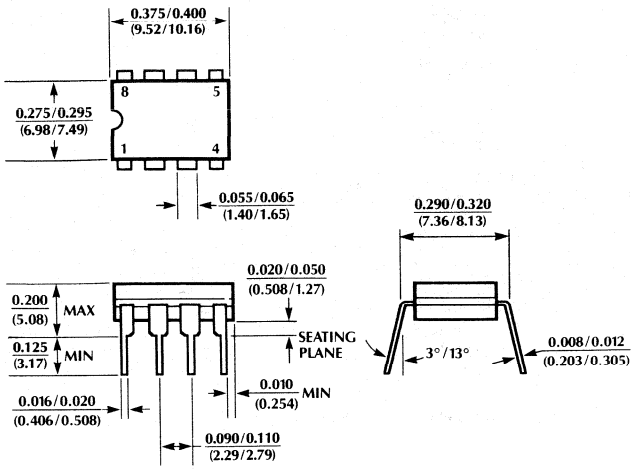
Figure 4. AUI Driver Circuitry

10

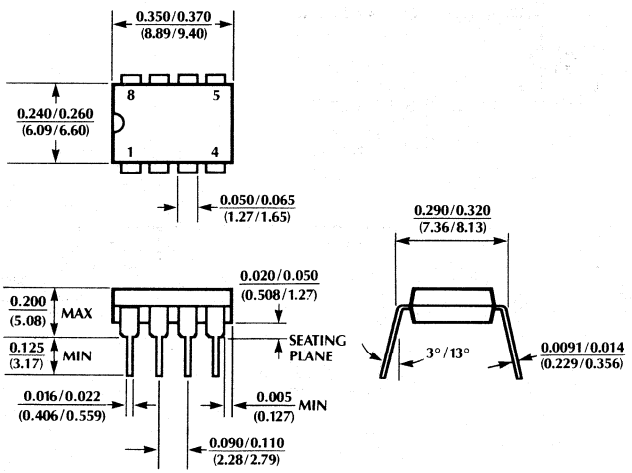
Packaging Information

Section 11

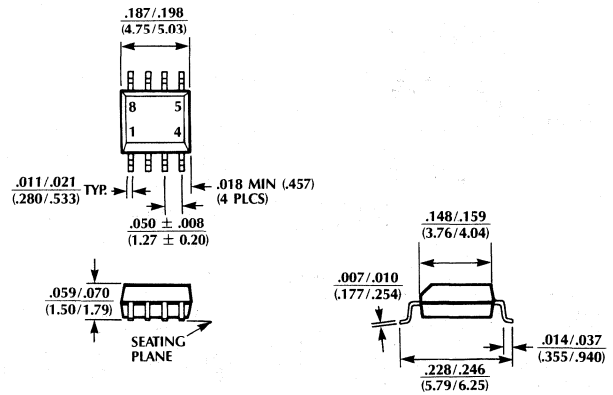
Package: J08
8-Pin Hermetic DIP (CERDIP)



Package: P08
8-Pin Molded DIP

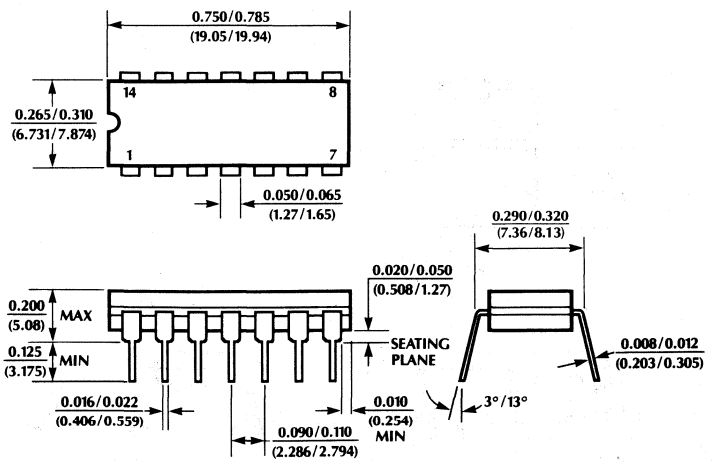


Package: S08
8-Pin SOIC

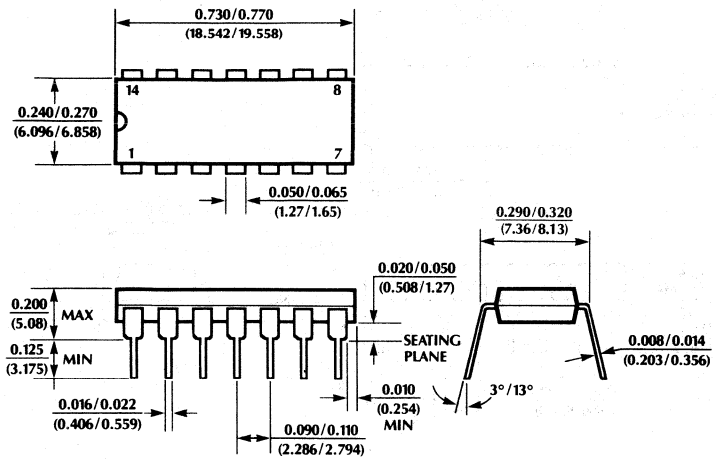


NOTE 1: SEATING PLANE LEAD COPLANARITY .005 (0.127) (BOTTOM OF LEADS).

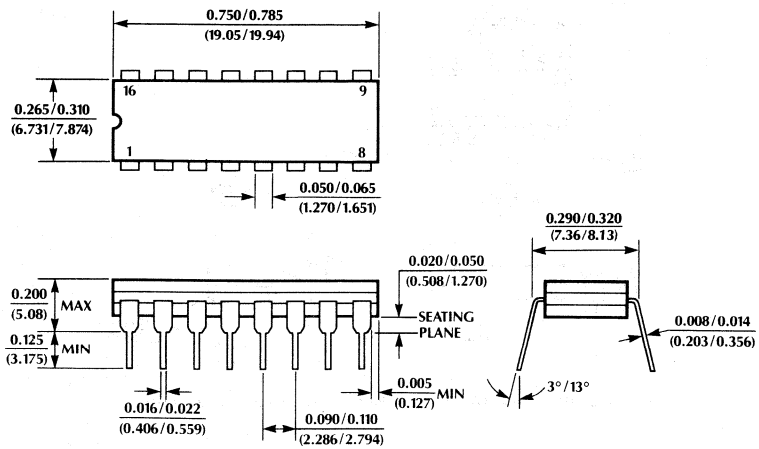
Package: J14
14-Pin Hermetic DIP (CERDIP)



Package: P14
14-Pin Molded DIP

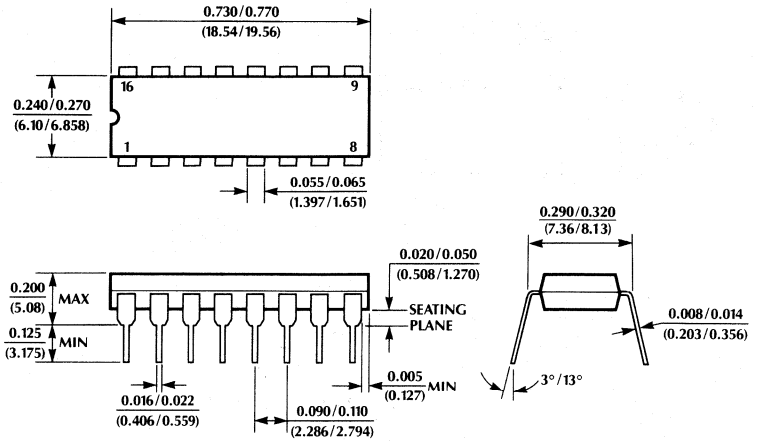


Package: J16
16-Pin Hermetic DIP (CERDIP)

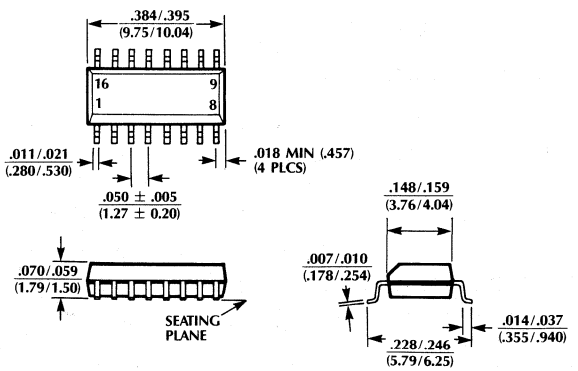


11

Package: P16
16-Pin Molded DIP

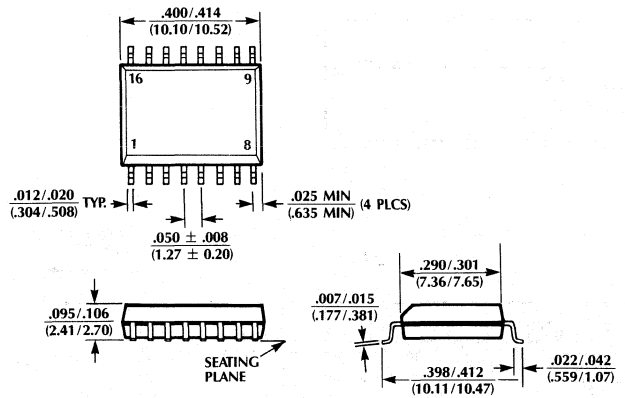


Package: S16
16-Pin SOIC (Narrow)



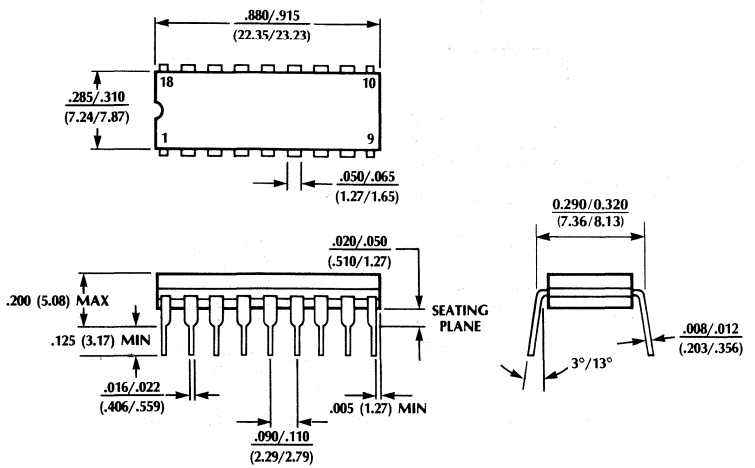
NOTE 1: SEATING PLANE LEAD COPLANARITY .005 (0.127) (BOTTOM OF LEADS).

Package: S16W
16-Pin SOIC (Wide)

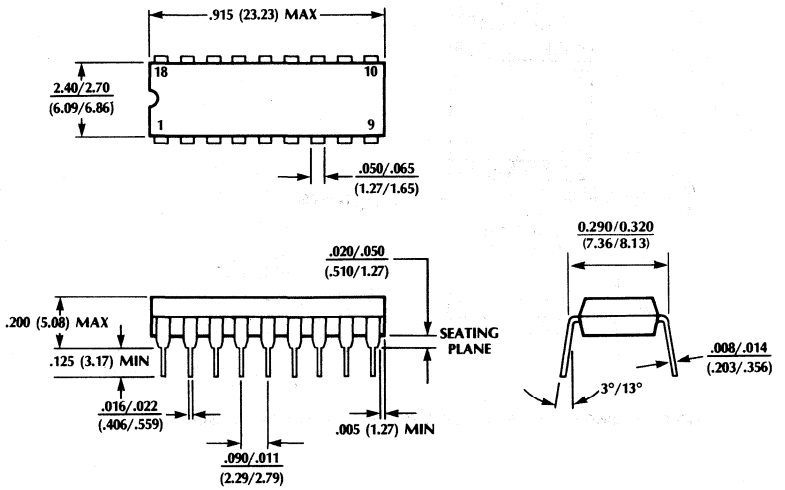


NOTE 1: SEATING PLANE LEAD COPLANARITY .005 (0.127) (BOTTOM OF LEADS).

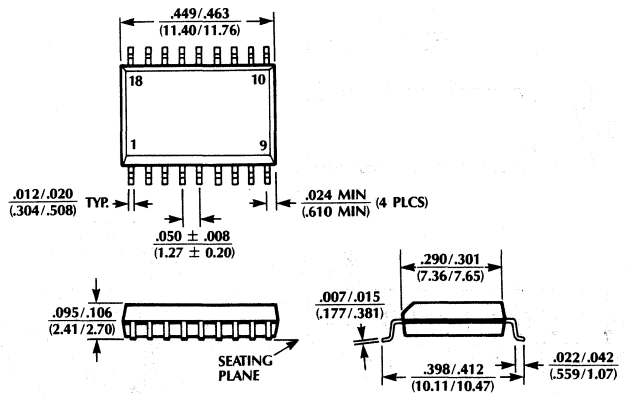
Package: J18
18-Pin Hermetic DIP (CERDIP)



Package: P18
18-Pin Molded DIP

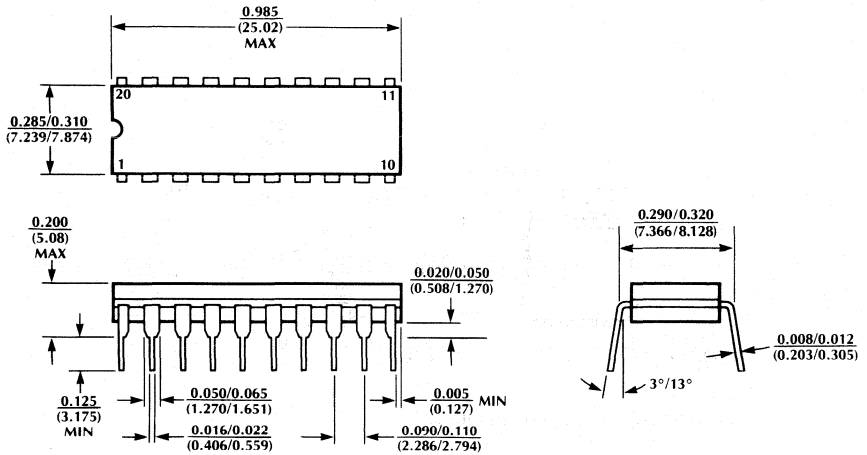


Package: S18W
18-Pin SOIC (Wide)

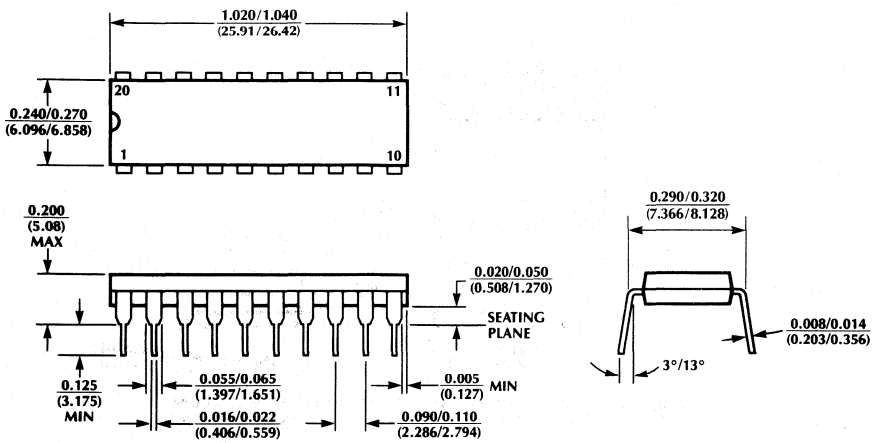


NOTE 1: SEATING PLANE LEAD COPLANARITY .005 (0.127) (BOTTOM OF LEADS).

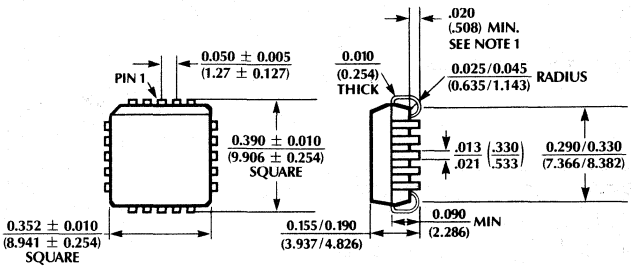
Package: J20
20-Pin Hermetic DIP (CERDIP)



Package: P20
20-Pin Molded DIP

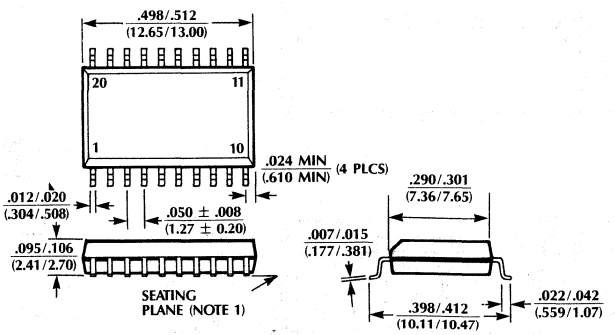


Package: Q20
20-Pin Molded Leaded PCC



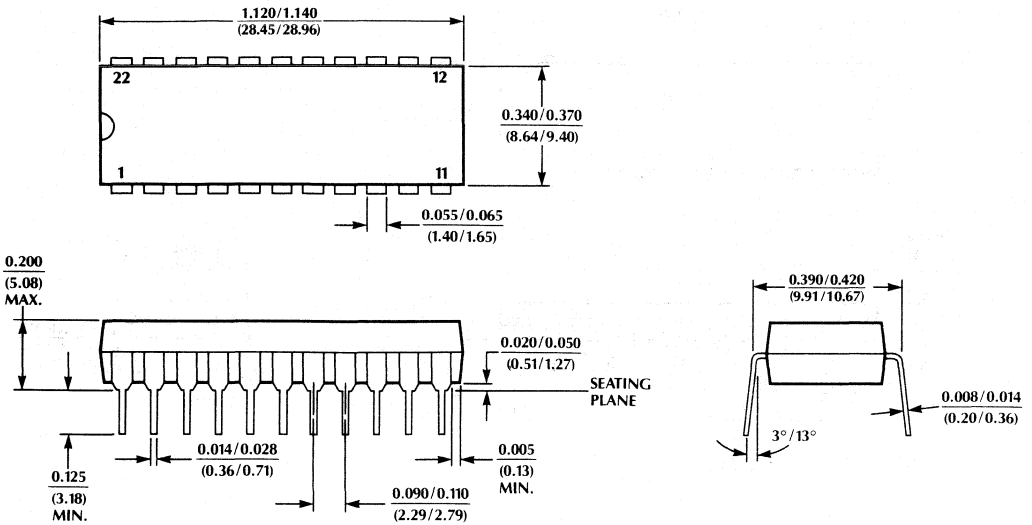
NOTE: SEATING PLANE LEAD COPLANARITY .005".

Package: S20W
20-Pin SOIC (Wide)

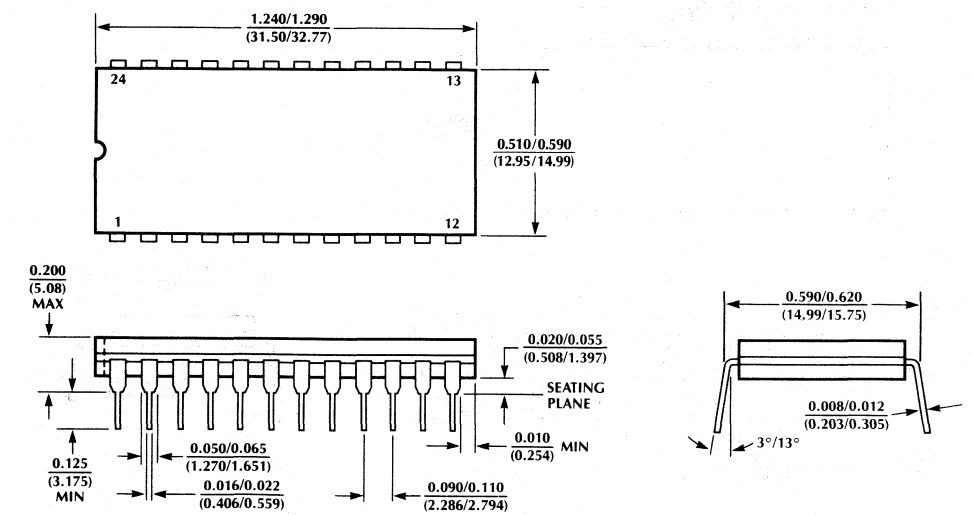


NOTE 1: SEATING PLANE LEAD COPLANARITY .005 (0.127) (BOTTOM OF LEADS).
NOTE 2: NOMINAL DIMENSIONS ±0.005 (0.127) UNLESS OTHERWISE SPECIFIED.

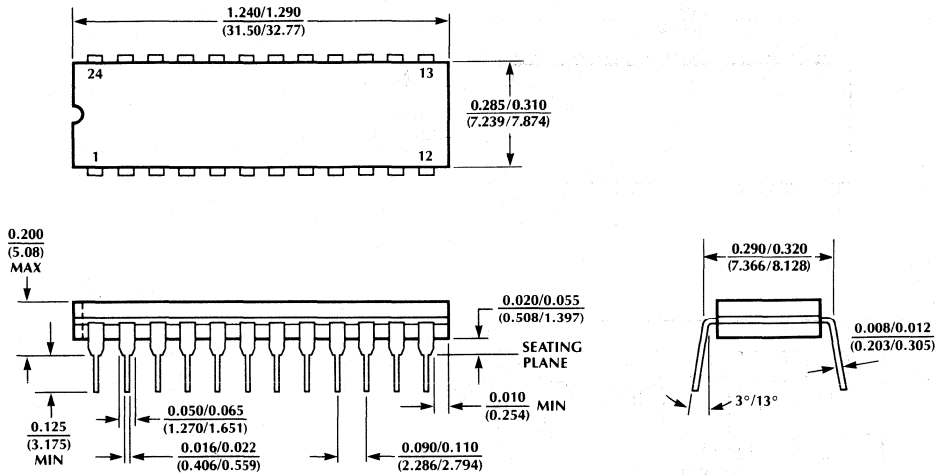
Package: P22
22-Pin Molded DIP



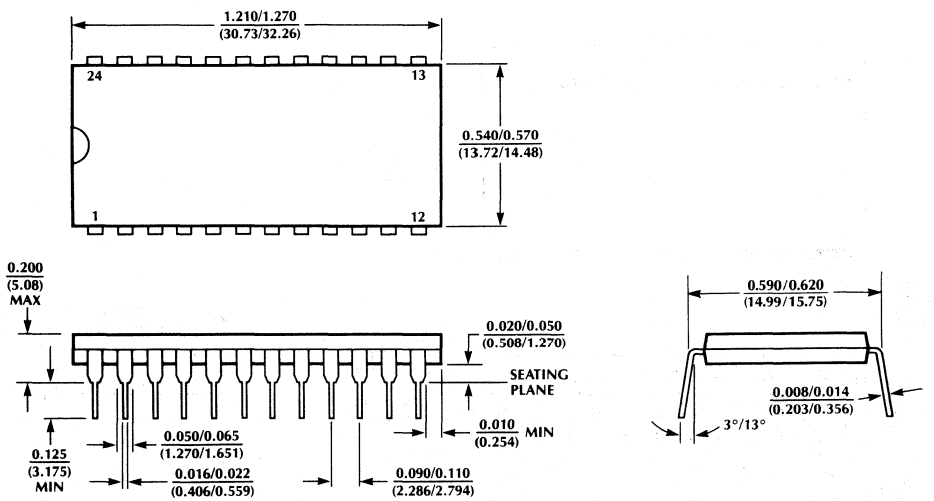
Package: J24W
24-Pin Hermetic DIP (CERDIP)



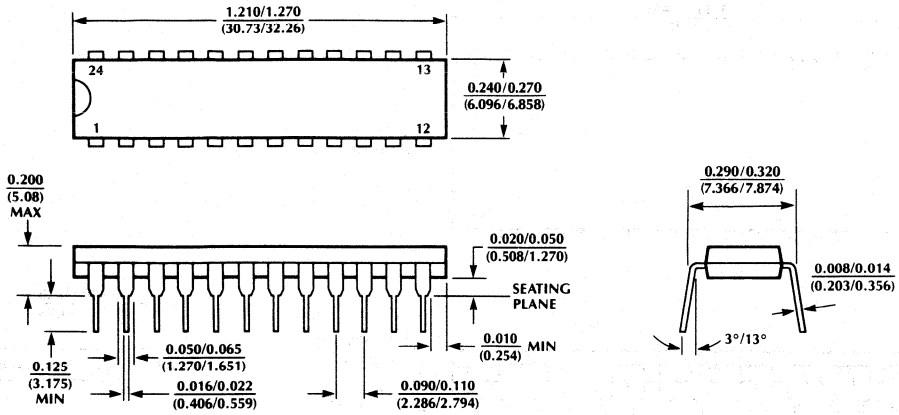
Package: J24N
24-Pin Hermetic Ceramic DIP (Narrow)



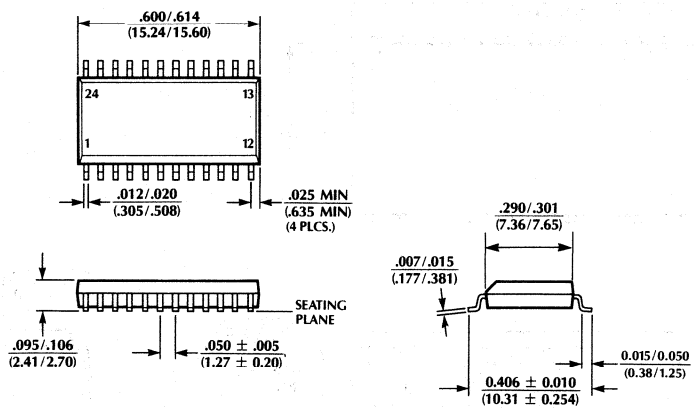
Package: P24W
24-Pin Molded DIP (Wide)



Package: P24N
24-Pin Molded DIP (Narrow)

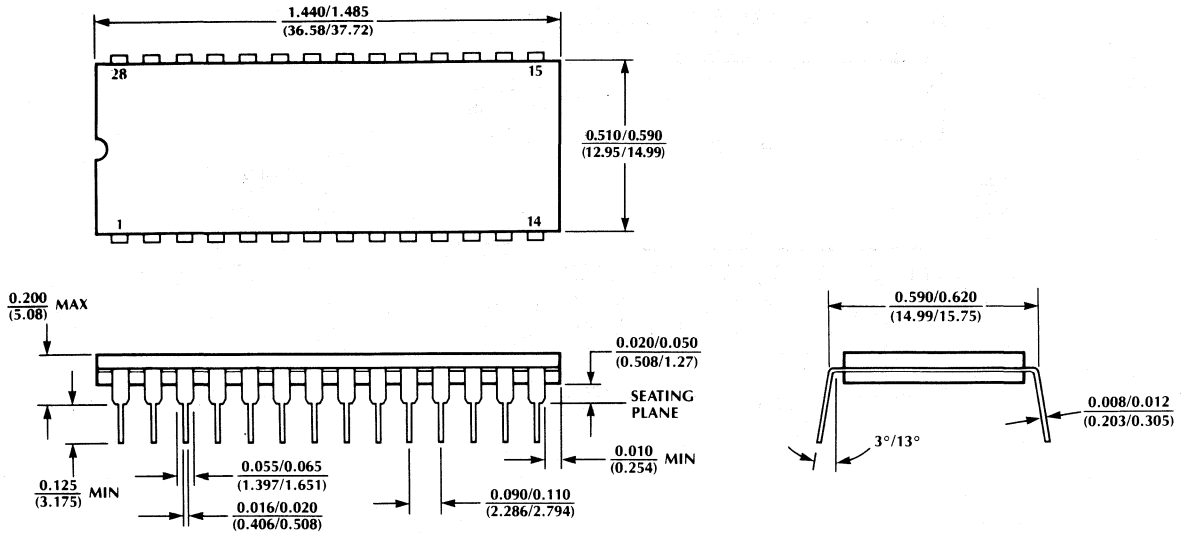


Package: S24W
24-Pin SOIC

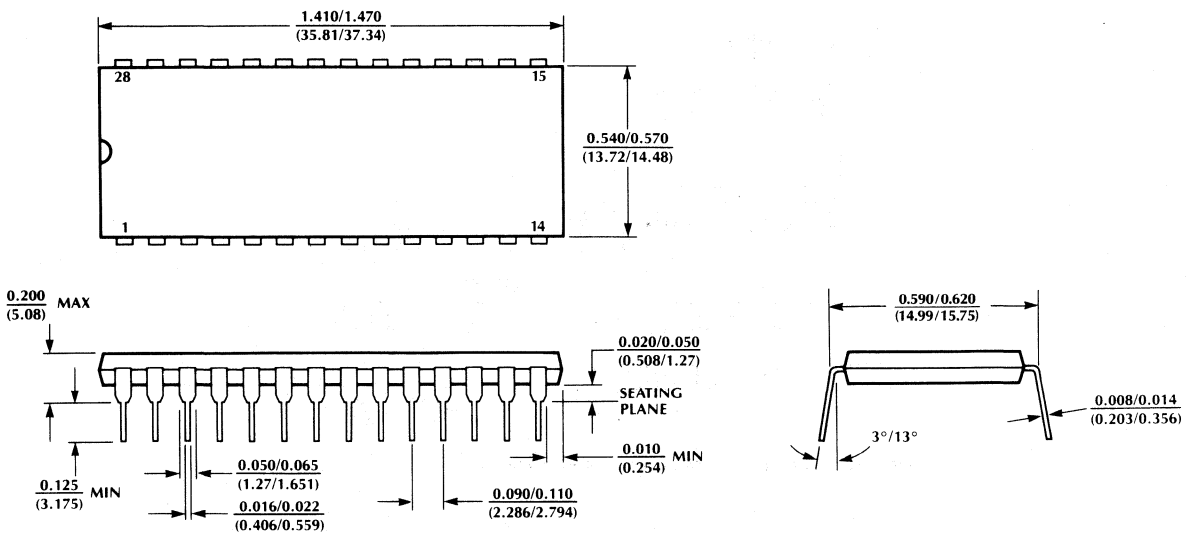


NOTE 1: SEATING PLANE LEAD COPLANARITY .005 (0.127) (BOTTOM OF LEADS).

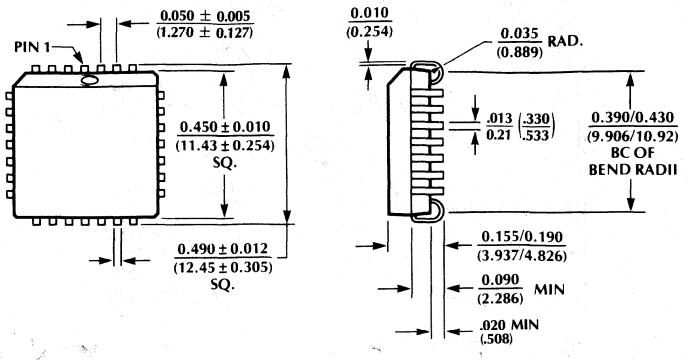
Package: J28W
28-Pin Hermetic DIP (CERDIP)



Package: P28W
28-Pin Molded DIP

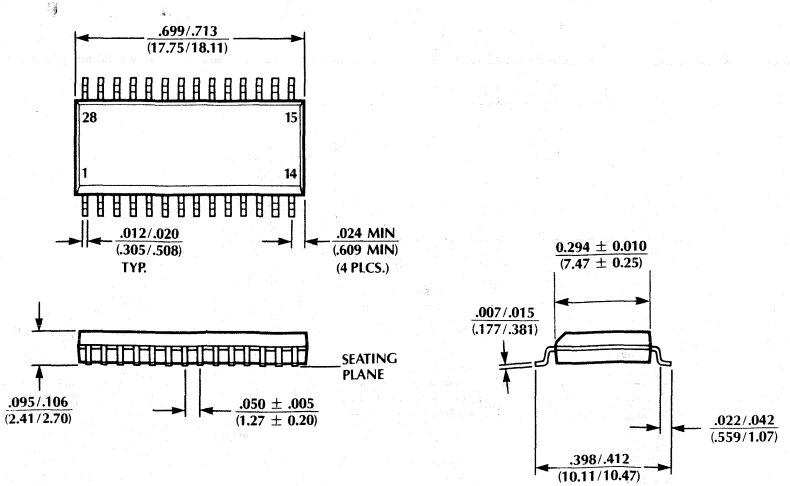


Package: Q28
28-Pin Molded Leaded PCC



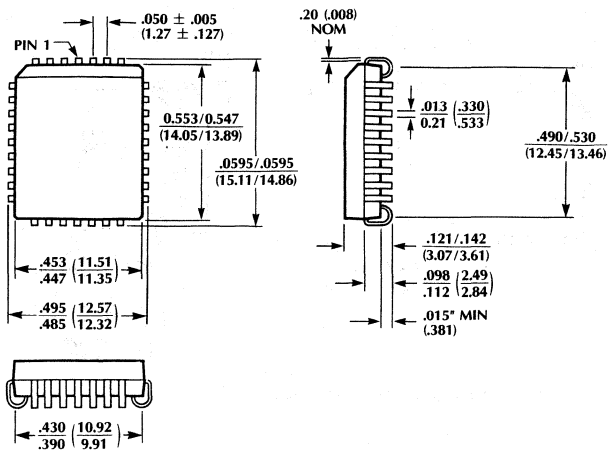
NOTE: SEATING PLANE LEAD COPLANARITY 0.005.

Package: S28W
28-Pin SOIC

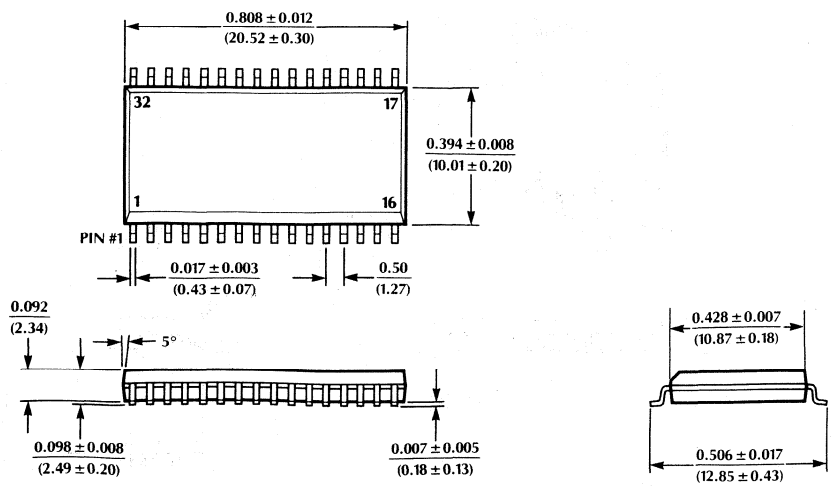


NOTE 1: SEATING PLANE LEAD COPLANARITY .005 (0.127) (BOTTOM OF LEADS).

Package: Q32
32-Pin Molded Leaded PCC

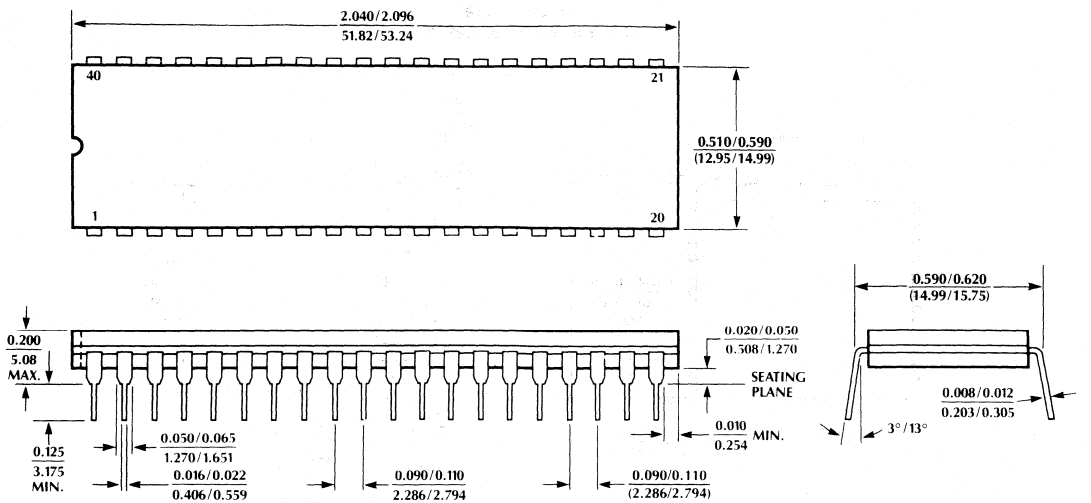


Package: S32W
32-Pin SOIC

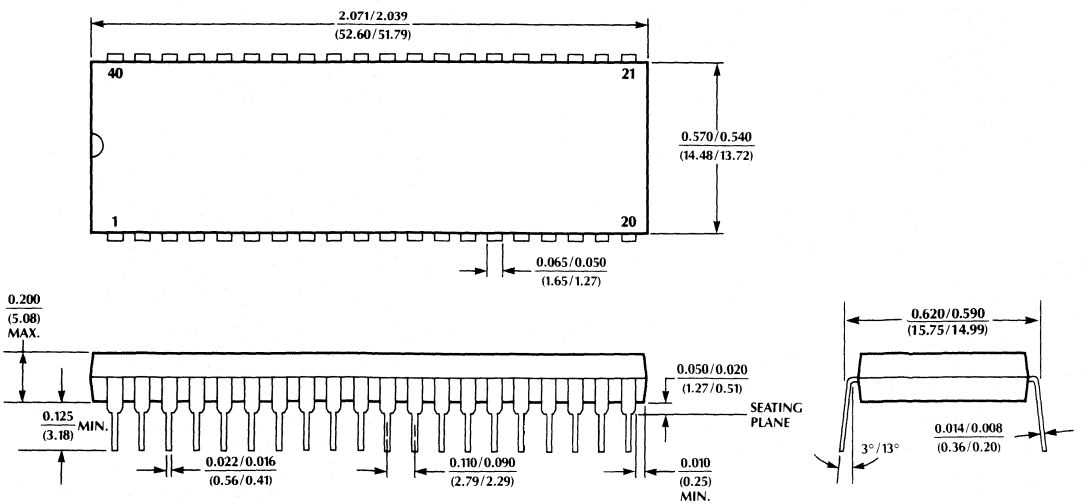


NOTE 1: SEATING PLANE LEAD COPLANARITY .005 (0.127) (BOTTOM OF LEADS).

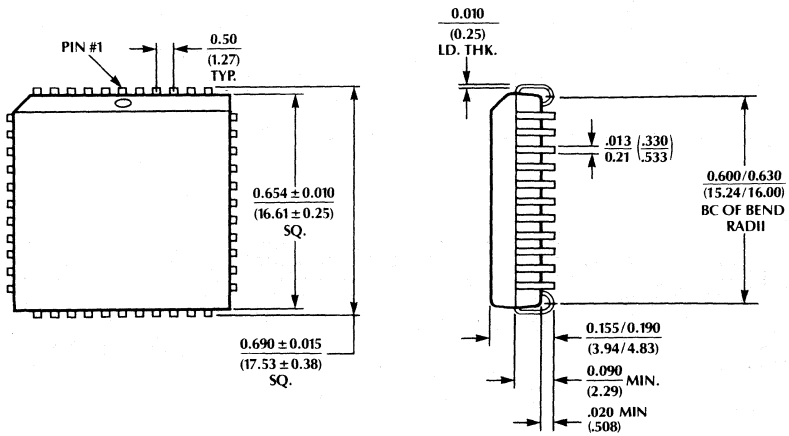
Package: J40
40-Pin Hermetic DIP (CERDIP)



Package: P40
40-Pin Molded Plastic DIP



Package: Q44
44-Pin Molded Leaded PCC



NOTE:
1. SEATING PLANE LEAD COPLANARITY ±.005

G520 GE/HP/CP 30K 1290 Printed in U.S.A.